1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram

ΣΔ CHARGE AMPLIFIER MUX

Y+ Z+
Y- Z-

X+ X-

DE MUX

ΣΔ Reconstruction Filter

Reconstruction Filter

Reconstruction Filter

Reg Array

SPI

CS SPC SDO/SDI SDO

CONTROL LOGIC & INTERRUPT GEN.

RDY/INT

SELF TEST

REFERENCE

TRIMMING CIRCUITS

CLOCK

Reserved NC

Vdd NC

GND NC

Reserved NC

Reserved NC

Vdd NC

GND NC

CK NC

Reserved NC

Y 1

X

Z

DIRECTIONS OF THE DETECTABLE ACCELERATIONS (TOP VIEW)