Figure 1. SPC560Px block diagram

e200z0 Core 32-bit

- Exception Handler
- Instruction Unit
- Load/Store Unit
- Instruction
- Branch Prediction Unit
- Special Purpose Registers
- Integer Execution Unit
- Exception Handler

1.2 V Regulator Control
XOSC
16 MHz RC Oscillator
FMPLL_0 (System)
FMPLL_1 (FlexRay, MotCtrl)
JTAG
Nexus Port Controller

eDMA2 × 16 channels

Instruction (32-bit)
Data (32-bit)

Crossbar Switch (XBAR, AMBA 2.0 v6 AHB)

Master
Slave
Slave
Slave

- Master
- FlexRay
- Slave
- FlexRay

Flash memory (with ECC)
SRAM (with ECC)

Peripheral Bridge

- FlexPWM
- 1.2 V Rail Vreg
- 2 × ADC
- Junc. Temp. Sensor
- 2 × eTimer (6 ch)
- 4 × DSPI
- 4 × ECSM
- PIT
- STM
- SWT
- Boot Assist Module
- System Integration Unit-Lite
- FlexCAN
- Safety Port
- Fault Collection Unit

CTU Cross Triggering Unit
DSPI Deserial Serial Peripheral Interface
ECSM Error Correction Status Module
eTimer Enhanced Timer
FlexCAN Flexible Controller Area Network
FlexPWM Flexible Pulse Width Modulation

FMPLL Frequency-Modulated Phase-Locked Loop
LINFlex Serial Communication Interface (LIN support)
PIT Periodic Interrupt Timer
SRAM Static Random-Access Memory
STM System Timer Module
SWT Software Watchdog Timer