Functional description

The main internal blocks are shown in the device block diagram in Figure 3. They are:

- A voltage regulator supplying the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available.
- A voltage monitor circuit which checks the input and the internal voltages.
- A fully integrated sawtooth oscillator with a frequency of 500 kHz ±15%, including also the voltage feed forward function and an input/output synchronization pin.
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high side driver for the internal P-MOS switch.
- An inhibit block for stand-by operation.
- A circuit to implement the thermal protection function.

Figure 3. Block diagram

5.1 Power supply and voltage reference

The internal regulator circuit (shown in Figure 4) consists of a start-up circuit, an internal voltage pre-regulator, the Bandgap voltage reference and the Bias block that provides current to all the blocks. The Starter supplies the start-up currents to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the Bandgap cell with a pre-regulated voltage VREG that has a very low supply voltage noise sensitivity.