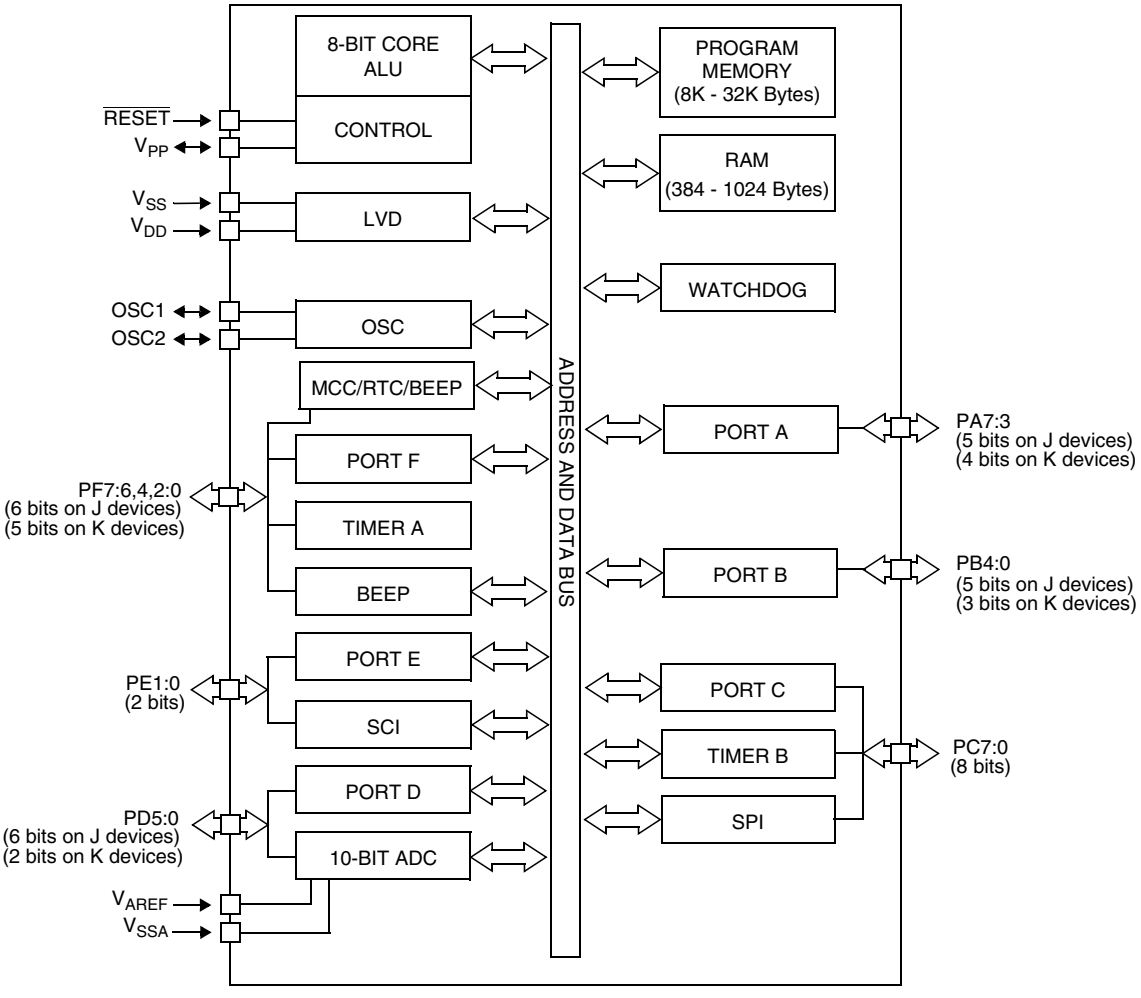
8-BIT CORE ALU
CONTROL
RESET
VPP
VSS
VDD
LVD
OSC1
OSC2
OSC
MCC/RTC/BEEP
PORT F
TIMER A
BEEP
PF7:6,4,2:0
(6 bits on J devices)
(5 bits on K devices)
PORT E
SCI
PE1:0
(2 bits)
PORT D
10-BIT ADC
PD5:0
(6 bits on J devices)
(2 bits on K devices)
VAREF
VSSA
ADDRESS AND DATA BUS
PROGRAM MEMORY
(8K - 32K Bytes)
RAM
(384 - 1024 Bytes)
WATCHDOG
PORT A
PA7:3
(5 bits on J devices)
(4 bits on K devices)
PORT B
PB4:0
(5 bits on J devices)
(3 bits on K devices)
PORT C
TIMER B
SPI
PC7:0
(8 bits)