Automotive 32-bit Microcontroller Technology & Product Roadmap

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STMicroelectronics
Automotive MCU Market Drivers

- Increase Levels of Security Level
- Increase Levels of Safety
- Increase Processing Power
- Increase Product Scalability
- Ensure Price competitiveness
- Increase Networking Capability
- Increase Quality levels
32-bit Automotive Microcontrollers

Market coverage

High performance

- High performance multicores with dedicated timing unit, Security and ASIL-D Safety

General Purpose

- Scalable family to cover car networks, interiors and car body applications with Security and ISO CAN-FD

Professional Tools and Software Offer

- Enabled by an extensive support ecosystem for tools and software

Internal Manufacturing

- More than 200 part numbers Available

Zero ppm target

- More than 150M parts shipped

Performance

- SPC5

General Purpose

- Braking
- EV’s
- Engine Management
- Transmission
- RADAR
- 2 Wheelers

EV’s Battery Managament

- 1st Install Accessories
- Park Pilot & Rear Camera
- Lighting & Body control units
- EV’s Power Converters (DC-DC)
- in-car Gateways

Over-the-air update

Internal Manufacturing

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- High performance General Purpose
- More than 150M parts shipped
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EV’s
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Over-the-air update
Technology Roadmap
Automotive Technology Roadmap

Embedded NVM

1-Transistor NOR Flash

M10 (90 nm)
0.18 \( \mu \text{m}^2 \)
Flash cell

PRODUCTION

M55 (55 nm)
0.135 \( \mu \text{m}^2 \)
Flash cell

PRODUCTION

M40 (40 nm)
0.082 \( \mu \text{m}^2 \)
Flash cell

RAMP-UP

In-house Embedded NVM
Development & Manufacturing in
Advanced 300mm Wafer Fab

Under Development

STMicroelectronics, CMOS Headquarters,
200mm/300mm wafer fabs, Crolles, France
Automotive package roadmap

Yesterday:
- BGA
- Wire bonding

Today:
- QFN
- Exposed
- System in Package
- Metal-Lid
- Higher freq
- Better safety
- Better thermal performance
- Passive integration
- Up to 4Mbyte Flash in 10x10 64Pin
- 7x7 Body- 48Pins
- QFN Dual Row
- More I/Os same size

Roadmap:
- ST leading the way towards smaller, faster and cooler MCU

Efficient
Performance

Small
Pins vs Size
32-bit Automotive MCU Roadmap
### 32-bit Automotive Microcontroller Roadmap

<table>
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<th>CMOSM10… P28…</th>
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<tr>
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<td>Single to Multicore Full Autosar</td>
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<tr>
<td>Safety, Security</td>
<td>ISO26262 ASIL A-D / Fail Operational HSM / SHE+</td>
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<td>Quality and Reliability</td>
<td>Top ranking Zero Defect Strategy</td>
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<td>Manufacturig</td>
<td>Flexible and Independent Manufacturing</td>
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<th>2018</th>
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<tbody>
<tr>
<td>Model</td>
<td>SPC56 (90nm)</td>
<td>SPC57 (55nm)</td>
<td>SPC58 (40nm)</td>
<td>Sxx (28nm)</td>
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</table>

![Silicon technology evolution](image1)

- In Production
- In Design / Qualif
- Conceptual Design
32-bit Automotive MCU Roadmap

Full roadmap view

Extended functionality and increased performance
2nd Generation+ products recommended for new designs
General Purpose - Body & Gateway
32-bit MCUs Roadmap
32-bit Automotive MCU Roadmap

General purpose / body and gateway roadmap view

Extended functionality and increased performance
2nd Generation+ products recommended for new designs

1st Generation

2nd Generation

Bolero
- 120MHz, z0
- QFP176/208
- Bolero
- 64MHz, z0
- QFP100/144/176
- Bolero B
- 64MHz, z0
- QFP64/100/144
- Bolero D
- 64MHz, z0
- QFP64/100

Chorus
- 200MHz, 3x z4
- QFP144/176
- BGA292
- Chorus
- 180MHz, 3x z4
- QFP144/176
- BGA292
- Chorus
- 180MHz, 2x z4
- QFP64/100/144/176
- BGA292
- Chorus
- 120MHz, z4
- QFP64/100/144/176
- Chorus
- 80MHz, z2
- QFP64/100

Resources & Performance

General Purpose, Body & Gateway MCU

HW Security

Concept
Design
Sampling
Qualified

ASIL D
ASIL D
ASIL B
ASIL B
ASIL D
ASIL B
ASIL B
Bolero Family
Product Roadmap – B, C, D lines

**Body Access**

**SPC560D**
- e200z0h core (48MHz)
- 256KB Flash w/ ECC
- 4x16KB Data Flash (RWW) w/ ECC
- 16KB SRAM
- 1x CAN
- 3x LINFlex
- 2x SPI
- 1x 12-bit ADC (S&H)

**SPC560D40**
- 256K Flash 16KRam

**SPC560D30**
- 128K Flash 12KRam

**Bolero - SPC560B**
- e200z0h core (64MHz)
- 1.5MB Flash w/ ECC
- 4x16KB Data Flash (RWW) w/ ECC
- 96KB SRAM w/ ECC
- 6x CAN, 10x LINFlex
- 6x SPI, 1x PCI
- 1x 10-bit, 1x 12-bit ADC (S&H)

**SPC560B64**
- 1.5MB Flash 96KRam

**SPC560B60**
- 1MB Flash 80KRam

**SPC560B54**
- 768KFlash 64KRam

**Bolero(B)&Gateway(C)**

**SPC560B/C50**
- 512K Flash 32/48KRam

**SPC560B/C40**
- 256K Flash 24/32KRam

**SPC560B/C60**
- 256K Flash 24/32KRam

**SPC560B/C70**
- 512K Flash 32/48KRam

**Bolero(B)&Gateway(C)**

**SPC560B/C**
- e200z0h core (64MHz)
- 512KB Flash w/ ECC
- 4x16KB Data Flash (RWW) w/ ECC
- 48KB SRAM w/ ECC
- 6x CAN, 4x LINFlex
- 3x SPI, 1x PCI
- 1x 10-bit ADC (S&H)

**SPC560B/C64**
- 1.5MB Flash 128KRam

**SPC560B/C60**
- 1MB Flash 80KRam

**SPC560B/C54**
- 768KFlash 64KRam

**Bolero(B)&Gateway(C)**

**SPC560B/EC**
- e200z4d core (120MHz)
- e200z0h as second core (80MHz)
- 3MB Flash w/ ECC
- 4x16KB Data Flash (RWW) w/ ECC
- 256KB SRAM
- 1x 10-bit, 1x 12-bit ADC (S&H)
- 6x FlexCAN, 10x LINFlex
- FlexRay
- Ethernet
- Cryptographic Services Engine (CSE)

**SPC560EC74**
- 3MB Flash 256KRam

**SPC560EC70**
- 2MB Flash 256KRam

**SPC560EC64**
- 1.5MB Flash 192KRam
Chorus Family

Product Roadmap

SPC584B70
- 3x z4 core @120MHz
- 64K data flash
- COM: 8 / 14 / 1 / 0 / 7
- HSM (Evita Medium)
- ASIL-B
- QFP64 / 100 / 144 / 176

SPC584B70
- 2M Flash / 192K RAM

SPC584B60
- 2x z4 core @180MHz
- 128K data flash
- COM: 8 / 18 / 1 / 1 / 8
- HSM (Evita Medium)
- ASIL-B
- QFP64 / 100 / 144 / 176
- BGA292

SPC584B60
- 1M Flash / 160K RAM

SPC584B60
- 1M Flash / 128K RAM

SPC584EC80
- 3x z4 core @200MHz
- 256K data flash
- COM: 12 / 28 / 2 / 1 / 10
- Gigabit Ethernet
- OTA (flash context switch)
- eMMC / HyperFlash
- USB (no PHY)
- HSM (Evita Full)
- ASIL-D
- QFP144 / 176 / BGA292
- BGA292 / 376

SPC584EC80
- 4M Flash / 512K RAM

SPC584EC74
- 3M Flash / 416K RAM

SPC584EC70
- 2M Flash / 320K RAM

SPC58NH92
- 8M Flash / 1MRAM

SPC58NH90
- 8M Flash / 1MRAM

SPC58NH84
- 6M Flash / 768K RAM

SPC58EC80
- 6M Flash / 768K RAM

SPC58NG84
- 6M Flash / 768K RAM

SPC58NG84
- 4M Flash /

SPC58NH92
- 10M Flash / 1,28MRAM

SPC584EC80
- 4M Flash / 512K RAM

SPC584EC70
- 3M Flash / 416K RAM

SPC5858NG84
- 6M Flash / 768K RAM

SPC584B60
- 2M Flash / 192K RAM

SPC582B60
- 3x z4 core @200MHz
- 256K data flash
- COM: 12 / 28 / 2 / 1 / 10
- Gigabit Ethernet
- OTA (flash context switch)
- eMMC / HyperFlash
- USB (no PHY)
- HSM (Evita Full)
- ASIL-D
- QFP144 / 176 / BGA292
- BGA292 / 376

SPC582B60
- 2M Flash / 192K RAM

SPC582B54
- 768K Flash / 80K RAM

SPC582B50
- 512K Flash / 64K RAM
Chorus family designed in more than 50% of new gateway generation

Advanced in-car networking

Gateway MCU

eMMC 1Gbyte

Gateway + OTA storage MCU

Vehicle Software Update over-the-air FOTA

Body Units

Networking

Package Options

Scalability

BGA292/376 eQFP64-176 QFN48

Single, dual and triple cores
Up to 200MHz operation
Memory from 512Kbyte to 10Mbyte

Security & Safety

Evita Medium/Full

ISO 26262

ASIL-B / ASIL-D
• Embedded Memory and performance
  • up to 10M flash / 1.28MRAM
  • Single core, dual core and triple core platform up to 200MHz
  • Data and instruction cache as well as local data RAM to avoid waitstates at max freq.

• Rich set of automotive network protocols
  • Up to 12x CAN with ISO CAN FD
  • 2x Ethernet 10/100Mb/1Giga bit/s
  • FlexRay dual channel
  • Up to x 28 LIN interfaces

• Peripherals
  • eMIOS timer with 96ch combined with Cross Triggering Unit
  • ADC: 4x 12-bit / 1x 12-bit supervisor / 1x 10-bit Standby
  • Up to 10 SPI

• Miscellaneous
  • Security: HSM up to Evita Full
  • FOTA: Flash context switching
  • External memory interface: eMMC, HyperFlash, Fast SPI
Chorus provides extended scalability within the family by offering

- Wide range of packages from QFN48 to eTQFP176 and BGA376
- Compatible pinout from 512kB Flash up to 10MB Flash devices
- Aligned cores and platform architecture
- Common peripherals set and memory mapping

Easy migration path from Bolero products

- Reuse of well adopted Bolero peripherals like eMIOS/CTU, LINFlex, DSPI
- Maintained Low Power concept with the Mode Entry and Standby domain
- Extended standby capability with the Smart Standby Unit for autonomous Contact Monitoring handling

Development and Programming Tools

- Compiler, debugger and programmers can be reused
- 2-pin JTAG supported with backwards compatibility in 5-pin mode as for Bolero
**Core**
- 80 MHz Power Architecture™
  ISA e200z2 Core (VLE)
  - Single Issue Core with Floating Point Unit

**Memory**
- 1M byte RWW Flash with ECC
- 4x16k Data Flash with ECC
- 96k RAM with ECC

**I/O**
- 7 x MCAN / ISO CAN-FD
- 6 x LINFlex
- 4 x DSPI
- 1 x I2C
- 1x 32ch eMIOS
- 32ch CTU (Cross Triggering Unit)
- 32 channel ADC
  - 1x 12-bit ADC

**System**
- FM-PLL
- MPU
- 16 Channel eDMA Controller
- 2 x CRC Unit
- Fault Collection & Control Unit
- 8 x PIT / 1x STM / 1x RTC/API
- Nexus IEEE-ISTO 5001-2010 Class 2+

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**Block Diagram (superset)**

- **Available**
- **Crossbar Switch**
- **Memory Protection Unit**
- **Debug**
- **JTAG**
- **Nexus**
- **IEEE-ISTO 5001-2010**

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**System Platform**

<table>
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<tr>
<th>Description</th>
<th>Value</th>
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<tbody>
<tr>
<td>Freq. max.</td>
<td>80MHz</td>
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<tr>
<td>Voltage</td>
<td>5V / 3.3V</td>
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<tr>
<td>Temp.</td>
<td>-40 / +125°C</td>
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<tr>
<td>ASIL</td>
<td>B</td>
</tr>
<tr>
<td>I/O</td>
<td>80</td>
</tr>
<tr>
<td>Package</td>
<td>48 / 64 / 100</td>
</tr>
</tbody>
</table>

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**I/O**
- 7 x MCAN / ISO CAN-FD
- 6 x LINFlex
- 4 x DSPI
- 1 x I2C
- 1x 32ch eMIOS
- 32ch CTU (Cross Triggering Unit)
- 32 channel ADC
  - 1x 12-bit ADC

---

**Memory**
- 1M byte RWW Flash with ECC
- 4x16k Data Flash with ECC
- 96k RAM with ECC

---

**System**
- FM-PLL
- MPU
- 16 Channel eDMA Controller
- 2 x CRC Unit
- Fault Collection & Control Unit
- 8 x PIT / 1x STM / 1x RTC/API
- Nexus IEEE-ISTO 5001-2010 Class 2+
Core
- 120 MHz Power Architecture™ ISA e200z4 Core (VLE)
- Dual Issue Core with Floating Point Unit
- 8k-Instruction Cache, 4k-Data Cache
- 64k Local d-RAM

I/O
- 8 x MCAN / FD-CAN
- 14 x LINFlex
- 1 x Ethernet (100Mb/s, time stamping, AVB, IPv4 Checksum)
- 7 x DSPI
- 1 x I2C
- 2x 32ch eMIOS
- 64ch CTU (Cross Triggering Unit)
- 64 channel ADC
  - 1x 12-bit ADC
  - 1x 12-bit ADC Supervisor

Memory
- 2M byte RWW Flash with ECC
- 4x16k Data Flash with ECC
- 192K RAM (128k SRAM, 64k Local d-RAM) with ECC

System
- SSWU (Smart Standby Wake-up)
- Security Module: HSM (Evita Medium)
- FM-PLL
- MPU
- 32 Channel eDMA Controller
- 2 x CRC Unit
- Fault Collection & Control Unit
- 6 x PIT / 1x STM / 1x RTC/API
- Nexus IEEE-ISTO 5001-2010 Class 3+

Design

Freq. max | Voltage | Temp. | ASIL | I/O | Package
--------|--------|------|------|-----|------
120MHz   | 5V / 3.3V | -40 / +125°C | B    | 150 | 64/100/144/176
Core
- 180MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Dual Issue Core with Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 64k Local d-RAM
- 180MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Dual Issue Core with Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 64k Local d-RAM

Memory
- 4M byte RWW Flash with ECC
- 4x32k Data Flash with ECC
- 512k RAM (384k SRAM, 2x 64k Local d-RAM) with ECC

I/O
- 8 x MCAN / FD-CAN
- 18 x LINFlex
- 1 x Ethernet (100Mb/s, time stamping, AVB, IPv4 Checksum)
- Dual Channel FlexRay (10MB/s, 128 buffers)
- 8 x DSPI, 1 x I2C
  2x 32ch eMIOS
- 64ch CTU (Cross Triggering Unit)
- 95 channel ADC
  - 3x 12-bit ADC
  - 1x 12-bit ADC Supervisor
  - 1x 10-bit Standby ADC

System
- SSWU (Smart Standby Wake-up)
- Security Module: HSM (Evita Medium)
- FM-PLL
- MPU
- 64 Channel eDMA Controller
- 2 x CRC Unit
- Fault Collection & Control Unit (incl. error pin)
- 8x PIT / 1x STM / 1x RTC/API
- Nexus IEEE-ISTO 5001-2010 Class 3+
Chorus 6M SPC58 NG84
Block Diagram (superset)

Core
- 180MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 16k Local i-RAM, 64k Local d-RAM
  - Lock Step (optional)
- 180MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 16k Local i-RAM, 64k Local d-RAM
- 180MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Floating Point Unit & LSP(DSP)
  - 16k Local i-RAM, 32k Local d-RAM

Memory
- 6M byte RWW Flash with ECC
  - 4x64k Data Flash with ECC
  - 768kRAM (608k SRAM + 160k d-RAM) with ECC
  - Including 256k Standby

I/O
- 8 x MCAN / FD-CAN
- 18 x LINFlex
- 2 x Ethernet (100Mb/s, time stamping, AVB, IPv4 Checksum)
- Dual Channel FlexRay (10MB/s, 128 buffers)
- 10 x DSPI, 1 x I2C
- 2x 32ch eMIOS
- 64ch CTU (Cross Triggering Unit)
- 86 channel ADC
  - 4x 12-bit ADC
  - 1x 12-bit ADC Supervisor
  - 1x 10-bit Standby ADC

System
- SSWU (Smart Standby Wake-up)
- Security Module: HSM (Evita Medium)
- FM-PLL
- MPU
- 64 Channel eDMA Controller
- 2 x CRC Unit
- Fault Collection & Control Unit (incl. error pin)
- 8 x PIT / 1x STM / 1x RTC/API
- 1x LFAST (Interprocessor bus)
- Nexus IEEE-ISTO 5001-2010
  - Class 3+ (Aurora interface)

<table>
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<th>Freq. max</th>
<th>Voltage</th>
<th>Temp.</th>
<th>ASIL</th>
<th>I/O</th>
<th>Package</th>
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</table>
## 32-bit Automotive MCU Roadmap

### High Performance - Safety Critical MCUs

#### Resources & Performance

- **Andorra**
  - 150MHz, z4
  - 4MB, 3MB, 2MB, 1MB
  - QFP176/BGA324

- **Leopard**
  - 120MHz, 2x z4
  - 16MB, 1.5MB, 1MB
  - QFP100/144

- **Monaco**
  - 80MHz, z3
  - 1MB
  - QFP144/176

- **Pictus**
  - 64MHz, 2x z0
  - 1MB
  - QFP100/144

- **Sphaero**
  - 140MHz, z4
  - 4MB, 1.5MB
  - QFP80/100

- **Bernina**
  - 200MHz, 3x z4
  - 6MB, 4MB
  - QFP176/BGA292 KGD

- **Eiger**
  - 180MHz, 3 x z4
  - 2MB
  - QFP176/BGA292 KGD

- **Lavaredo**
  - 80MHz, z2
  - 1.5MB
  - QFP80/100

- **Velvety**
  - 80MHz, z0
  - 512k, 256k
  - QFP64/100

### 1st Generation

- **Pictus**
  - 64MHz, z0
  - 512k, 376k, 192k
  - QFP64/100/144

### 2nd Generation

- **Andorra**
  - 150MHz, z4
  - 4MB, 3MB, 2MB, 1MB
  - QFP176/BGA324

- **Leopard**
  - 120MHz, 2x z4
  - 16MB, 1.5MB, 1MB
  - QFP100/144

- **Monaco**
  - 80MHz, z3
  - 1MB
  - QFP144/176

- **Pictus**
  - 64MHz, 2x z0
  - 1MB
  - QFP100/144

- **Sphaero**
  - 140MHz, z4
  - 4MB, 1.5MB
  - QFP80/100

- **Bernina**
  - 200MHz, 3x z4
  - 6MB, 4MB
  - QFP176/BGA292 KGD

- **Eiger**
  - 180MHz, 3 x z4
  - 2MB
  - QFP176/BGA292 KGD

- **Lavaredo**
  - 80MHz, z2
  - 1.5MB
  - QFP80/100

- **Velvety**
  - 80MHz, z0
  - 512k, 256k
  - QFP64/100

**Extended functionality and increased performance**

**2nd Generation+ products recommended for new designs**
# High Performance - Safety Critical MCUs

Product Roadmap – P, L lines

## Pictus - SPC560P
- up to 64 MHz Power Architecture
- e200z0h core
- 512KB Program Flash with ECC
- 4x16KB EEPROM Flash with ECC
- 40KB SRAM with ECC
- 2 x CAN
- 1 x FlexRay
- 2 x LINFlex
- 4 x SPI
- 2 x 10-bit ADC (S&H)

- **SPC560P50**
  - 512KFlash / 40KRam
- **SPC560P44**
  - 384KFlash / 40KRam
- **SPC560P40**
  - 256KFlash / 20KRam
- **SPC560P34**
  - 192KFlash / 20KRam

## Pictus - SPC56AP/0P
- up to 64 MHz Power Architecture
- Single and Dual e200z0h core
- 1MB Program Flash with ECC
- 4x16KB EEPROM Flash with ECC
- 80KB SRAM with ECC
- 3 x CAN
- 1 x FlexRay
- 2 x LINFlex, 5 x SPI
- 2x 10-bit ADC (S&H)

- **SPC560P60**
  - 1MFlash / 80KRam
- **SPC560P54**
  - 768KFlash / 64KRam
- **SPC56AP60**
  - 1MFlash / 80KRam
- **SPC56AP54**
  - 768KFlash / 64KRam

## Leopard - SPC56EL/4L
- up to 120MHz Power Architecture
- Single (4L) and Dual (EL) e200z4d core
- Lock Step and Decoupled Parallel modes
- 2MB RWW Flash with ECC
- 192KB SRAM with ECC
- EE emulation
- 3 x CAN, 1 x FlexRay, 2 x LINFlex, 3 x SPI
- 2 x 12-bit ADC (S&H)

- **SPC564L70**
  - 2MFlash / 192KRam
- **SPC56EL70**
  - 2MFlash / 192KRam
- **SPC564L60**
  - 1MFlash / 128KRam
- **SPC56EL60**
  - 1MFlash / 128KRam
- **SPC564L54**
  - 768kFlash / 96KRam
- **SPC56EL54**
  - 768kFlash / 96KRam

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<table>
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<tr>
<th>LQFP64 / LQFP100</th>
<th>LQFP100 / LQFP144</th>
<th>LQFP100 / LQFP144</th>
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# High Performance - Safety Critical MCUs

## Product Roadmap – M, A lines

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<th>Family</th>
<th>Code</th>
<th>Flash (K)</th>
<th>SRAM (K)</th>
<th>Features</th>
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<tr>
<td><strong>Monaco - SPC563M</strong></td>
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</tr>
</tbody>
</table>
| SPC563M64 | 1.5M | 94 | | e200z3 core (80MHz)  
1.5MB RWW Flash with ECC  
111KB SRAM with ECC  
2x CAN  
2x SCI  
2x SPI  
2x 12-bit ADC (S&H) |
| SPC563M60 | 1M | 64 | | e200z4d core (150MHz)  
209KB SRAM with ECC  
3x CAN  
3x SCI  
3x SPI  
2x 12-bit ADC (S&H) |
| **Andorra - SPC564A** | | | | |
| SPC564A80 | 4M | 192 | 17 | e200z4d core (150MHz)  
4MB RWW Flash with ECC  
209KB SRAM with ECC  
3x CAN  
3x SCI  
3x SPI  
2x 12-bit ADC (S&H) |
| SPC564A74 | 3M | 160 | 17 | e200z4d core (150MHz)  
4MB RWW Flash with ECC  
209KB SRAM with ECC  
3x CAN  
3x SCI  
3x SPI  
2x 12-bit ADC (S&H) |
| SPC564A70 | 2M | 128 | 17 | e200z4d core (150MHz)  
4MB RWW Flash with ECC  
209KB SRAM with ECC  
3x CAN  
3x SCI  
3x SPI  
2x 12-bit ADC (S&H) |
Velvety – 0.5M SPC570S50
Superset Block Diagram

- **Core**
  - Up to 80 MHz Power Architecture™ ISA e200z0 Core (VLE)
  - ASILD SEooC

- **I/O**
  - 2x FlexCAN with 32MB
  - 2x LINFlex
  - 3x DSPI
  - 4x eTimer (6ch each)
  - ADC – 1+1 x 12Bit, up to 16Ch.
    - fast 10Bit conversion & supervisor ADC concept
  - 1x ADC cross triggering unit (CTU)

- **Memory**
  - 512k byte Flash with ECC
  - 4x8k Data Flash with ECC (1 RWW partition)
  - 48k SRAM with ECC
  - Crossbar with MPU (8 regions) w. process ID support

- **System**
  - 16ch eDMA (lockstep)
  - CRC Unit (2Ch.)
  - Fault Collection & Control Unit
  - Software watchdog timer (inc. window mode, flow monitoring)
  - Temperature Sensor
  - 3.3V or 5V single supply
  - FM-PLL and 16MHz internal RC OSC
  - Nexus Class 3 / JTAG (2 pin or 5 pin) / Trace Port (4MDO)
  - 64/100 pins LQFP package ePAD
  - -40°C - + 150°C TJ / 165°C Tj

**Diagram Details**
- Debug JTAG Nexus
- Power Architecture™ e200z0 VLE
- Crossbar Switch
- Memory Protection Unit
- MEMU FMPLL IRC
- Periph. Bridge
- 48K SRAM 512K FLASH
- Periph. Bridge
- 1* LinFlex 1* DSPI
- 1* FlexCAN
- 2* DSPI 1* LinFlex 1* FlexCAN
- 1* ADC
- 2* Timer 2* Timer
- 1* ADC
- 1* LinFlex 1* DSPI
- System / Platform
- Product / Application Specific
- Memory
- Connectivity
**Core**
- Up to 140 MHz Power Architecture™ ISA e200z4 Core (VLE)
- Dual Issue Core with Floating Point Unit
- 12k Cache (8k-Instruction Cache, 4k-Data Cache)
- 32k TCM (32k d-RAM)
- ASILD SEooC

**I/O**
- 1 x FlexRay Dual Channel with 128MB (optional)
- 3x ISO CAN FD
- 4 x LINFlex (3x master only)
- 4 x DSPi
- 2 x SENT (2x3ch overall)
- 2 x FlexPWM (4x3ch each) + 2 x FlexPWM (2ch each)
- 4 x eTimer (6ch each)
- ADC – 2x (3+1)x 12Bit, 18/32/33Ch. (on QFP100/144/BGA)
  - fast 10Bit conversion & supervisor ADC concept
- 2 x ADC enh’d cross triggering unit (eCTU)

**Memory**
- 1.5M byte + 4x16k Flash with ECC (1 RWW)
- 128k RAM with ECC (96k SRAM + TCM)
- Crossbar with MPU (16 regions)

**System**
- 16Ch eDMA
- CRC Unit
- Fault Collection & Control Unit
- Software watchdog timer (inc. window mode, flow monitoring)
- 3.3V or 5V advanced supply (internal or external logic supply)
- FM-PLL, FlexRay PLL and 16MHz internal RC OSC
- Nexus Class 3+ / JTAG (2 pin or 5 pin)
- 100-144 pins LQFP package (0.5mm pitch)
- -40°C - + 150°C Tj
Lavaredo – 1.5M SPC572L64
Superset Block Diagram

Core
• 80 MHz Power Architecture™ ISA e200z2 Core (VLE)
• Floating Point Unit & LSP(DSP)

Memory
• 1.5M byte RWW Flash with ECC
  • +2x16k Data Flash with ECC
• 64k RAM with ECC
  • +19k SRAM on Timer Module
  • +8k Overlay RAM

I/O
• Generic Timer Module (Mid-End Version)
  • 16 Inputs, 56 Outputs
• 2 x M-CAN
• 3 x LINFlex, 2 x DSPI including 1 x µSB
• 1 x Ethernet
• 4 x SENT
• 24 channel ADC
  • 3 SAR ADC, 12-bit, TUE ±4LSB
  • 1 σ-Δ ADC with OSR x32-64
  • Decimation filters (4th ord. IIR or 8th ord. FIR with prog.coeff.)

System
• PLL
• MPU
• 16 Channel eDMA Controller
• 5 x PIT
• 1 x LFAST (Interprocessor bus)
• Nexus Class 3+
• Designed for eTQFP80, eTQFP100
Core
• 160 MHz Power Architecture™ ISA e200z4 Core (VLE)
  • Floating Point Unit
  • 4k-Instruction Cache, 2k-Data Cache
  • 16k Local i-RAM, 64k Local d-RAM
  • 1x Lock Step configuration
• 80 MHz Power Architecture™ ISA e200z2 Core (VLE)
  • Floating Point Unit & LSP(DSP)
  • 16k Local i-RAM, 48k Local d-RAM

Memory
• 2.5M byte RWW Flash with ECC
  • +4x16k Data Flash with ECC
• 176k RAM (64k SRAM, 112k Local d-RAM) with ECC
  • +26k SRAM on Timer Module
  • +16k Overlay RAM

I/O
• Generic Timer Module (Mid-End Version)
  • 24 Inputs, 64 Outputs
• Dual Channel FlexRay (10MB/s), 128 buffers
• 3 x ISO CAN FD
• 4 x LINflex, 5 x DSPI including 2 x µSB
• 1 x Ethernet, 1 x I2C
• 6 x SENT, 2 x PSI5
• 48 channel ADC
  • 5 SAR ADC, 12-bit, TUE ±4LSB
  • 2 Σ-Δ ADC with OSR x32-64

System
• FM-PLL
• MPU
• 32 Channel eDMA Controller
• 2 x CRC Unit
• Fault Collection & Control Unit (incl. error pin)
• 6 x PIT
• 1x LFAST (Interprocessor bus)
• Nexus Class 3+
• EBI only for Calibration (High speed debug interface)
• Designed for eTQFP144, eLQFP176

Superset Block Diagram

- System Platform
- Memory
- Timer
- Peripherals

K2 – 2.5M SPC574K72
Core
- 2x 180 MHz Power Architecture™ ISA e200z4d Core (VLE)
  - Dual Issue Core with Floating Point Unit
  - 2x (8k-Instruction Cache, 4k-Data Cache)
  - 2x (16k Local i-RAM, 64k Local d-RAM)
  - 1x Lock Step configuration
- 180 MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Dual Issue Core with Floating Point Unit & LSP(DSP)
  - 8k-Instruction Cache
  - 16k Local i-RAM, 32k Local d-RAM

Memory
- 6M byte RWW Flash with ECC
  - +4x64k+2x16k Data Flash with ECC
- 768k RAM (608k SRAM, 160k Local d-RAM) with ECC
  - +61k SRAM on Timer Module
  - +32k Overlay RAM

I/O
- Generic Timer Module (High-End Version)
  - Dual Channel FlexRay (10MB/s), 128 buffers
  - 7 x (FD)M-CAN, 1 x (FD)M-TTCAN
  - 18 x LINFlex, 10 x DSPI including 2 x μSB
  - 2 x Ethernet, 1 x I2C
  - 15 x SENT, 2 x PSI5, 1 x PSI5-S
- 86 channel ADC
  - 5 SAR ADC, 12-bit, 1.5us conversion time, TUE ±4LSB
  - 3 SAR ADC, 10-bit, 1us conversion time, TUE ±2LSB
  - 6 Σ-Δ ADC with OSR x32-64

System
- Security Module (HSM)
- FM-PLL
- MPU
- AMU
- 96 Channel eDMA Controller
- 2 x CRC Unit
- Fault Collection & Control Unit (incl. error pin)
- 8 x PIT
- 1x LFAST (Interprocessor bus)
- Nexus Class 3+
- EBI only for Calibration (High speed debug interface)
- Designed for eLQFP176, LFBGA292 and KGD
Please find more SPC5 information from ST Website

http://www.st.com/spc5