48V Direct Conversion to CPU, Memory or ASIC

High efficiency (ZVS, ZCS), fully isolated, scalable and energy proportional
Innovative Resonant Current Doubler Architecture for 48V to PoL Direct Conversion Addressing Data Center Power Needs

- Fully Isolated, Scalable, Maximized Flat Efficiency (ZVS, ZCS), Energy Proportional Able to Support Any Load (DDR, GPU, ASIC)
- Fully Compliant to Intel and Other Brand CPUs
- Flexible Architecture Extendable to Direct Conversion from 400V Bus Ideal for Module Based Solutions
- Available in Mass Production Since 2016
Data Center Power Challenges

High Energy Consumption Increases Need for Efficiencies and Direct Conversion from 48V

• Data Center Energy Consumption *(US Department of Energy Study)*
  • US data centers consumed about 70 billion kilowatt-hours of electricity in 2014
  • Total US data center energy consumption to grow by 4 percent between now and 2020
  • Efficiency improvements played an enormous role in taming the growth rate of the data center industry’s energy consumption.
  • If stayed at efficiency levels of 2010, data centers would have consumed close to 40 billion kWh more than they did in 2014

• Higher Power Needed by Silicon Key Components
  • CPU power demand going above 240W
  • GPU and Networking ASICs power demand above 350W
  • DDR power increase due to faster memory and higher number of DIMMs

• More Efficient Data Center and Power Architectures are Needed
Power Distribution Overview

- **12V IBA from AC Line**
- **12V IBA from 48V Line**
- **48V Direct Conversion**

### 48V Direct Conversion Advantages

- 48V distribution current is 1/4th compared to 12V with distribution losses reduced to 1/16th
- Better conversion efficiency (downstream and upstream)
- High Power Boost converter not required
- Simpler distributed BBS maximizing server density
- Leverage of existing Telecom infrastructure
New Architecture: Resonant Current Doubler

**Needed For Resonant Architecture**

**Needed For Isolated Architecture**

<table>
<thead>
<tr>
<th>Cell</th>
<th>Digital Controller</th>
<th>Synchronous Driver</th>
<th>Full Bridge Driver</th>
<th>Digital Isolator</th>
</tr>
</thead>
</table>

**STRG06**  
Multiphase Resonant Constant On Time Digital Controller 6 interleaved Cells (automatically turned on/off by load request) with PMBUS

**STRG04**  
100V Full Bridge Driver with programmable predictive control for zero voltage operations in constant phase shift control

**STRG02**  
Single wire controlled Synchronous Rectifier able to zero voltage and zero current operations
Architecture Scalability

More Power → More Cells

- Design Only One Cell to Design a Flexible System
- Support up to 6 Cells
- Automatic Interleaving Among Cells
- Automatic Cell Turn on/off Management
- Active Current Balancing Among Cells
- Pulse Skipping Mode When in Single Cell
Architecture Key Advantages

- Fully Isolated, Resonant or Non-Resonant Direct Conversion
  - $54V \rightarrow V_{\text{CORE}}(1.xV), V_{\text{DDR}}(1.2V), V_{\text{SOC}}(0.8V), V_{\text{IBC}}(12V, 5V, 3.3V)$

- Maximum Efficiency Across Full Load Range
  - ZVS and ZCS under any working conditions
  - Energy Proportional Management $\rightarrow$ Dynamic Cell Management, Pulse Skipping
  - No Heat Sink Required
  - OpEx savings enhances system and datacenter performance/watt

- Scalable and Flexible
  - Converter Cells are paralleled and interleaved
  - System scalability according to the load power demand
  - Variable Frequency in CCM and DCM
  - Instantaneous turn-on of resonant converters when load increases
  - Resonant or Non-Resonant Mode of Operations

- Any Digital Load (CPU, GPU, DDR, ASICs)
  - High Bandwidth to sustain CPUs' load transient
  - Easy to design and to compensate like a Buck converter
  - Up and down reference transitions $\rightarrow$ Sink mode operations
  - Minimized noise content for closer proximity to Digital Loads

- High Power Density and Telemetry (PMBus™, AVS1.3)
STRG0X Part Number & Main Features

High performance Resonant Digital control loop RVCOTTM
- Drives up to 6 Cells with STRG02 and STRG04, from 50 W up to >300 W
- Compliant with Intel VR12.5 and VR13 protocol
- Fully configurable through PMBus™ rev1.3
- Advanced Power Management
  - Auto Cell Shedding with PFM
- Programmable Protections
  - OV / UV and FB Disconnection
  - Pos/Neg OC per Cell
  - Current Sharing Error
  - Black Box Recorder (BBR)
  - Catastrophic Fault Precursor (CFP)
- Embedded Non-Volatile Memory (NVM)
- Primary uC interface for telemetry (PuC)
- Single-wire Synchronous Rectifier Drive
- RST and EN1V8 for Low Power Mode
- VFQFPN68, 8x8mm Package

60V Full-Bridge driver for N-Channel MOSFETs
- Adjustable dead-time control
- 2 A Sink/Source Current
- Operating Frequency up to 1 MHz
- Enable Input
- Programmable Over Current Protection
- VFQFPN, 4x4mm Package

Dual Low-Side Driver for N-Channel MOSFETs
- 4 A Sink/Source Current
- Operating Frequency up to 1 MHz
- Predictive ZCS / ZVS Control
- High-Impedance Control
- START Input
- DFN12, 3x3mm Package
The specifications view
The actual view
A full set of analysis diagrams
Reference Designs

Same Scalable Topology for Different Point of Load -- Ideal for Power Module Applications

<table>
<thead>
<tr>
<th>Conversion Type</th>
<th>Application</th>
<th>Output Current and Power</th>
<th>Number of Cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>54V → 1.8V</td>
<td>Intel VR13 CPU</td>
<td>165W TDC 360W Peak</td>
<td>4</td>
</tr>
<tr>
<td>54V → 1.2V</td>
<td>VDDQ DDR3/4</td>
<td>120A - 150W</td>
<td>2</td>
</tr>
<tr>
<td>54V → 0.9V</td>
<td>ASIC Core</td>
<td>300A - 270W</td>
<td>6</td>
</tr>
<tr>
<td>54V → 12V</td>
<td>Point of Load</td>
<td>42A - 500W</td>
<td>1</td>
</tr>
<tr>
<td>54V → 1V</td>
<td>Point of Load</td>
<td>80A - 80W</td>
<td>1</td>
</tr>
<tr>
<td>54V → 3.3V</td>
<td>Point of Load</td>
<td>46A - 150W</td>
<td>1</td>
</tr>
</tbody>
</table>
DDR Reference Designs

Featuring:
- Transformer: Payton N=9
- Lout: Eaton FP1008R1R220
- 6x SecMOS / cell
- Isolated architecture
- 2 cells + VR Cout, VPP, VTT included in 5x5cm area
- Optional 3rd cell (currently not used)
DDR Board Dynamic Tests

Intel Gen4 VR Test Tool TP11 drives the control signals

Current transient specification
- 64.28A * 0.025V/A = 1.607V --> 0x128E
- 15.22A * 0.025V/A = 0.380 --> 0x495
- Rise time = 3570 meas RiseTime = 2.86µs
  (10%-90%) as specified in Intel xls sheet.
- Vout sensed from pin J7-7/8 of worst VRTT DIMM module
DDR Board Dynamic Tests

Test configuration

- Nominal Voltage: 1.2V
- No offset, No load line
- 15A - 65A max transient current, 1Khz, 50% Duty

Undershoot <40mV and Overshoot <<60mV

Excellent margin on dynamic test while keeping best efficiency
Module Approach

• 2 different modules proposal:
  • MAIN: STRG06 embedded, Drivers and Multi-Cell Digital Controller embedded
  • CELLS: Up to 6 Cell with Drivers embedded

• Automatic current sharing between modules

• Automatic synchronization and interleaving between modules

• Dynamic Module management provides flat system efficiency

Pictures taken from ST reference design showing the scalability of the application
Innovative Resonant Current Doubler Architecture for 48V to PoL Direct Conversion Addressing Data Center Power Needs

Fully Isolated, Scalable, Maximized Flat Efficiency (ZVS, ZCS), Energy Proportional Able to Support Any Load (DDR, GPU, ASIC)

Fully Compliant to Intel and Other Brand CPUs

Flexible Architecture Extendable to Direct Conversion from 400V Bus Ideal for Module Based Solutions

Available in Mass Production Since 2016