Digital Control IC for Interleaved PFCs

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Presentation Outline

- PFC Basics
- Interleaved PFC Concept
- Analog Vs Digital Control
- The STNRGPF01 Digital Controller
  - Main Functions
  - Edesign suite GUI
- Application Example:
  - 3kW Three channel Interleaved PFC
  - Performance Evaluation
- Conclusions
Power Factor Correction

A PFC is the input stage of an AC/DC converter connected to the AC mains to address the need to limit energy consumption.

A PFC pre-regulator placed between the bridge and the bulk capacitor draws a quasi-sinusoidal current from the mains, in-phase with the line voltage.

Harmonic current emission is regulated by IEC 61000-3-2. Lighting requirements > 25W, SMPS & chargers > 75W.

Maximize the energy delivery to load means to reduce the Total Harmonic Distortion (THD) and therefore maximize the Power Factor.
**Introduction to PFC**

PF = \( \frac{V_{rms}I_{1rms}\cos\phi}{V_{rms}I_{rms}} = \frac{I_{1rms}}{I_{rms}} \cos\phi = K_d \cos\phi \)

PF = \( K_d \cdot K_\theta \)

K_d = Distortion Factor
K_\theta = Displacement Factor

\[ THD \ (\%) = 100 \times \sqrt{\frac{1}{K_d^2} - 1} \]
Passive vs Active PFC

• PFC stage can be “Passive” or “Active”.
  • **Passive**: bulky capacitors and inductors
  • **Active**: high frequency topologies
Passive PFC Topologies

- **AC side inductor**
- **DC side inductor**
- **SR Bandpass filter**
- **PR Bandstop filter**
- **Harmonic Trap filter**
- **LCD Rectifier**
Active PFC Topologies

- Main topologies for PFC stage:
  - Boost (most used because it’s stepping-up the voltage)
  - Buck
  - Flyback
  - Cuk
  - Sepic

- Operation modes:
  - Continuous Conduction Mode (CCM) > 350W
  - Transition Mode (TM) <350W
  - Discontinuous Conduction Mode (DCM)
## PFC – Control Technique

<table>
<thead>
<tr>
<th>Type</th>
<th>Strengths</th>
<th>Weakness</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Average current control</strong></td>
<td>Low distortion on input current</td>
<td>Two control loops</td>
</tr>
<tr>
<td><strong>Peak Current control</strong></td>
<td>Fast current correction</td>
<td>High distortion on input current</td>
</tr>
<tr>
<td><strong>Hysteresis Current control</strong></td>
<td>Fast current correction Low distortion on input current</td>
<td>Need two comparators</td>
</tr>
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PFC – Interleaved Concept

Diagram showing a PFC controller connected to a DC/DC or DC/AC converter, followed by a load. The diagram includes components such as L1, LN, M1, M_n, I_1, and I_c, illustrating the flow of current through different phases.
Example: 3kW iPFC
Switching frequency 100kHz

Core: EE70
L = 150µH
Size: h=70mm, W=66mm, D=31mm
Volume=8.72 in³

Core: PQ3230
L = 120µH
Size: h=30mm, W=32mm, D=27mm
Volume=1.58 in³
Total Volume=4.74 in³

45% Less!
Output Capacitor Ripple Current Reduction

RMS Current Reduction

Capacitors with higher ESR can be used → Lower cost
Digital vs Analog PFC Control

- Full digital control of PFC is already state of the art.
- More PFC topologies can be implemented
- More sophisticated control algorithms

- Availability of ICs for PFCs from many manufacturers
- Cycle by cycle control loop
- High bandwidth
- Low Cost
The STNRGPF01: Overview

- TSSOP38 Package
- Mixed Signal Control
- Configurable By GUI
The STNRGPF01: Overview

- Semi-digital control
- Analog current controller
- Voltage controller, feed-forward compensation, multiplier, PWM clock generator and non-time critical protection functions are implemented digitally.

- Interleaved boost PFC
- Up to 3 interleaved channels
- CCM, fixed frequency
- Average current control, cycle-by-cycle
- Inrush current control
- Burst mode support
- OCP, OVP and thermal protection
- Soft start-up
- Flexible phase-shedding strategy
STNRGPFO1: Voltage Loop

- Output Voltage Sensing
- Input Voltage Sensing
- Output Current Sensing
- ZVD Sensing

Internal control block scheme
STNRGPF01: Current Loop

Analog Current OP-Amp PI

Internal control block scheme
STNRGPFO1: Driving and Interleaving

Interleaving operation (internal)

- CP32
  - TRIG(CP3): High Level
  - TRIG(CP2): Low Level

- SMED0
  - TRIG: Rising Edge
  - DELAY 1

- SMED1: ON
  - TRIG: Rising Edge
  - DELAY 1

- SMED2: OFF
  - TRIG: Falling Edge
  - DELAY 1

- SMED4: ON
  - TRIG: Rising Edge
  - DELAY 2

- SMED5: OFF
  - TRIG: Falling Edge
  - DELAY 2

Internal control block scheme

PWN GENERATION

- PWM0
  - CLOCK
  - SYNR[1]
  - SET1

- PWM1
  - FLIP-FLOP1
  - RESET1
  - SYNR[2]

- PWM2
  - FLIP-FLOP2
  - RESET2

- INTERLEAVING CHANNEL 1 180° / 120°

- INTERLEAVING CHANNEL 2 240°

STNRGPFO1

CLOCK

ENABLE
STNRGPF01 GUI: eDesign Suite Tool

eDesignSuite smart configurator for STNRGPF01

Binary file generation ➔ BoM + SCHEMATIC ➔ Build
3kW Three Channels Interleaved PFC

The device performance have been evaluated developing a 3kW Three channels PFC.

- Pout = 3kW @ Vin = 230Vac; 1.5kW @ Vin = 110Vac
- Vout = 400V
- PF > 0.98 @ 20% load
- THD < 5% @ 20% load
- CCM with analog current control loop
  (cycle by cycle regulation)
- Input Voltage feed forward

- Load feed forward
- Working frequency = 111kHz per channel
- Thermal protection set at 120°C
- Current protection set at 33A
- Direct fan driving
- Current reference realized by internal map (200 pt)

High Power Density
52W/in³!

Key Products

- STNRGPF01 (Digital controller for PFC)
- PM8834D (Double Channel low side driver)
- ALTAIR05-800 (Off-line primary-sens. switch. reg.)
- STW40N60M2 (MDmesh II Plus low Qg )
- STPSC1206 Schottky silicon carbide diode
- TSV911 (High speed OP)
- LMV358 (Standard OP)
- M74HC132 (Quad NAND Gate)

L=24.5 cm; W=11 cm; H=3.5 cm (including heatsink area)
Experimental Results: Steady State

- Duty cycle
- Inductors current
- PWM master
The load feed forward when load step is applied reduces the over and under voltage of the output dc bus voltage!
Experimental Results: Load Feed Forward

Load step sequence: 0.4kW - 2kW - 0.4kW

The load feed forward when load step is applied reduces the over and under voltage of the output dc bus voltage!
Experimental Results: Load Feed Forward

Load step sequence: 0W - 2kW - 0W

The PFC interrupts the Burst Mode to meet the load requirement and when load is disconnected it returns in Burst Mode.
Experimental Results
Efficiency and ITHD%
Conclusions

• Interleaved PFC benefits include: the use of smaller components, better thermal performance, low current ripple

• The STNRGPF01 is a controller for CCM interleaved PFCs

• It supports up to three independent channels

• Cycle by Cycle current control allows fast dynamic response

• The STNRGPF01 can be easily and quickly configured using the eDesign Suite GUI resulting in reduced development time, lower development cost and faster time-to-market
Thank You!