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Xilinx KU060 power reference board

Xilinx FPGA KU060 – STMicroelectronics Power Management Reference Design:

Power requirements and sequencing

Power Rail	XC Current (A)	XPE XC Conditions
VCCINT	30.8	Utilization: 80% registers, 100% LUTS, 500Mhz clock freq
VCCINT_IO	1.674	71% IO utilization (2x72, 2x32 DDR4 interface at 1800MTs)
VCCBRAM	0.645	80% BRAM utilization
VCCAUX	1.448	71% IO utilization (2x72, 2x32 DDR4 interface at 1800MTs)
VCCAUX_IO	1.107	71 % IO utilization (2x72, 2x32 DDR4 interface at 1800MTs)
MGTVCCAUX_RS	0.091	
MGTVCCAUX_L	0.055	
MGTAVCC_RS	3.604	
MGTAVCC_L	2.163	
MGTAVTT_RS	0.653	
MGTAVTT_L	0.392	32 GTH channels running at 12.5Gb/sec using low power mode
VCCO _48	0.132	
VCCO _47	0.132	
VCCO _46	0.132	
VCCO _45	0.132	
VCCO _44	0.132	71 % IO utilization (2x72, 2x32 DDR4 interface at 1800MTs)
VCCO _68	0.132	
VCCO _67	0.132	
VCCO _66	0.132	
VCCO _65 (HR)	0.150	Estimated number from F-Hing
VCCO _64 (HR)	0.150	
VCCO_25	0.132	71 % IO utilization (2x72, 2x32 DDR4 interface at 1800MTs)
VCCO_24	0.132	

Regulator Supply Requirements

Source	Voltage	Total (A)
V_{CCINT}	0.958	16.525
V_{CCBRAM}	0.962	0.426
V_{CCAUX}	1.822	0.731
V_{CCAUX_IO}	1.820	0.424
V_{CCO} 3.3V	3.327	0.141
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.805	0.141
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
V_{CCO} 1.0V	1.000	
$MGTV_{CCAUX}$	1.809	0.105
$MGTAV_{CC}$	1.013	2.984
$MGTAV_{TT}$	1.210	0.982
-		
-		
-		
-		
V_{CCADC}	1.800	0.020
Total Regulator Power		**23.5W**

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is **VCCINT, VCCBRAM, VCCAUX/VCCAUX_IO**, and **VCCO** to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. **VCCAUX** and **VCCAUX_IO** must be connected together. When the current minimums are met, the device powers on after the VCCINT, VCCBRAM, VCCAUX/VCCAUX_IO,and VCCO supplies have all passed through their power-on reset threshold voltages. **VCCADC and VREF** can be powered at any time and have no power-up sequencing recommendations.

The recommended power-on sequence to achieve minimum current draw for the GTH transceivers is **VCCINT, VMGTAVCC, VMGTAVTT** OR VMGTAVCC, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from VMGTAVTT can be higher than specifications during power-up and power-down.

Groups

Group1: VCCINT, VCCINT_IO & VCCBRAM	1V
Group2: VMGTAVCC	1V
Group3: VMGTAVTT	1.2V
Group4: VCCAUX,VCCAUX_IO & VCCADC	1.8V
Group5: VMGTAVCCAUX	1.8V
Group6: VCCO3.3V	3.3V
Group7: VCCO1.8V	1.8V

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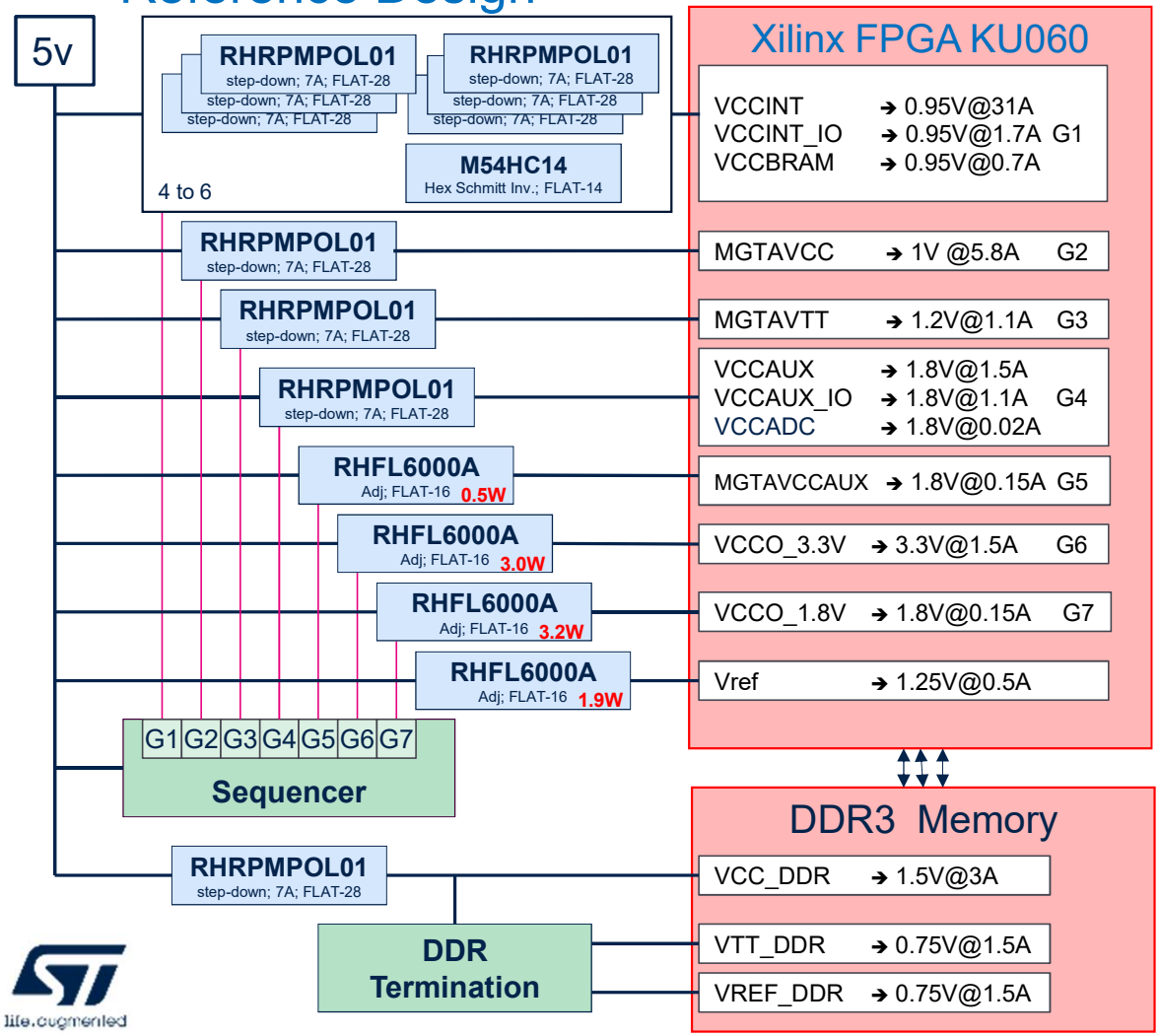
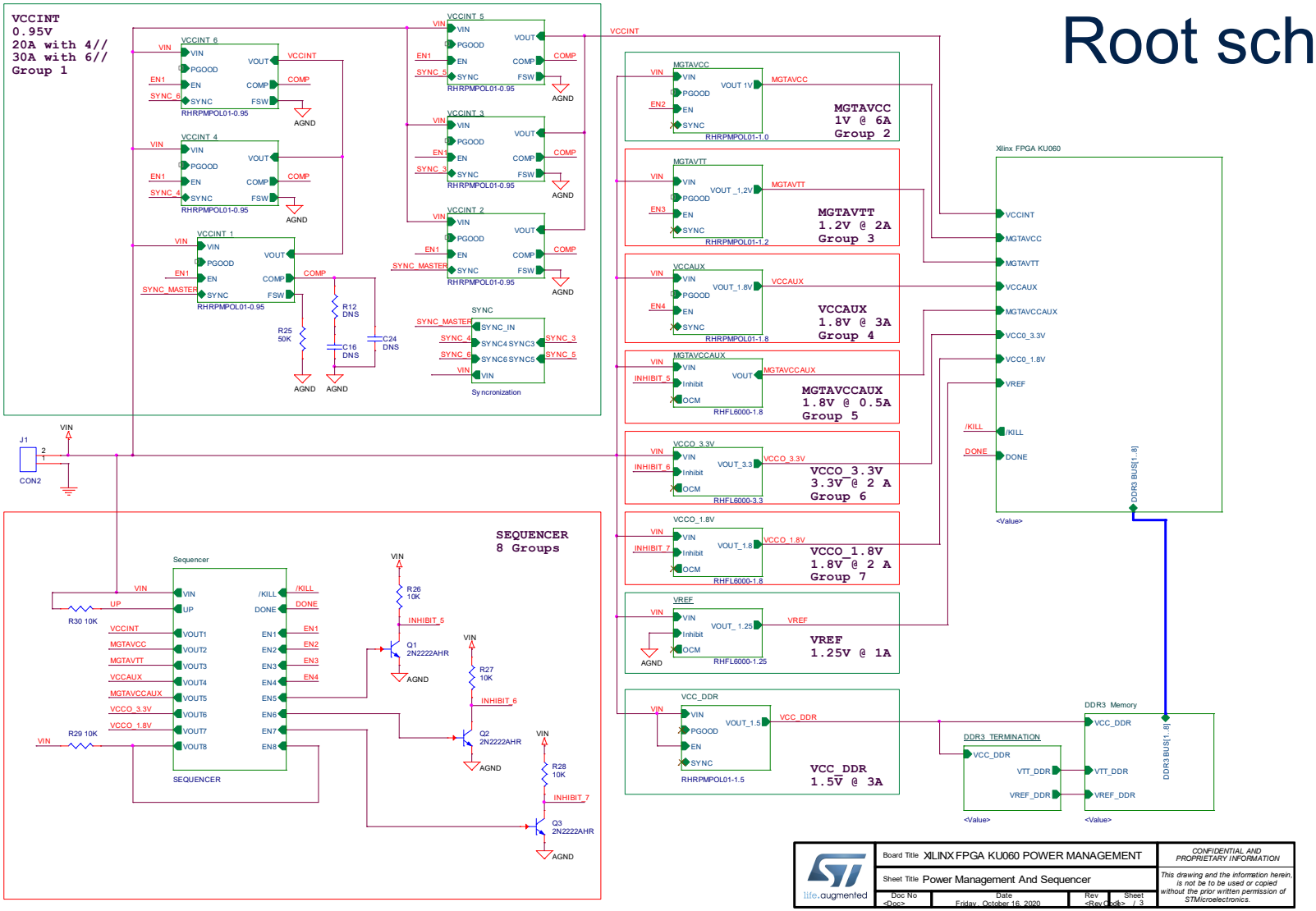


Block diagram

Source	Groups	Vout(V)	Iout(A)	ST Device
V_{CCINT} V_{CCINT_IO} V_{CCBRAM}	1	0.95	34	RHRPMPOL01 x6
			17.5	RHRPMPOL01 x4
$MGTAV_{CC}$	2	1	3 to 5.8	RHRPMPOL01
$MGTAV_{TT}$	3	1.2	1.1	RHRPMPOL01
V_{CCAUX} V_{CCAUX_IO} V_{CCADC}	4	1.8	2.6	RHRPMPOL01
			1.2	RHFL6000A
$MGTV_{CCAUX}$	5	1.8	0.15	RHFL6000A
V_{CCO} 3.3V	6	3.3	1.5	RHFL6000A
V_{CCO} 1.8V	7	1.8	1	RHFL6000A
V_{REF}		1.25	0.5	RHFL6000A
DDR3 Memory				
VCC_DDR	NA	1.5	3	RHRPMPOL01
VTT_DDR	NA	0.75		?
VREF_DDR	NA	0.75		?

Root schematic



life.augmented	Board Title: XILINX FPGA KU060 POWER MANAGEMENT	CONFIDENTIAL AND PROPRIETARY INFORMATION
	Sheet Title: Power Management And Sequencer	This drawing and the information herein, is not be to be used or copied without the prior written permission of STMicroelectronics.
	Doc No: <Doc> / Date: Friday, October 16, 2020 / Rev: <Rev Code> / Sheet: / 3	

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SMD 5962R20208	SAMPLES EM	MASS PROD	QML-V

RHRPMPOL01
7A point of load

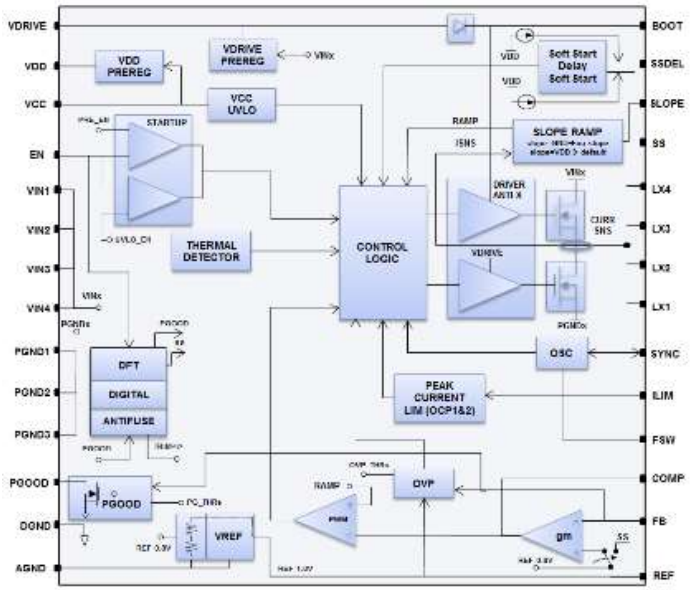
Rad-Hard Point of Load >7A monolithic synchronous step-down regulator

MAIN BENEFITS & FEATURES

- Input operating voltage range: 3.0V to 12V(radiation performance up to 7v)
- Output voltage range: 0.8V to 0.85xVin
- Fast load transient response Peak Current Mode control loop
- Integrated NCH MOSFETs for synchronous step-down conversion
- Integrated BOOT diode
- Input under-voltage protection
- Over voltage protection
- Latched/Re-Triggerable over temperature protection
- Latched/Re-Triggerable 2nd level of current protection
- **Power good output pin**
- Programmable switching frequency: from 100kHz to 1MHz
- **Easy synchronization with 180° out-of-phase (up to 2 ICs)**
- **Current sharing configuration for higher load requirements**
- Adjustable output overcurrent protection
- Programmable soft-start with increased current capability
- OTP circuitry embedded for fine accuracy tuning by trimming
- **FLATPACK-28** Hermetic Package

RADIATION HARDENED

- Total Ionizing Dose: 100 krad
- Tested ELDRS-free
- SEL-free up to 70 MeV/mg/cm2 (@ Vcc up to 7 V)
- SEU-SEFI characterized up to Vcc 7V, Proton Free
- No performance degradation due to SET



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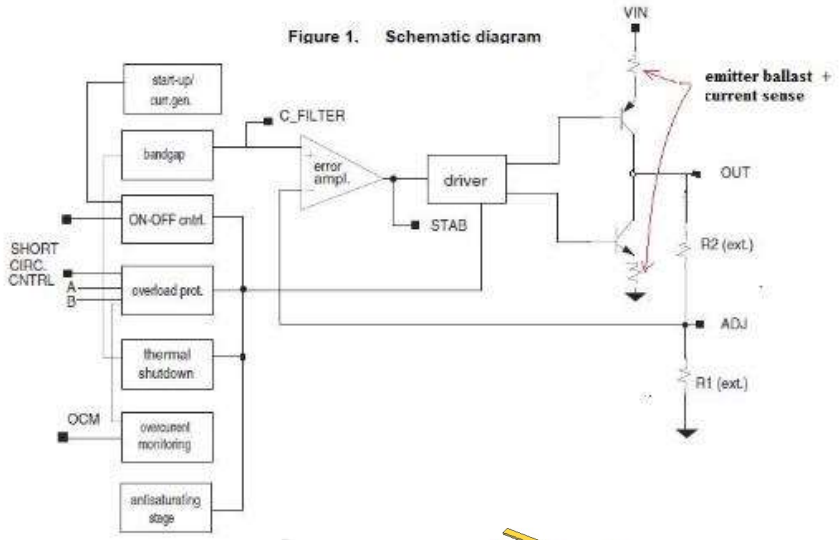
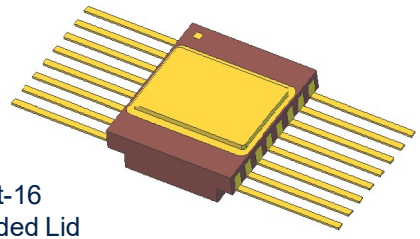
RHFL6000A
ST new generation voltage regulator

SMD : 5962F15216

- Electrical Characteristics
  - Vin: 2.5 to 12V
  - Vout: 1.2 Volt min
  - Iout: 2A max
  - Low Drop: 0.28 V typ @ 0.4A
  - Over Temperature & Over Current Protection
  - Adjustable Short Circuit Protection
  - Accessible Control Loop
  - Inhibit Pin: 35µA max shutdown
  - HF2CMOSRH: Same as RHFL4913
- Best in Class Radiation Performances
  - 300 krad(Si) ELDRS free
  - SEL Free @ 120 MeV.cm2/mg @ 125 °C
  - SET < 3% up to 12 Volt / 300 mA & < 3.3% up to 4.0 V / @ 1 A

Figure 1. Schematic diagram





Flat-16
Grounded Lid

Thank you

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