EMC - System Immunity against Electrostatic Discharges Webinar

How to protect PCB against electrostatic discharges

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Introduction
EMC Immunity is the ability of an equipment to properly operate in its electromagnetic environment by limiting the interference of electromagnetic energy that may cause physical damage.

- Radiated immunity
- Radiated emission
- Conducted immunity
- Conducted emission
• ESD Protection at System Level
• How to select an ESD protection device?
• ESD Layout Guidelines
• Application Examples
ESD Protection at System Level
How ESD is Generated?

**Triboelectric Charge**

- Material Contact
- Material Separation

Figure 1: The Triboelectric Charge. Materials Make Intimate Contact

Figure 2: The Triboelectric Charge - Separation

<table>
<thead>
<tr>
<th>Mean of Generation</th>
<th>10-25% RH</th>
<th>65-90% RH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Walking Across Carpet</td>
<td>35,000V</td>
<td>1,500V</td>
</tr>
<tr>
<td>Walking Across Vinyl Tile</td>
<td>12,000V</td>
<td>250V</td>
</tr>
<tr>
<td>Worker at a Bench</td>
<td>6,000V</td>
<td>100V</td>
</tr>
<tr>
<td>Poly Bag Picked up from Bench</td>
<td>20,000V</td>
<td>1,200V</td>
</tr>
<tr>
<td>Chair with Urethane Foam</td>
<td>18,000V</td>
<td>1,500V</td>
</tr>
</tbody>
</table>

Source: https://www.esda.org/about-esd/esd-fundamentals/part-1-an-introduction-to-esd/
In preparation for this white paper, the Industry Council conducted a worldwide survey of the electronics industry concerning EOS. Results confirmed the long held view that EOS is consistently one of the “high bars” on product failure Pareto charts. Looking at the EOS survey, respondents reported greater than 20% of total failures being EOS-related or 30% of total electrical failures being EOS-related, making EOS the largest bar on the Pareto chart of that responder’s known causes of returns.

Source: https://pdfs.semanticscholar.org/235b/0bfd01dd5f0c6c2c99df3b93bc27f56a9cfd.pdf

“30% of total electrical failure is EOS -related”

- Silicon melting
- Hole in the oxide
- Melting Flash

Source: STMicroelectronics
ESD Sensitivity is Increasing

$V_{dd} = \text{power supply voltage}$

$V_{BD} = \text{breakdown voltage}$
ESD and EOS Standards

ESD
Electro-Static Discharge

Component level
to ensure manufacturability

HBM
Human Body Model

MM
Machine Model

CDM
Charged Device model

System level
to assure robustness

IEC 61000-4-2
ISO10605 (auto)
Final user simulation

EOS
Electrical Over Stress

System level
to simulate car behavior

ISO7637
ISO16750

These standards have low-level surges as factories are well-controlled environments.

System robustness for end users. Uncontrolled environment.
HBM and IEC Standards

Difference in standards: IEC 61000-4-2 carries more energy than HBM

IEC 61000-4-2 for system (+/-8kV for level 4)

Human Body Model for IC (+/-2kV for most of IC)
Component Level vs System Level

Silicon Die Area Comparison

Silicon die area for component level ESD
(2 kV HBM)

Silicon die area for system level ESD
(8 kV IEC contact)
System-level ESD protection standard

IEC 61000-4-2 test bench

<table>
<thead>
<tr>
<th>Stress Level</th>
<th>Contact discharge</th>
<th>Air discharge</th>
<th>Number of dischargeq</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>4</td>
<td>At least 10 single discharges at 1 Hz in the most sensitive polarity</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

System state as a result of system–level ESD stress

A. Normal performance
B. Temporary loss of function or degradation of performance which cease after the disturbance ceases. The DUT recover its normal performance, without operator intervention
C. Temporary loss of function or degradation of performance, the correction of which requires operator intervention
D. loss of function or degradation of performance, no recovery possible

Self-restored
Require a system reset
## ESD in Automotive: ISO10605

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Mode</th>
<th>Component accessible from:</th>
<th>Test (A= Air, C= Contact)</th>
<th>Capacitance</th>
<th>Resistance</th>
<th>Max test voltage</th>
<th>Operating conditions</th>
<th>Min. number of discharges</th>
<th>Min. time interval</th>
<th>Max suggested severity levels (ISO10605 Annex C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td>Direct</td>
<td>Inside</td>
<td>A &amp; C</td>
<td>330 pF</td>
<td>330 ohm</td>
<td>-</td>
<td>Powered</td>
<td>3</td>
<td>1s</td>
<td>15 kV C 25kV A</td>
</tr>
<tr>
<td>Component</td>
<td>Direct</td>
<td>Outside</td>
<td>A &amp; C</td>
<td>150 pF</td>
<td>330 ohm</td>
<td>-</td>
<td>Powered</td>
<td>3</td>
<td>1s</td>
<td>15 kV C 25kV A</td>
</tr>
<tr>
<td>Component</td>
<td>Indirect</td>
<td>Inside</td>
<td>C</td>
<td>330 pF</td>
<td>330 ohm</td>
<td>-</td>
<td>Powered</td>
<td>50</td>
<td>50ms</td>
<td>20kV C</td>
</tr>
<tr>
<td>Component</td>
<td>Indirect</td>
<td>Outside</td>
<td>C</td>
<td>150 pF</td>
<td>330 ohm</td>
<td>-</td>
<td>Powered</td>
<td>50</td>
<td>1s</td>
<td>20kV C</td>
</tr>
<tr>
<td>Component packaging and handling</td>
<td>Direct</td>
<td>NA</td>
<td>A &amp; C</td>
<td>150 pF</td>
<td>330 or 2000 ohm</td>
<td>-</td>
<td>Unpowered</td>
<td>3</td>
<td>1s</td>
<td>8kV C 15kV A</td>
</tr>
<tr>
<td>Vehicle test</td>
<td>Direct</td>
<td>Inside</td>
<td>A &amp; C</td>
<td>330 pF</td>
<td>330 or 2000 ohm</td>
<td>15 kV Engine drive or idle</td>
<td>3</td>
<td>1s</td>
<td>8kV C 25kV A</td>
<td></td>
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<tr>
<td>Vehicle test</td>
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<td>1s</td>
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<td></td>
</tr>
</tbody>
</table>
How to Select ESD Protection Device
### Key Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RM}$</td>
<td>Stand-off voltage (normal condition voltage)</td>
</tr>
<tr>
<td>$I_{RM}$</td>
<td>Leakage current</td>
</tr>
<tr>
<td>$V_{BR}$</td>
<td>Breakdown voltage (voltage when the ESD protection starts working)</td>
</tr>
<tr>
<td>$V_{CL}$</td>
<td>Clamping voltage (maximum voltage across the ESD protection)</td>
</tr>
<tr>
<td>$I_{PP}$</td>
<td>Peak Pulse Current (maximum current in the ESD protection)</td>
</tr>
<tr>
<td>$C$</td>
<td>Line capacitance (impacts signal integrity)</td>
</tr>
</tbody>
</table>

![Diagrams showing the behavior of ESD protection under unidirectional and bidirectional conditions.](image)
Protection Selection
Key Parameter: Voltage

No TVS protection

With TVS protection

Failure
Key Parameters
Voltage Polarity

- Mandatory for audio and RF signals

No TVS protection

With TVS protection

- Bi-directional

- Failure

- Voltage Polarity

- No TVS protection

- With TVS protection
Key Parameters

Capacitance Value

- Example of the impact of parasitic capacitance on high-speed signal simulated with discrete capacitance

\[ fc = \frac{1}{\pi t_r} \]

fc is high enough to comply with HDMI 1.485 Gbps
Eye Diagram

What is an Eye Diagram?
Impact on Data-lines
Eye Diagram Integrity

- USB 3.1 Gen2 mask at 10.0 Gbps per channel
  (Type-C connector, reference cable, EQ with DC=6dB and DFE)

Line without HSP053-4M5

Line with HSP053-4M5
Impact on Data-lines

Time Domain Reflectometer Impedance

TDR with 200ps pulse rise time impedance of 100Ω line without / with HSP053-4M5

HDMI 2.0b TDR specification: 100Ω ±15Ω
Impact on RF-signal
S21 Attenuation

- **ESDARF02-1BU2CK S21**
  - 30 GHz at -3 dB
  - 8 GHz at -0.5 dB

- **Negligible impact major frequencies for tele**
  - FM radio: 87.5 MHz - 108.0 MHz
  - Numerical TV: 400 MHz – 900 MHz
  - Cellular phones: 700 MHz … 4.7 GHz
  - GNSS: 1.6 GHz
  - Bluetooth: 2.4 GHz
  - Sub-GHz industrial: 400 MHz … 1.1GHz
  - WiFi: 2.4 / 5.0 GHz
ESD Protection

IEC 61000-4-2 +/-8kV ESD Response

- IEC 61000-4-2 response of ESD051-1BF4:
  - First peak: 23V (low energy, CDM like)
  - 30ns clamping: 11V (clamping voltage)
• IEC 61000-4-2 8 kV 30 ns clamping voltage ↔ TLP* 16 A 100 ns 70 - 90% voltage

Injected current:
16A – 100ns square current

Measured voltage on 70% – 90% windows on ESD051-1BF4 : 10.5V

*ANSI / ESD STM5.5.1-2014
ESD Protection

Transmission Line Pulse* I/V Curve

- I/V TLP* curve is done with several pulses

ESD051-1BF4 TLP* I/V curve

*ANSI / ESD STM5.5.1-2014
System-Efficient ESD Design Methodology

- TLP input current shared between high performance MCU FT input and ESDA5-1BF4
- High performance MCU + ESDA5-1BF4 robustness reach more than 8kV IEC 61000-4-2
  - Even if, ESD5-1BF4 clamping voltage > High Performance MCU FT input AMR
- ESD051-1BF4
  - 11V clamping voltage at +8kV ESD 61000-4-2
- High Performance MCU FT input
  - 3.6 V max operating
  - 2 kV HBM ESD
  - 250 V CMD ESD
  - 5.5 V AMR

MCU destruction voltage: 12.5V
MCU working voltage: 3.3V
Snap-back Protections
System Integration

- Snap-back protection (ESDZV5-1BF4) clamping voltage lower than standard protection (ESD051-1BF4) clamping voltage

- Protected line DC voltage MUST be lower than holding voltage
  - To avoid protection latch-up i.e. continuous leakage current flowing into the protection
Recap

Basics of ESD Protection

• Transparency:
  • Capacitance must be in-line with application bandwidth / data rate

• Efficiency:
  • $V_{RM}$ must be slightly higher than maximum line voltage
    To obtain a low clamping voltage

• System integration of snap-back protection:
  • Holding voltage must be higher than DC voltage

AN5241, Fundamentals of ESD protection at system level
ESD Layout Guidelines
ESD Robustness

PCB Layout Impact

- PCB Tracks must be under control!
- For protection device length connection of ~1cm from side to side, 35µm copper, 0.5mm wide (microstrip)
- $2 \times L = 5 \text{ nH}$!
Assuming that lines inductance is $L = 5\text{nH}$

$\frac{di}{dt} = 37.5\text{ A/ ns}$

$V_{ic} = V + 2 \times L \times \frac{di}{dt}$

$V_{ic} = V + 375\text{ V}$

ESD surge is 8 kV /0.8 ns rise time, this makes 37.5 A/ns
ESD Robustness
PCB Layout Recommendation

Vias to GND plane as close as possible to the product GND
In this case, $V_{ic} \leq V$

In addition, ESD protection must be placed as close as possible to the ESD source, to avoid any coupling between tracks on the PCB.
Application Examples
Recommended Protection Devices and PCB Layouts
Protections and Filters Around MCUs

- **ESDA7P120-1U1M**
- **DSILC6-4P6 (TAG)**
- **EMIF03-SIM02M8**
- **SMA6F**
- **ESDA5V3L**
- **ETH 1G, secondary**
- **EMIF06-MSD02N16 (SD 2.0)**
- **TCP01-M12 Type-C Port Protection**
- **HSP051-4M10 ETH 1G, secondary**
- **ECMF04-4HSWM10 High Speed Differential MIPI, USB 3.1, Display port, HDMI**
- **SWD & JTAG ESDALC6V1W5**
- **USBLC6-2SC6**
- **ESDA14V2BP6**
- **SMA6F**
- **SMAJ40CA**
- **CLT03-2Q3 PLC inputs**
DESIGN TIP: Place the ESD protection close to ESD source: here close to USB connector.

- Compliant with USB 2.0 eye diagram
- ESD robustness: ± 15 kV contact discharge IEC61000-4-2

USBLC6-2SC6

SOD323-6L
**DESIGN TIP:**
Place the ESD protection close to ESD source:
here close to RS-232 connector

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**ESDA14V2BP6**

- Low capacitance, 4-line, bi-directional ESD protection
- ESD protection as per IEC61000-4-2 Level 4: ± 8kV contact

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**STM32L4R9I-EVAL**

- **Low capacitance, 4-line, bi-directional ESD protection**
- **ESD protection as per IEC61000-4-2 Level 4: ± 8kV contact**
USER BUTTON
GPIO Input

Design note:
Although buttons are not made of conductive materials, they are highly sensitive to ESD air discharge used during IEC certification tests.

ESDA5V3L
- PCB space saving: 2 diodes array
- ESD robustness: ± 30 kV contact discharge IEC61000-4-2

SOT23-3L
ESD protections in STM32MP1

- **MORPHO CONNECTOR**
  - ESDA7P120-1U1M
  - 5V Vin

- **MICRO SD CARD**
  - HSP051-4M10 (x2)
  - SDMMC dataline

- **USB Type-C Power Delivery**
  - ESDA7P120-1U1M, ESDA25L
  - VBUS, CC1, CC2

- **ETHERNET**
  - HSP053-4M5

- **AUDIO**
  - ESDA6V18C6: 4-line ESD protection
  - OUTA, OUTB, MIC IN

- **USER BUTTONS**
  - ESDALC6V1-1U2

- **ST-LINK USB CONNECTOR**
  - USBLC6-2P6
  - DP, DM, VBUS

- **USB HOST x2 (Dual USB Type-A)**
  - ESDA7P120-1U1M (x2), ECMF02-2AMX6 (x2)
  - VBUS, DP, DM

- **USB Type-C DRP (Source Only)**
  - ESDA7P120-1U1M, ESDA25L, ECMF02-2AMX6
  - VBUS, CC1, CC2, DP, DM

- **USB HOST x2 (Dual USB Type-A)**
  - ESDA7P120-1U1M (x2), ECMF02-2AMX6 (x2)
  - VBUS, DP, DM

- **HDMI**
  - ECMF04-4HSWM10 (x2), ESDALC6V1-5M6
  - CEC, I2C, HPD, TMDS datalines
Any Electronic Board Must be Protected

3D-printer Control Board

- Protections on the application PCB
  - Power lines → surge protection : IEC 61000-4-5
  - Connector
  - Button
  - SD card
- Integrated on all IC’s → ESD protection for manufacturing is JEDEC HBM

ESDA5V3L   EMI06-MSD02N16
SMAJ12A   SMBJ24A
3x USBLC6-2SC6

ESD protection for system : IEC 61000-4-2
Resources
Application Notes and Video

- **AN5241**, Fundamentals of ESD protection at system level
- **AN4871**, USB Type-C protection and filtering
- **AN5121**, HDMI ESD protection and signal conditioning products for STBs
- **AN3353**, IEC 61000-4-2 standard testing
- **AN2689**, Protection of automotive electronics from electrical hazards, guidelines for design and component selection
- **AN1826**, TRANSIENT PROTECTION SOLUTIONS: Transil™ diode versus Varistor
- **AN5241**: Fundamentals of ESD Protection
- **Video** - ESD Protection: why and how to protect microcontrollers efficiently
ST PROTECTION-FINDER is an application available for Android™ and iOS™ that allows you to explore ST’s TVS product portfolio.

- Parametric or series search engine
- Efficient part number search engine
4 Steps to Discover ST’s Portfolio

1. OPEN application
   - ST Protection Finder (1.0.1 ML off)

2. SELECT parameter
   - ESD Protection (ESD1000-E-3)
   - TVS clamping diodes (TVS1000-3 and TVS2000-3)
   - Current-Limiting Termination for Programmable Logic Controllers

3. CHOOSE product
   - Vth Typ 5 V
   - Breakdown voltage: 700 mV to 39 V
   - Line Capacitance I/O-GND: 300 pF to 350 pF
   - Nb of Line 4

4. GET datasheet
   - EMI02-020ABRY
     - Vth Typ 3 V
     - CLine Typ 1.2 pF
     - Nb of Line 2
     - Package QFN-6L WF

Key Features:
- Attenuation profile compliant with BroadR Reach™ requirements from -40 °C to 125 °C
- Return loss (S21) at 60 MHz: -20 dB
- Components matching: ±1% (between line 1 and 2)
- Package:
  - Dimensions: 3.0 x 3.0 mm
  - Pitch: 1.1 μm
  - Wettable flank QFN
- AEC-Q101 compliant

Technical Documentation:
Data Sheet
- Description: Version 1.0
- Size: 115 KB
Thank you!