



HSP series portfolio overview

High-speed port ESD protection

Is this presentation suited for you?

Where do you stand with high-speed port protection?

Beginner?

I am not familiar with this subject. I am in the discovery phase and would like an overview and a basic understanding of the technology.

[Click here to continue to next slide](#)

Overview

Intermediate?

I have a basic understanding of this subject. I would like to go deeper in details and tackle more aspects of this subject.

[Click here to open new presentation](#)

Basic

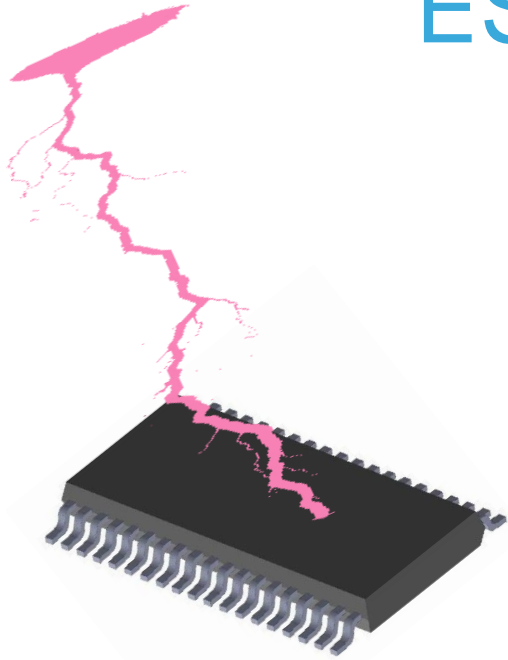
Advanced?

I am very familiar with this subject. I would like to deepen my knowledge and become an expert.

[Click here to open new presentation](#)

In depth

ESD protection is needed for



Core ICs such as microcontrollers, micro-processors, transceivers, etc.

Advanced technology with very **thin lithography** and gate oxide highly vulnerable to ESD

Integrated electronics systems with **PCBs having a high component density** facilitate ESD **coupling** and **propagation**

IC manufacturers reluctant to make robust embedded ESD protection diodes that would require a **significant active area of their advanced and expensive technology.**



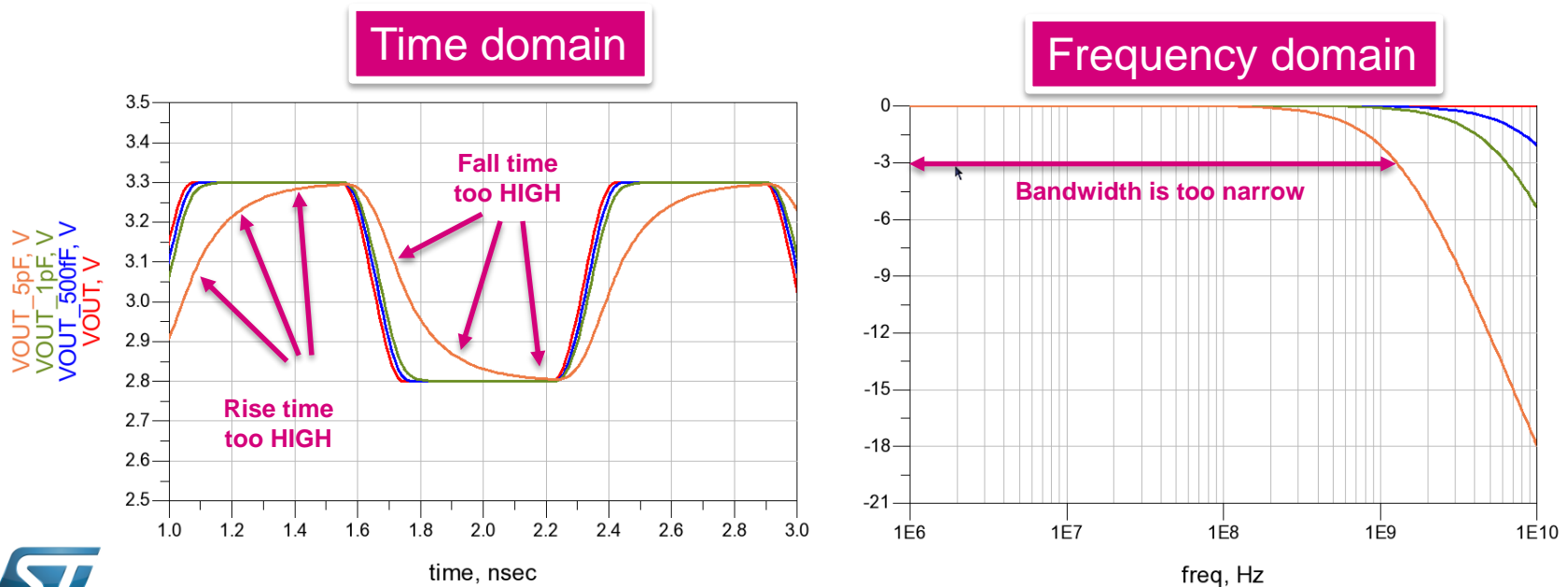
When the **application uses RF** (Wi-Fi or Bluetooth), a **common-mode filter is required**, in addition to ESD protection, to avoid **RF performance decrease** due to the EMI generated by the high-speed link.

Dedicated to high-speed ports

Ultra-low capacitance

- The parasitic capacitance of ESD protection devices must be low enough to allow high-speed signals to be transmitted without degradation.
- A high parasitic capacitance of the ESD protection devices would increase too much the signal rise/fall time and prevent the communication.

Example of the impact of parasitic capacitance on an HDMI signal simulated with discrete capacitance



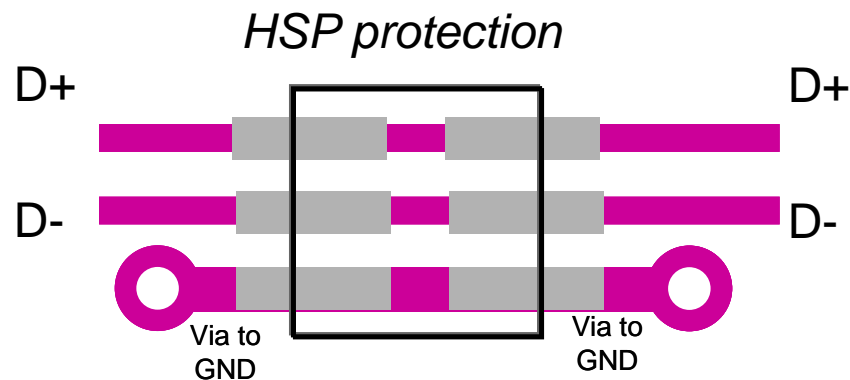
Dedicated to high-speed ports

Flow-through layout

5

- To make the design and PCB layout **easier and simpler**
- To preserve the **symmetry** between the 2 lines of the differential lane

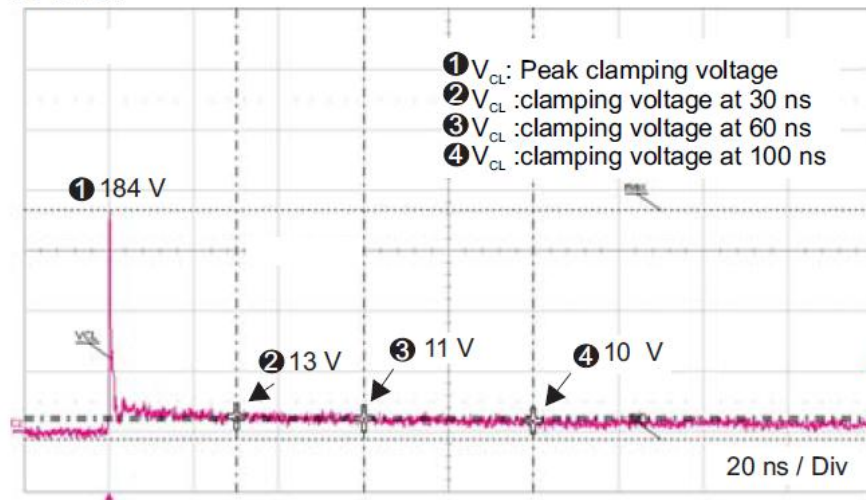
→ **High-speed port protection must be flow-through**



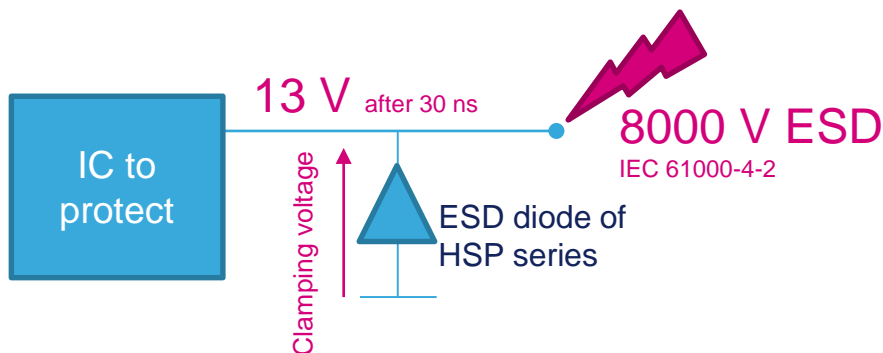
Clamping voltage

**ESD response to IEC 61000-4-2 (+8 kV contact discharge)
Example of HSP051-4M10**

50 V / Div



- The quality of protection lies in the clamping voltage of the ESD diodes
- It is measured after 30 ns (the first peak voltage is in the nanosecond range; too fast to be significant)
- HSP protection devices can clamp 8000 V ESD strikes down to 13 V !



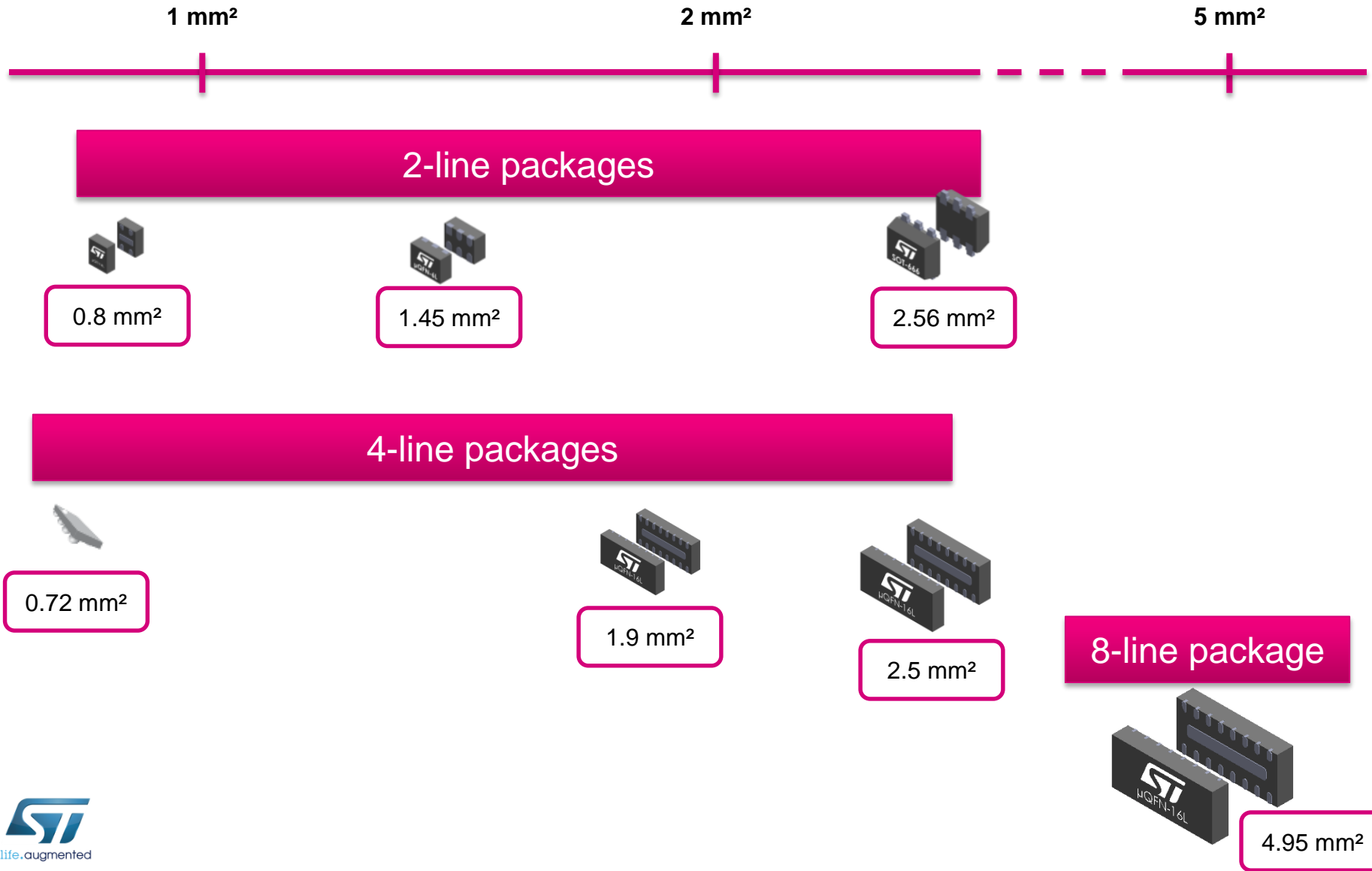
Main selection criteria

- **V_{BR} Breakdown voltage** higher than operating signal
Above this voltage, the ESD protection devices will enter Clamping mode
- **f_c Cut-off frequency** higher than high-speed signal bandwidth defined by the rise time value
- **$C_{I/O \text{ to GND}}$ Low parasitic capacitance** (a consequence of high bandwidth) minimizing the impact on transmission line impedance
- **R_d Dynamic resistance & V_{CL} Clamping voltage** to keep the protected IC safe

Example of HSP051-4M10

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	4.5	5.8		V
I_{RM}	$V_{RM} = 3.6 \text{ V}$		10	100	nA
V_{CL}	$I_{PP} = 1 \text{ A}, 8/20 \mu\text{s}$			10	V
V_{CL}	IEC 61000-4-2, +8 kV contact ($I_{PP} = 16 \text{ A}$), measured at 30 ns		13		V
R_d	Dynamic resistance, pulse duration 100 ns	I/O to GND	0.48		Ω
		GND to I/O	0.96		
$C_{I/O - I/O}$	$V_{I/O} = 0 \text{ V}, F = 200 \text{ MHz to } 9 \text{ GHz}$		0.2	0.3	pF
$C_{I/O - GND}$	$V_{I/O} = 0 \text{ V}$	$F = 200 \text{ MHz to } 2.5 \text{ GHz}$	0.4	0.55	pF
		$F = 2.5 \text{ GHz to } 9 \text{ GHz}$	0.35	0.45	pF
f_c	-3dB		10		GHz
Z_{diff}	Time domain reflectometry: $t_r = 200 \text{ ps}$ (10 - 90%), $Z_0 = 100 \Omega$	85	100	115	Ω

High-speed port protection package offer



High-speed port protection portfolio

2 lines

HSP061-2N4

*μQFN-4L 400-μm pitch
Size: 1 x 0.8 x 0.5 mm*

HSP062-2M6

*μQFN-6L 500-μm pitch
Size: 1 x 1.45 x 0.55 mm*

HSP062-2P6

*SOT-666
Size: 1.6 x 1.6 x 0.52 mm*



4 lines

HSP061-4F4

*Flip Chip / WLCSP
6 bumps – 300-μm pitch
Size: 0.6 x 1.2 x 0.38 mm*

HSP051-4N10

*DFN-10L 400-μm pitch
Size: 1 x 1.9 x 0.3 mm*

HSP051-4M10

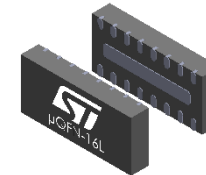
*DFN-10L 500-μm pitch
Size: 1 x 2.5 x 0.48 mm*



8 lines

HSP061-8M16

*DFN-16L 400-μm pitch
Size: 1.5 x 3.3 x 0.55 mm*



Basic presentation

*Intermediate product presentation soon available:
'Understanding ST's HSP series specification'*

In-depth information

Application Notes:

- [HSP06x-2 high-speed line protection on HDMI 1.4 link \(AN4138\)](#)
- [HSP061-8M16 high-speed line protection on HDMI 1.4 link \(AN3357\)](#)
- [TVS short-pulse dynamic resistance measurement ... \(AN4022\)](#)
- [IEC 61000-4-2 standard testing \(AN3353\)](#)

Selection

- [Selection guide \[pdf\]](#)
- www.st.com/hsp-protection



Thank you