Ultra-low capacitance single-line ESD protection portfolio overview

‘Ultra Low’ (ULC) and ‘eXtra Low’ (XLC) capacitance ESD protection
Is this presentation suited for you?

Where do you stand with high-speed port protection?

<table>
<thead>
<tr>
<th>Beginner?</th>
<th>Intermediate?</th>
<th>Advanced?</th>
</tr>
</thead>
<tbody>
<tr>
<td>I am not familiar with this subject. I am in the discovery phase and would like an overview and a basic understanding of the technology.</td>
<td>I have a basic understanding of this subject. I would like to go deeper in details and tackle more aspects of this subject.</td>
<td>I am very familiar with this subject. I would like to deepen my knowledge and become an expert.</td>
</tr>
</tbody>
</table>

Options:
- Overview
- Basic
- In depth

Click here to continue to next slide.
ESD protection is needed for

- Advanced technology with very **thin lithography** and gate oxide highly vulnerable to ESD.
- Integrated electronics systems with **PCBs having a high component density** facilitate ESD **coupling and propagation**.
- IC manufacturers reluctant to make robust embedded ESD protection diodes that would require a **significant active area of their advanced and expensive technology**.

Core ICs such as microcontrollers, micro-processors, transceivers, etc.

When the **application uses RF** (Wi-Fi or Bluetooth), a **common-mode filter is required**, in addition to ESD protection, to avoid **RF performance decrease** due to the EMI generated by the high-speed link.
Why ultra-low capacitance?

- The parasitic capacitance of ESD protection devices must be low enough to allow high-speed signals to be transmitted without degradation.

- A high parasitic capacitance of ESD protection devices would increase too much the signal rise/fall time and prevent the communications.

Example of the impact of parasitic capacitance on an HDMI signal simulated with discrete capacitance.

(Time domain)

(Frequency domain)

Bandwidth is too narrow

Rise time too HIGH

Fall time too HIGH
Single line for flexibility

- Single-line ESD protection provides flexibility on the PCB layout.
- ST offers industry-standard micro-packages such as the 0402 and 0201 to release designers from space constraints.

**Example of PCB density**

PCB area < 0.5 cm²

- **0402**
  - 0.5 mm
  - 1.0 mm
  - Thickness: 0.5 mm
  - 0.6 mm²
  - More than 3 x SMALLER AREA

- **0201**
  - 0.3 mm
  - 0.6 mm
  - Thickness: 0.3 mm
  - 0.18 mm²
The quality of protection lies in the clamping voltage of the ESD diodes.

It is measured after 30 ns (the first peak voltage is in the nanosecond range; too fast to be significant).

0.2 pF single-line ESD protection devices can clamp 8000 V ESD strikes down to 19 V!
Main selection criteria

• $V_{BR}$ Breakdown voltage higher than operating signal
  Above this voltage, the ESD protection devices will enter Clamping mode

• $C_{LINE}$ Low parasitic capacitance (a consequence of high bandwidth) minimizing the impact on transmission line impedance

• $f_c$ Cut-off frequency higher than high-speed signal bandwidth defined by the rise time value

• $R_d$ Dynamic resistance & $V_{CL}$ Clamping voltage to keep the protected IC safe

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Example of ESDARF02-1BU2CK

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<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR}$</td>
<td>$I_R = 1 \text{ mA}$</td>
<td>5</td>
<td>6.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{RM}$</td>
<td>$V_{RM} = 3.6 \text{ V}$</td>
<td>5</td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$V_{CL}$</td>
<td>$I_{PP} = 1 \text{ A}, 8/20 \mu\text{A}$</td>
<td>10</td>
<td>12</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_d$</td>
<td>Dynamic resistance, pulse duration 100 ns</td>
<td>1.3</td>
<td></td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$C_{LINE}$</td>
<td>$F = (200 \text{ MHz} - 3000 \text{ MHz}), V_R = 0 \text{ V}$</td>
<td>0.2</td>
<td>0.3</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

$fc @ -3 \text{ dB} >> 10 \text{ GHz}$
**Single-line portfolio**

**0402 package**
1.0 x 0.6 x 0.5 mm

- ESDAXLC6-1BT2
  - 0.5 pF (maximum)

- ESDAXLC6-1MY2
  - 0.35 pF (maximum)

**0201 package**
0.6 x 0.3 x 0.3 mm

- ESDAULC5-1BF4
  - 1.5 pF (typical)
  - 13.5 V @ 30 ns

- ESDAULC6-1U2
  - 0.8 pF (typical)

- ESDARF01-1BF4
  - 0.6 pF (typical)
  - 6.8 V @ 30 ns, \( V_{BR} = 0.6 \) V

- ESDAXLC6-1BU2
  - 0.4 pF (typical)

- ESDARF02-1BU2
  - 0.24 pF (typical)
  - 36 V @ 30 ns

- ESDARF02-1BU2CK
  - 0.2 pF (typical)
  - 30 V @ 30 ns

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**CLC**
Line capacitance

- < 2 pF

**ULC**
Ultra Low Capa

- < 0.5 pF

**XLC**
eXtra Low Capa

- < 0.5 pF
Let’s go further

Basic presentation
Intermediate product presentation soon available: ‘Understanding ST’s ESD ultra-low capacitance (XLC and ULC) series specification’

In-depth information
Application Notes:
- TVS short-pulse dynamic resistance measurement ... (AN4022)
- IEC 61000-4-2 standard testing (AN3353)

Selection
- Selection guide [pdf]
- www.st.com/esda-ultralowcapa
Thank you