LDBL20

Ultra-small 200 mA LDO in an ST STAMP™ package

Product presentation

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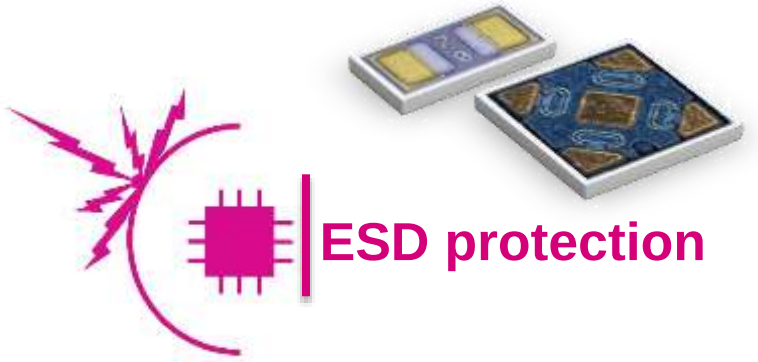
What is ST STAMP™

ST STAMP™ ▪ **ST S**mall **T**hickness **A**dvanced **M**icro **P**ackage

is S*T's* trademark for the unique and innovative bumpless CSP package.

Compared to the smallest available DFN plastic packages and flip-chips, the ST STAMP™ solution provides similar package performance and reliability, reducing the total height to 200 µm or less, with a dramatically smaller footprint.

ST STAMP is compatible with industry-standard SMT processes and soldering techniques.



ESD protection

Voltage regulators

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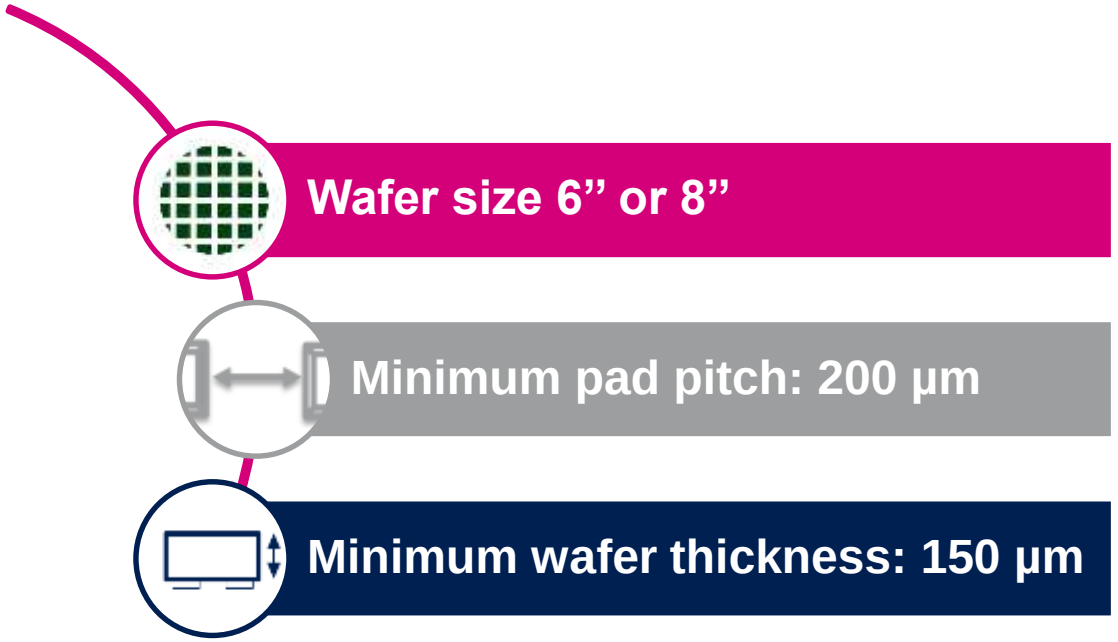
ST STAMP™ - Key facts and benefits



Examples:

01005 SMD

DFN4-like (0.8 x 0.8 mm)

4 pads (0.47 x 0.47 mm)

- Discrete or integrated components manufactured in chip-scale at wafer level, on standard production 6” and 8” silicon wafers.

→ **BENEFIT: production cost effectiveness**

- ST STAMP™ overcomes the constraints of minimum bump size and pitch of the flip-chips

→ **BENEFIT: smaller footprint and PCB area**

- The total package thickness is reduced to the silicon wafer thickness

→ **BENEFIT: the devices can be put on ultra-thin substrates and smartcards**

- The footprint can be made compatible with industry-standard leadless plastic packages (QFN, SSON…)
- JEDEC-standard SMT processes and soldering compatible

→ **BENEFIT: ease of use**

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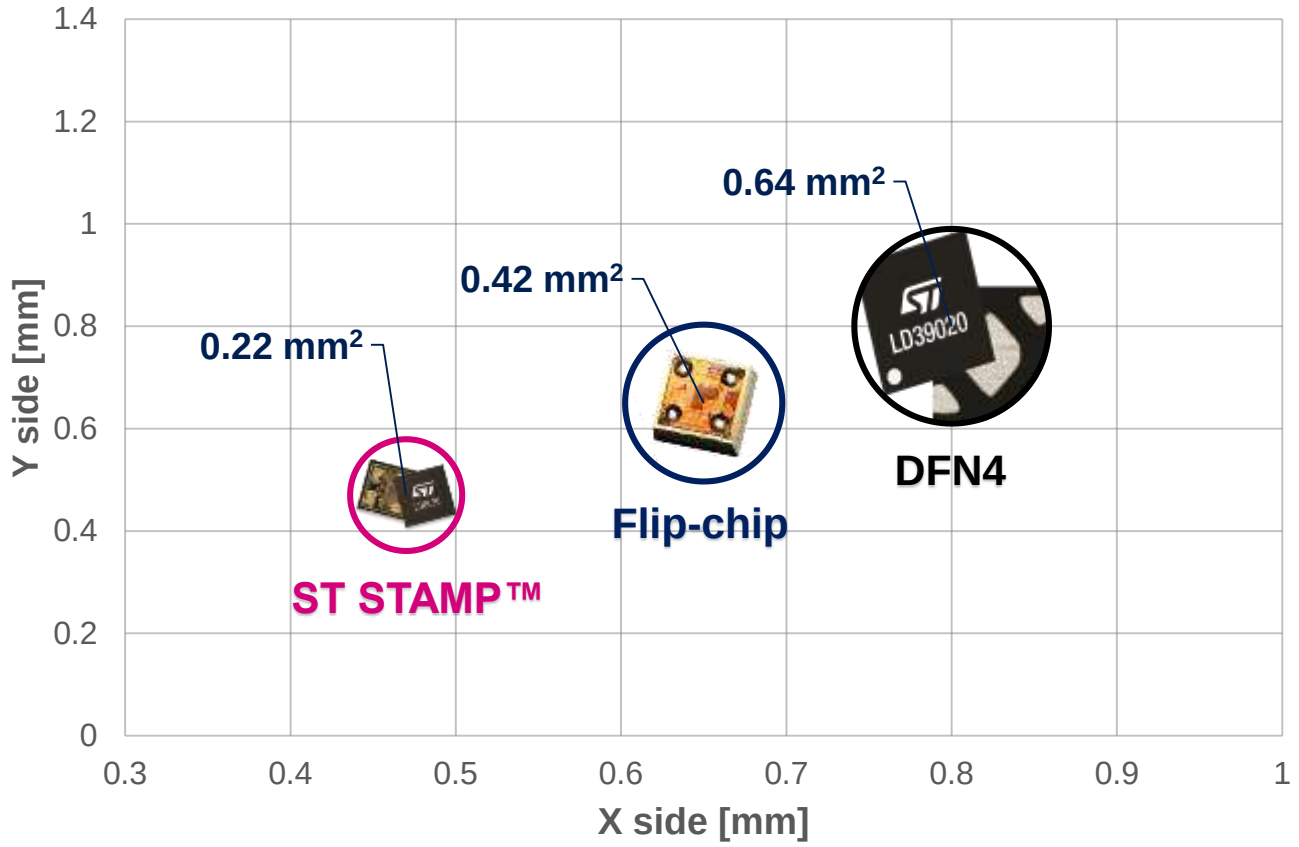
ST STAMP™ - Footprint benchmark



The graph shows a comparison in terms of footprint dimension, among the state-of-the art miniaturized packages for integrated circuits: the Flip-Chip, DFN and ST STAMP™.

The minimum package size currently available is considered for each family.

In terms of area, the ST STAMP™ can be as tiny as one third than the smallest plastic package on the market and a half of the smallest Flip-Chip.

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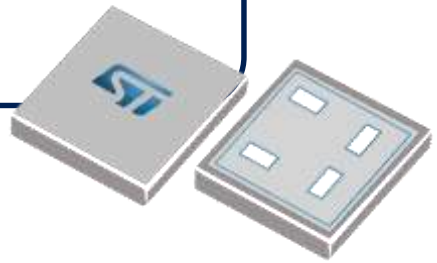
LDBL20

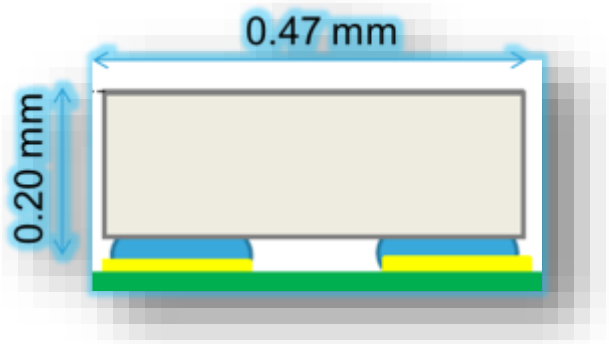
World’s smallest 200 mA LDO

Main features

- Input voltage: from 1.5 to 5.5V
- Very low dropout voltage [300 mV (typ.) @ 200 mA load current]
- Low quiescent current
  - 20 µA @ no load
  - 100 µA max @ 200 mA
  - 0.1 µA max in Off mode
- Output voltage selection range from 0.8 to 5V with 50 mV steps
- High PSRR (80 dB @1 kHz, 50 dB @100 kHz)
- Logic-controlled electronic shutdown
- Internal soft start
- Active output voltage discharge (optional)
- Available in bumpless CSP [ST STAMP™] 0.47 x 0.47 mm



The LDBL20 high-accuracy voltage regulator provides 200 mA of maximum current from an input voltage ranging from 1.5 to 5.5 V, with a typical dropout voltage of 200 mV.
It is available in the new ST STAMP™ package, allowing the maximum space saving.
The very low dropout voltage, low quiescent current and high PSRR features make the LDBL20 suitable for low power battery-operated applications.



~ 70% PCB saving vs. equivalent device in DFN4 (0.8 x 0.8 mm) package (LD39020)

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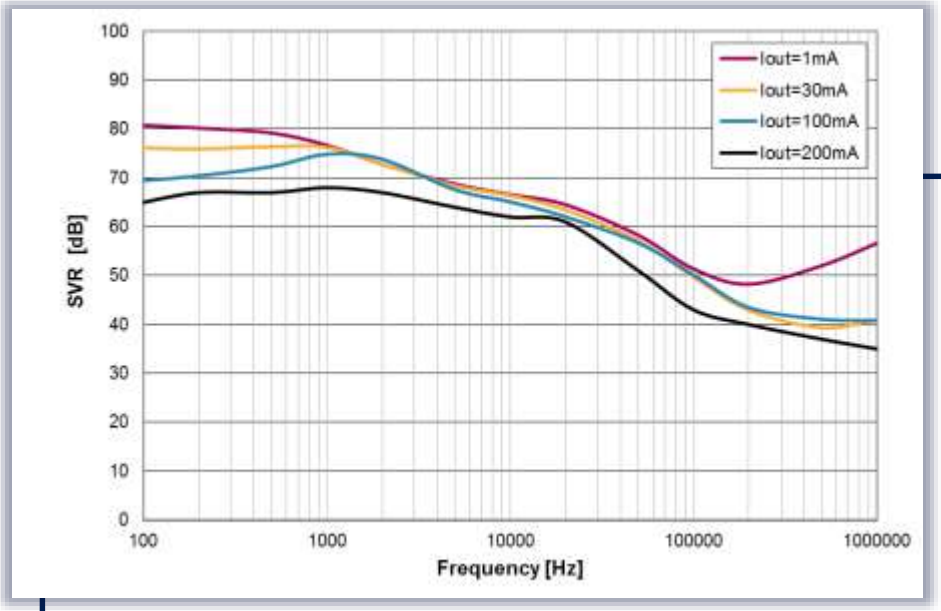
LDBL20

World's smallest 200 mA LDO
Not just small…



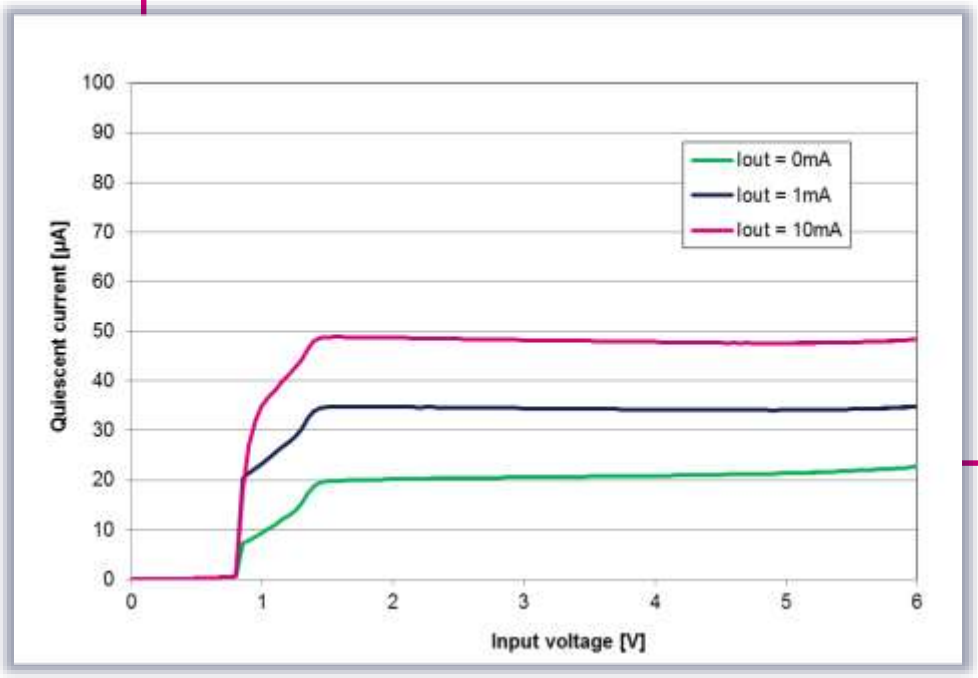
The LDBL20 features remarkable
80 dB @ 100 Hz and 50 dB @ 100 kHz PSRR figures

Cleans the DC bus from ripple and switching noises in a wide frequency band.

Provides a stable signal to MCUs and low power digital ASICs.

Allows operation at light load and low input voltage, prolonging the battery life

Low and stable quiescent current at light load.
No quiescent current increase in dropout.



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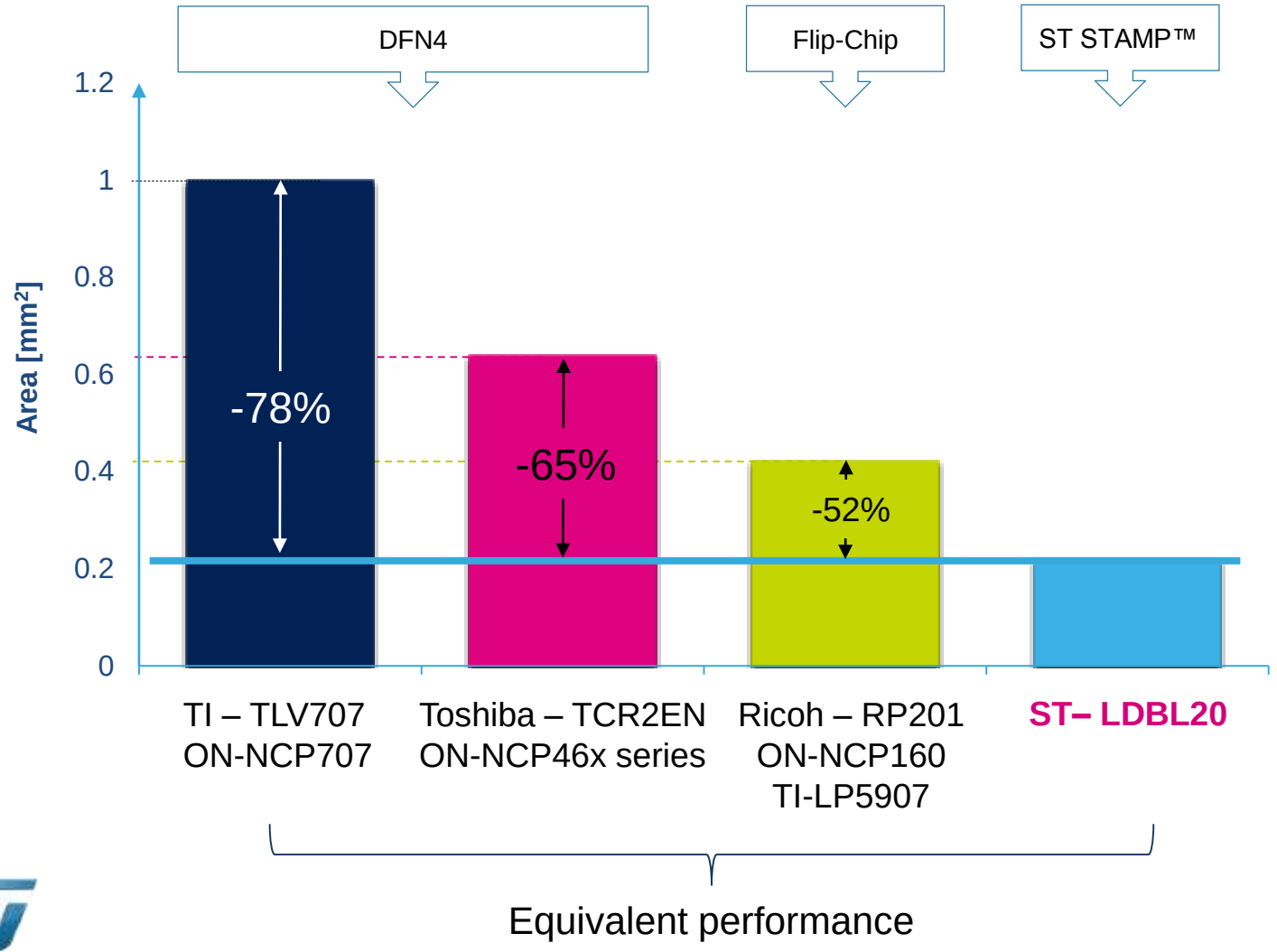
ST has… lowered the bar



Size squeezed to a minimum…
Performance maintained to the maximum

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“Think Small” with ST LDOs

100 µm

1 mm

10 mm

0.47 x 0.47 mm	0.69 x 0.69 mm	0.8 x 0.8 mm	1 x 1 mm	1.2 x 1.3 mm	2 x 2 mm
LDBL20 **STSTAMP™** **200 mA** **Fast transient response** **High PSRR**	**LD39130SJ** CSP 300 mA Auto Green Mode	**LD39115J/LD39030SJ** CSP 150 mA / 300 mA PSRR>50dB Low Noise **LD39020** DFN 200 mA 0.5% accuracy / High PSRR	**LD39020** DFN 200 mA 0.5% accuracy PSRR>50dB	**LDK120-130** DFN 200-300 mA Low noise and cost effective **LD39130SPUR** DFN 300 mA Auto green mode	**LDLN015** DFN 150 mA Ultra low noise, high PSRR **LD59015** SC70 150 mA High PSRR

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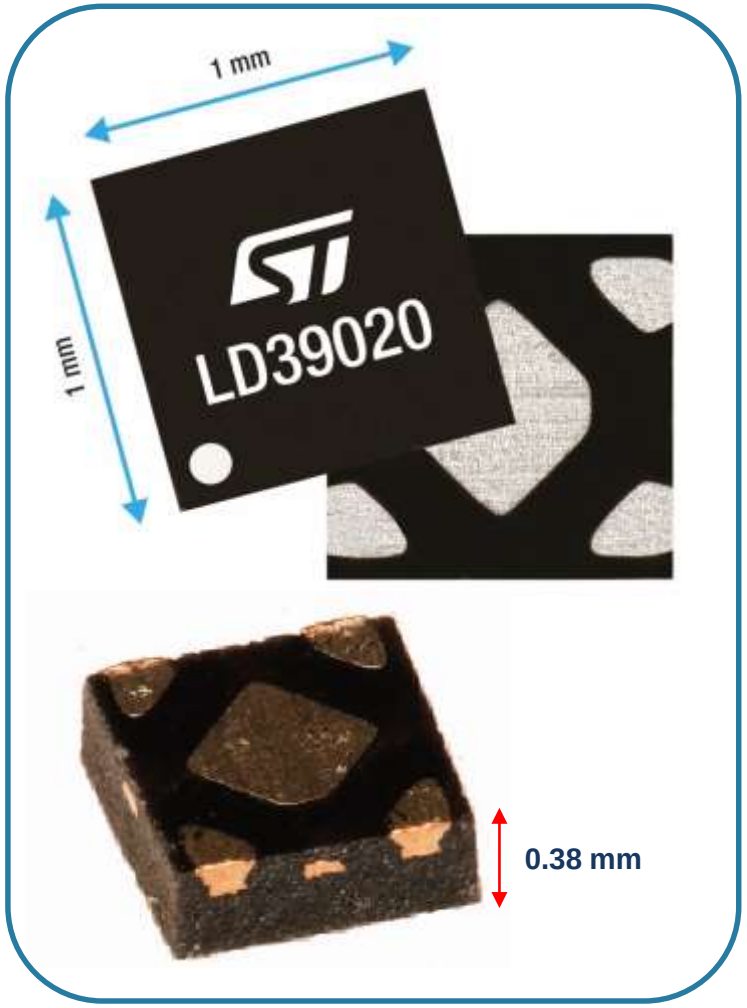
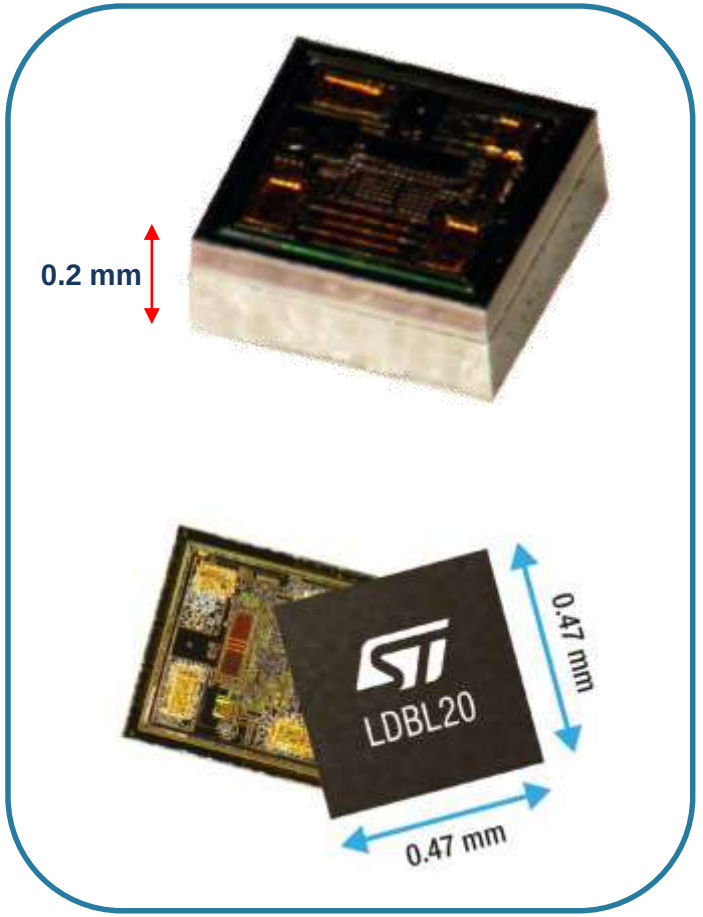
ST's high-performance miniature LDOs



LD39020
200 mA,
High PSRR



LDBL20
200 mA,
High PSRR

LD39130
300 mA,
1µA ultra low Iq

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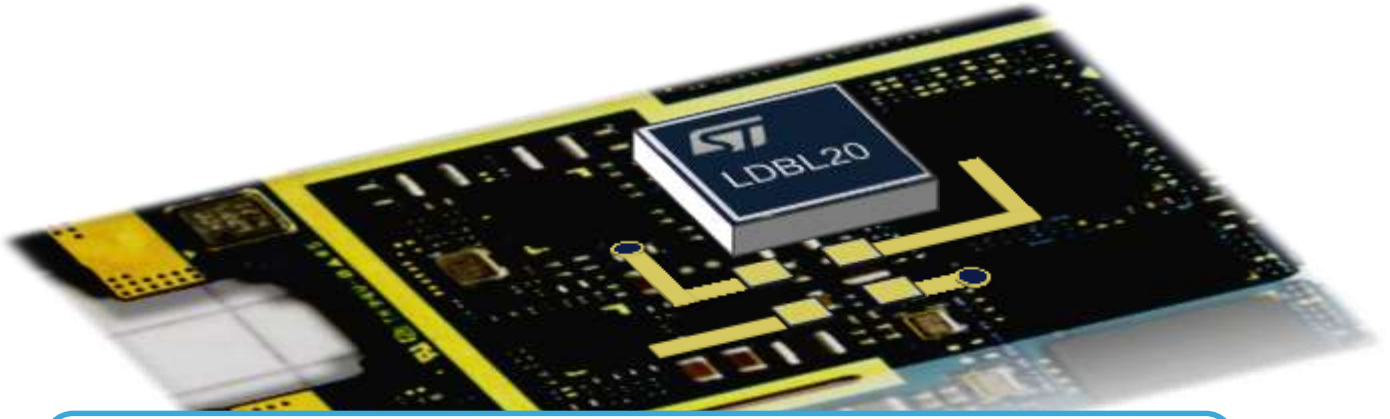
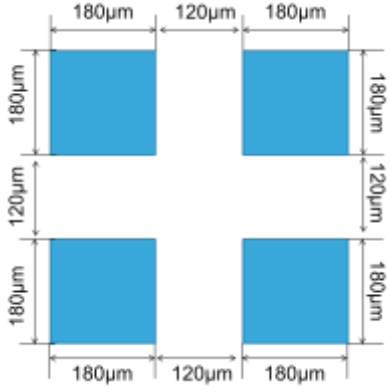
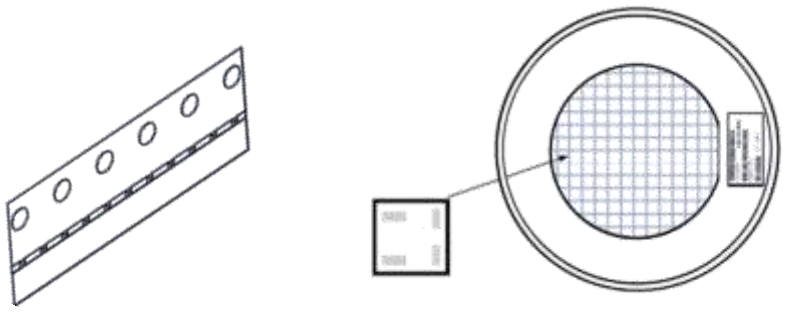
LDBL20 – Packing and mounting info



LDBL20's ST STAMP™ package is compatible with SMT mounting and soldering process.

Suggested landpattern



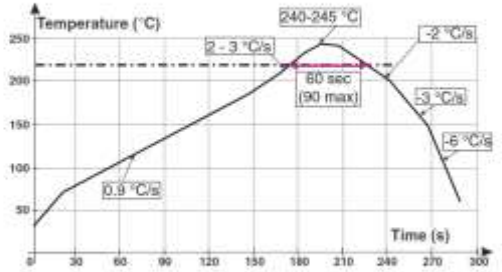


It is available in standard Tape'n'Reel and wafer on sticky foil packing solutions

SMT reflow profile as per JEDEC standards

Reflow profile

Figure 13. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement.
Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

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