ST Application Support and System Solution for NEV

Jackie JIANG

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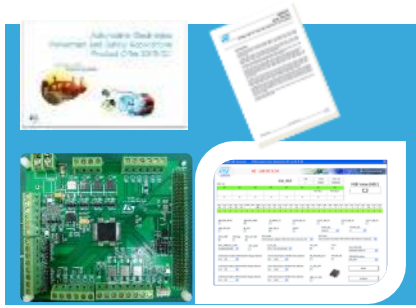
Technical Support



- Provide component level technical support environment
- Enable customer / Disty to familiar with ST device and start system development.

- Kit level solution on own or cop with Partner
- Enable Customer / DISTY to verify ST solution at system level.

- On site Joint system development with customer
- Fasten customer project time to market

- Develop China dedicated device fits China market
- Ensure new products on time, on spec on quality

- Technical training / workshop with customer / DISTY
- Enhance the technical knowhow of ST product & solution
- Quarterly bases PowerPC deep training

Product Support Package Development

System Application Development

Joint Development with Customer

China Dedicated ASSP

Training

GCSA Application Support Team

- ✓ 5.0+ Year Average Technical and application Experience
- ✓ Field / Application Engineer with good geographic coverage
- ✓ IDH / Design House
- ✓ Local Key Software Houses
- ✓ Local NPP support

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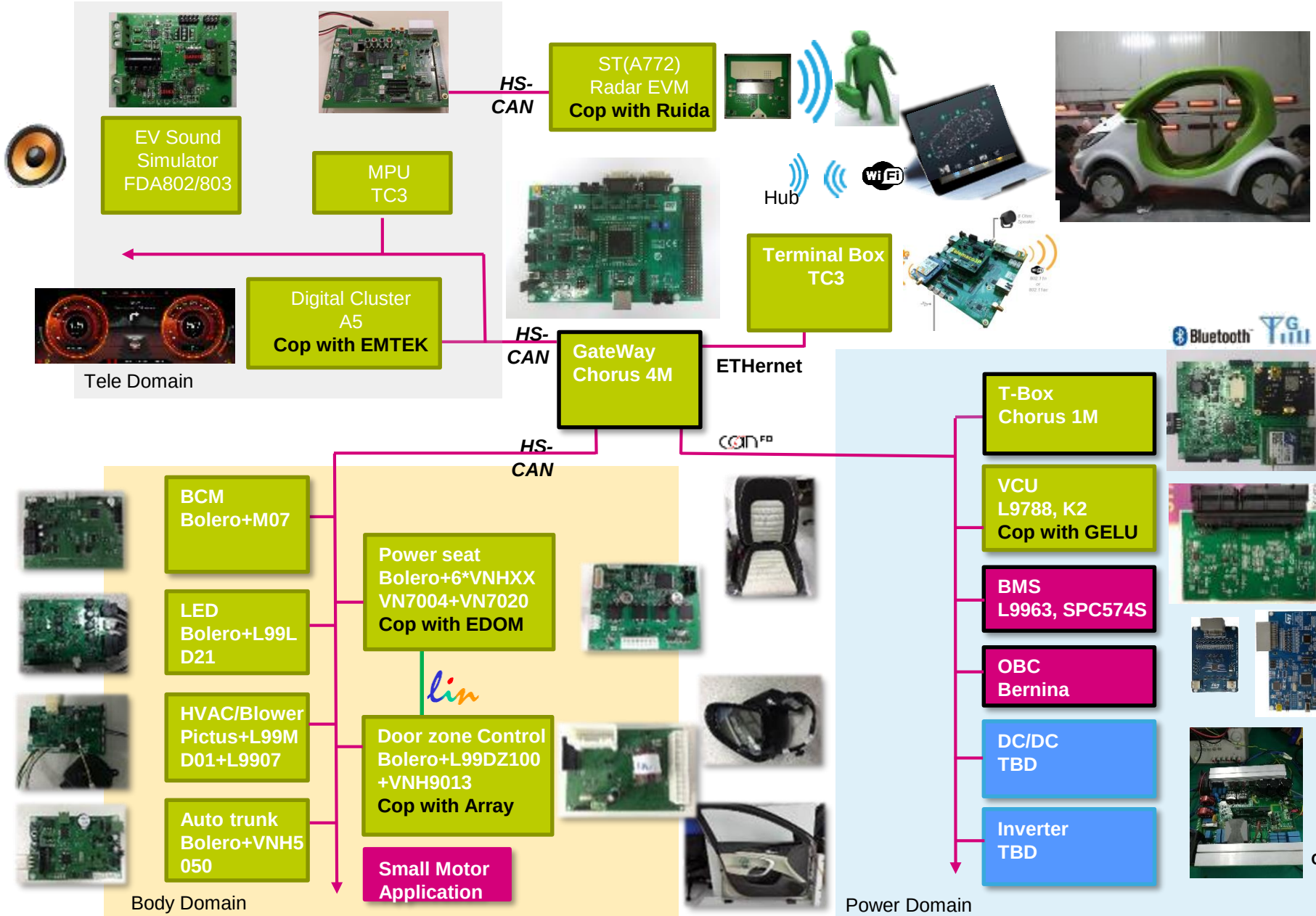
System development
ST Demo Car with Kit Solution



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Cooperation with 3rd party or Disty

Green for available module
Red for module in development
Blue for modules in planning

EHB(Electro-Hydraulic Booster)
(i-booster, c-booster, e-booster)
电动助力刹车系统解决方案 (无刷)

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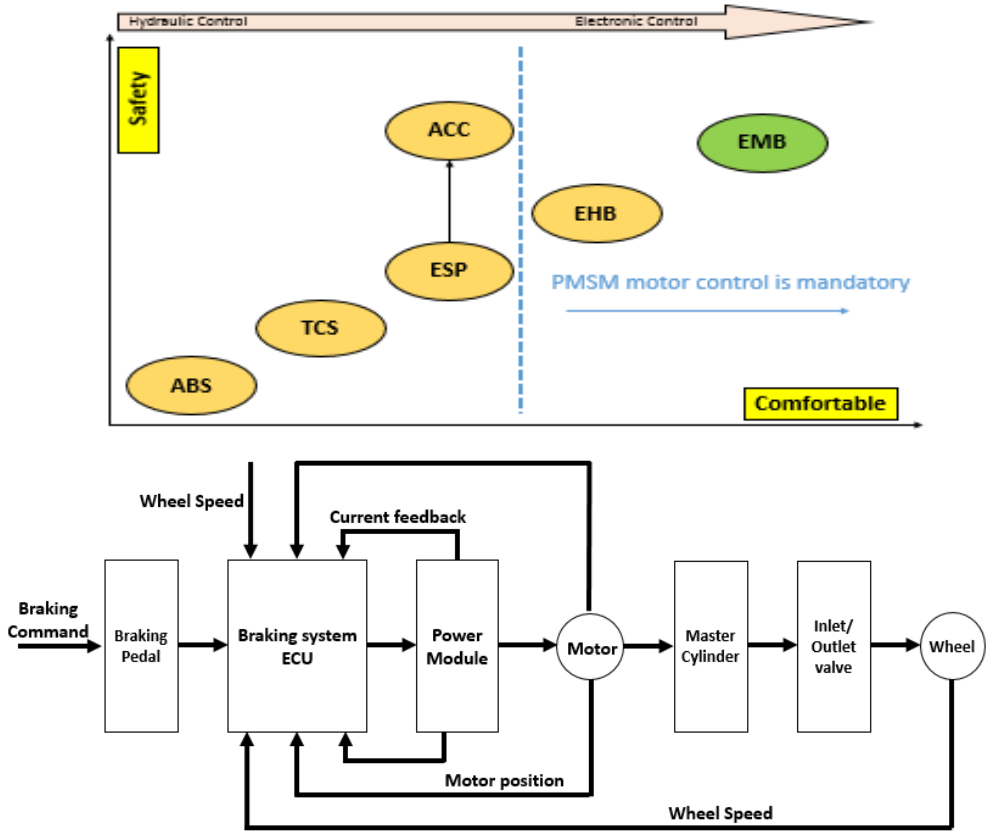
EHB System and Market Overview

EHB/EMB



Why EHB?

- There is no engine supporting a vacuum pump in EV, and no brake signal from pedal for ADAS concept, a brushless motor is mandatory to drive the main cylinder in EHB.
- Only vacuum pump is not needed in i-Booster, original hydraulic system (valve, pipeline, etc) is still kept in EHB.
- EMB is future trend , which use BLDC motor directly connected to mechanical piston for braking with the following advantages:
  - Response time is greatly shortened, from EHB 120ms to EMB 90ms.
  - No hydraulic system, no liquid leakage, which is extremely important for EV.

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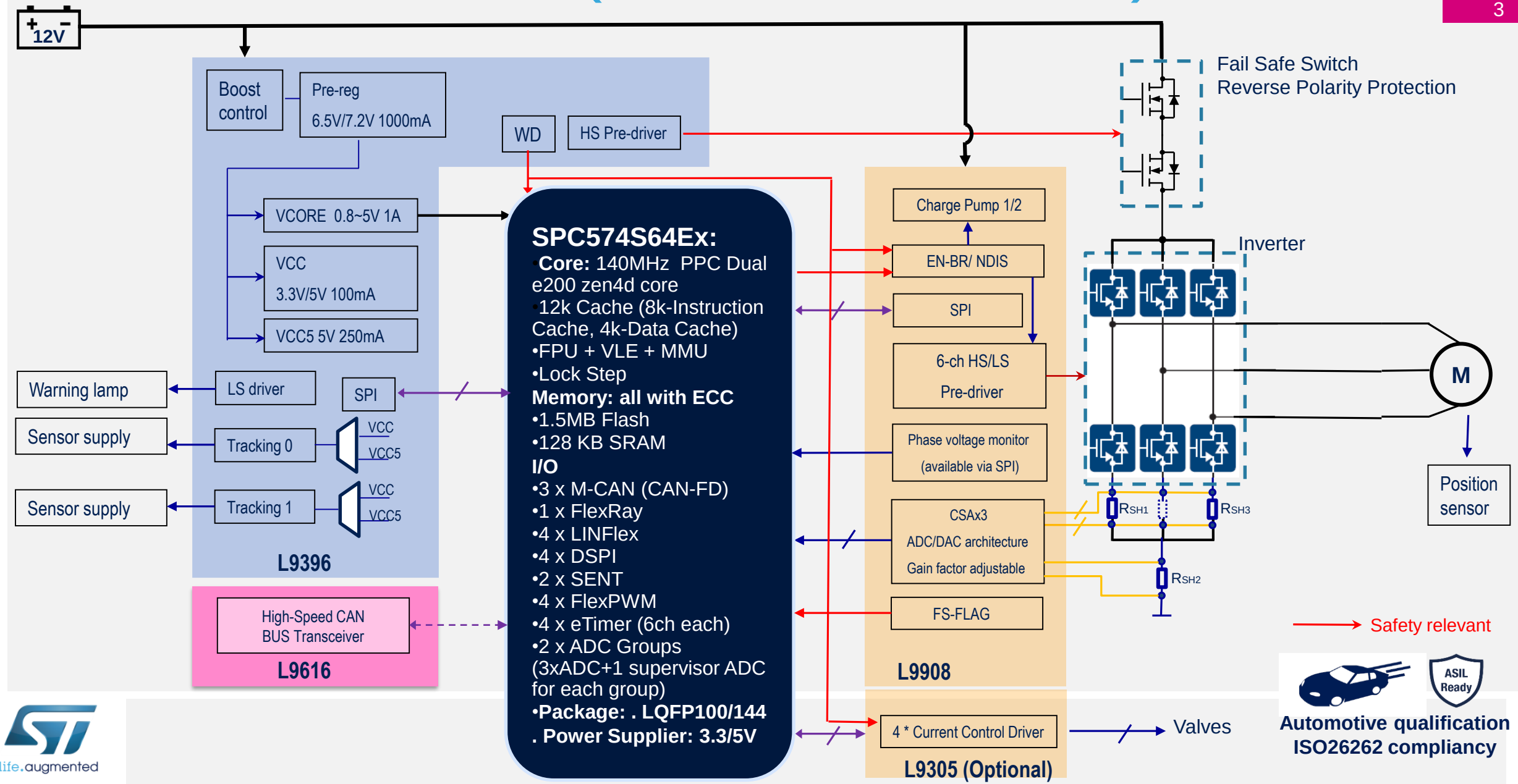
Brushless EHB (i / c / e - Booster) Solution



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Sphaero SPC574S

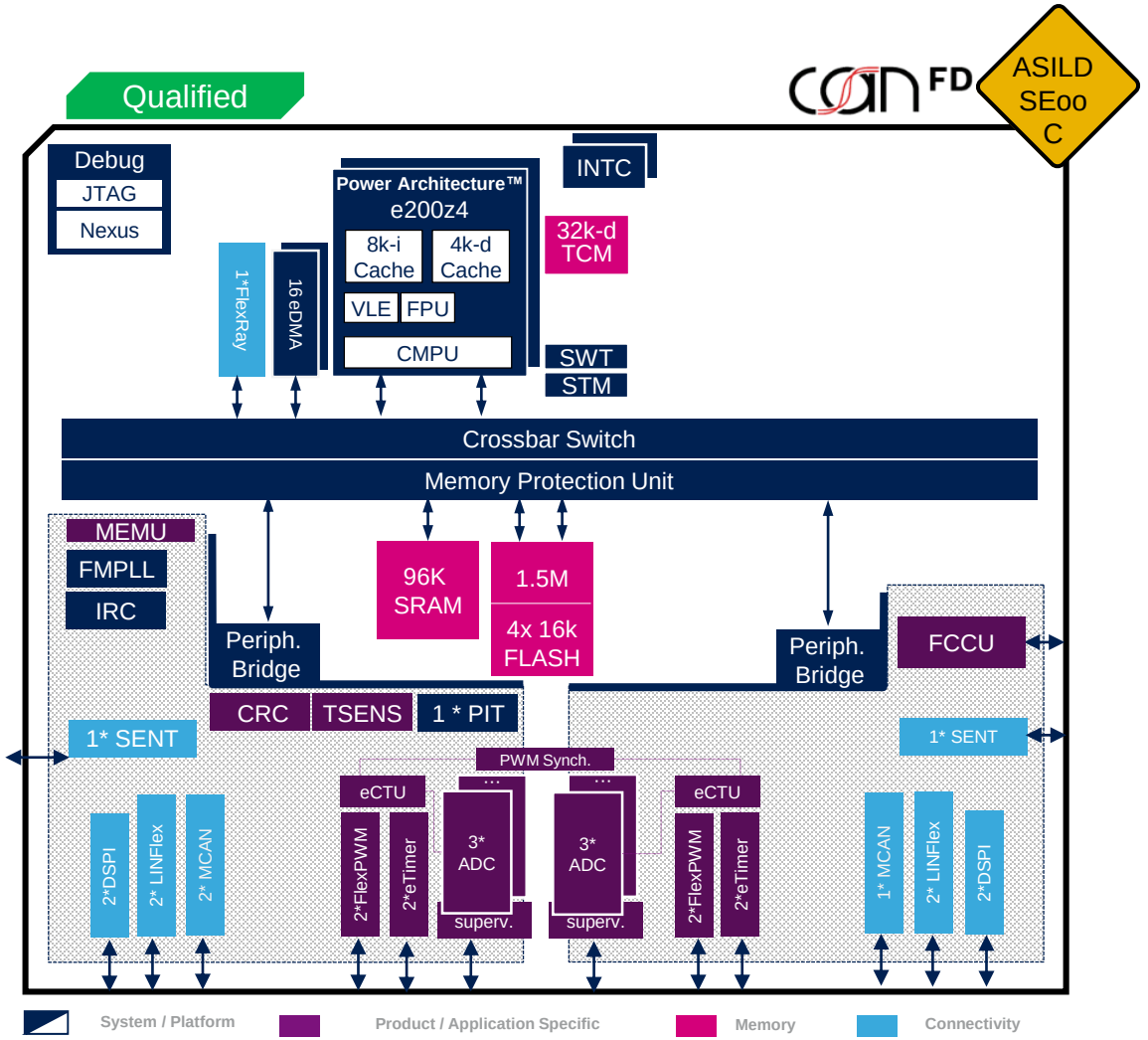
Superset Block Diagram

Core
- Up to 140 MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Dual Issue Core with Floating Point Unit
  - 12k Cache (8k-Instruction Cache, 4k-Data Cache)
  - 32k TCM (32k d-RAM)
- ASILD SEooC *(see technical safety concept)*

Memory
- 1.5Mbyte + 4x16k Flash with ECC *(1 RWW)*
- 128k RAM with ECC (96k SRAM + TCM)
- Crossbar with MPU (8 regions)

I/O
- 1 x FlexRay Dual Channel with 128MB (optional)
- 3 x MCAN with ISO CAN-FD
- 4 x LINFlex *(3x master only)*
- 4 x DSPI
- 2 x SENT (2x3ch overall)
- 2 x FlexPWM (4x3ch each) + 2 x FlexPWM (2x2ch each)
- 4 x eTimer (6ch each)
- ADC – 2x (3+1)x 12Bit, 18/32/33Ch. (on QFP100/144)
  - fast 10Bit conversion & supervisor ADC concept
- 2 x ADC enhanced cross triggering unit (eCTU)

System
- 32Ch eDMA
- CRC Unit
- Fault Collection & Control Unit
- Software watchdog timer (inc. window mode, flow monitoring)
- 3.3V or 5V advanced supply (internal or external logic supply)
- FM-PLL, FlexRay PLL and 16MHz internal RC OSC
- Nexus Class 3+ / JTAG (2 pin or 5 pin)
- 100-144 pins LQFP package (0.5mm pitch)
- -40ºC - + 150ºC Tj



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Sphaero, Next Generation MCU for Safety Critical Applications & 3ph BLDC

Major Enhancements

Safety	
Next generation safety concept	
Enhanced Safety (DMA, Core-peripheral path, peripheral specific e.g. ADC	reduced cost of safety (smarter than just replication (e.g. E2E ECC)
Increased Availability e.g. E2E ECC, MEMU, FCCU	

Advanced & Flexible Supply Concept	
3.3V or 5V device	
Full External Supply or Fully integrated	
Full External Supply for IO and core voltage for best thermal optimization	Fully integrated core voltage generation for optimzed supply and external circuitry
Possibility for up to 4 independant supplies	
One domain per ADC/motor control subsystem	Two further IO domains for rest of the IOs

Advanced 3ph. Motor Control	
Full Dual 3ph BLDC Motor Control	
QFP144	Dual 3ph BLDC motor control
QFP100	Single 3ph BLDC motor control
Highly enhanced ADC subsystem	
Enhanced safety: Supervisor ADCs	Up to 8 ADC for dedicated ADC/phase, simultaneous sampling of all 2x3 phases

Advanced Packaging
High efficiency pinout
advanced QFP technology Exposed pad/power bars/ground rings

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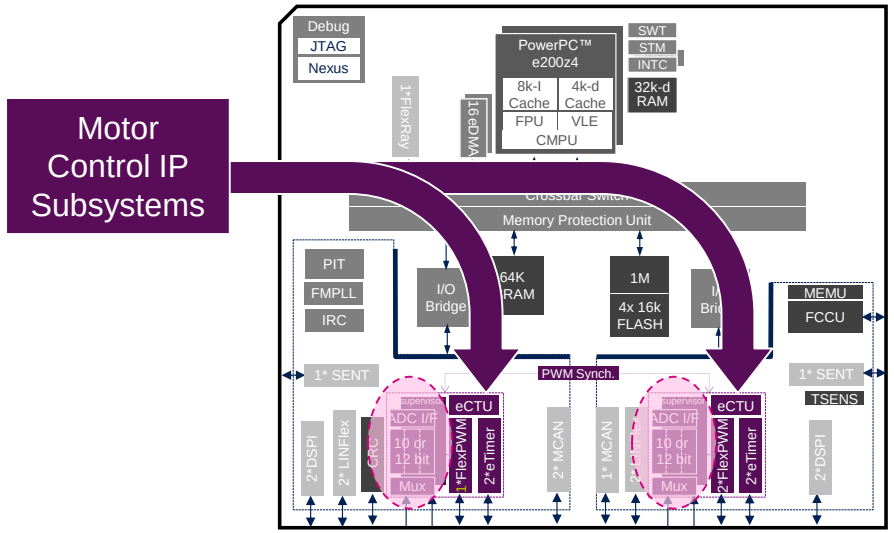
SPC574S (Sphaero)

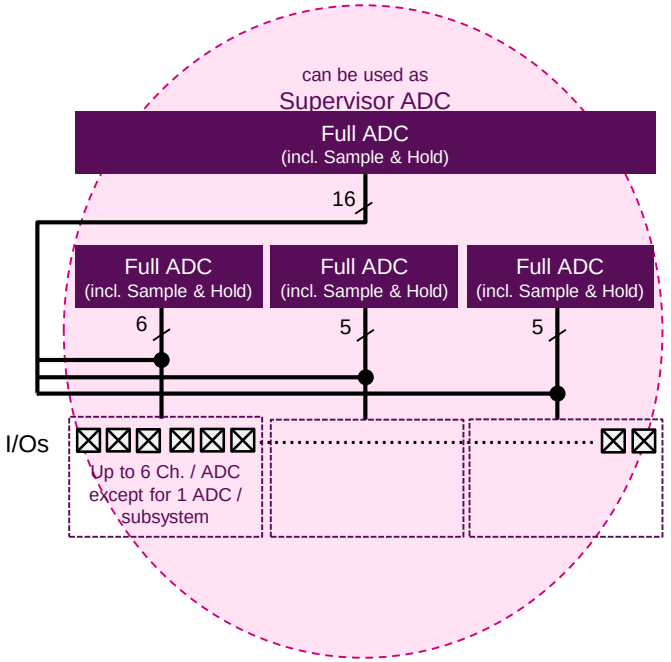
ADC/Motor Control Subsystems



	2x complete & independant Advanced 3ph BLDC Motor Control
ADC	2x full ADCs groups (3 ADC/phase +1 safety supervisor/motor in each group) 18-32ch (QFP100-QFP144)
CTU	2x enhanced CTU
eTimer	4x etimer (6ch each)
FlexPWM	2x FlexPWM (2x 4ch) + 2 FlexPWM (SWG emul.)

ADC Subsystem (present twice per device) optimized for advanced 3ph BLDC motor control

- 8 Full ADCs overall: 1 full ADC per motor phase + additional ADC for safety check (supervisor ADC usage)
- 1.5 µs conversion time at 12 MHz ADC



2x fully replicated and independent motor control subsystems on 2 independant I/O Bridges (with up to 8 simultaneous ADC conversions)

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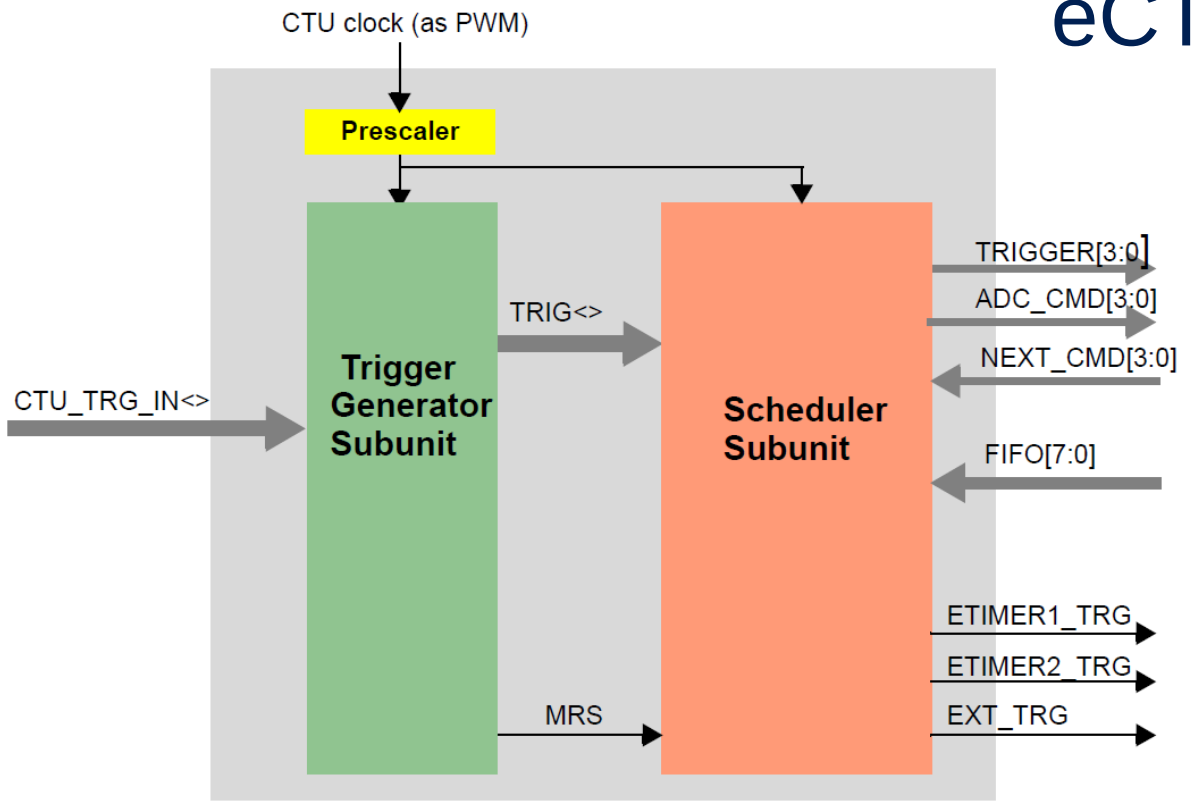
SPC574S (Sphaero)

eCTU/Motor Control Subsystems



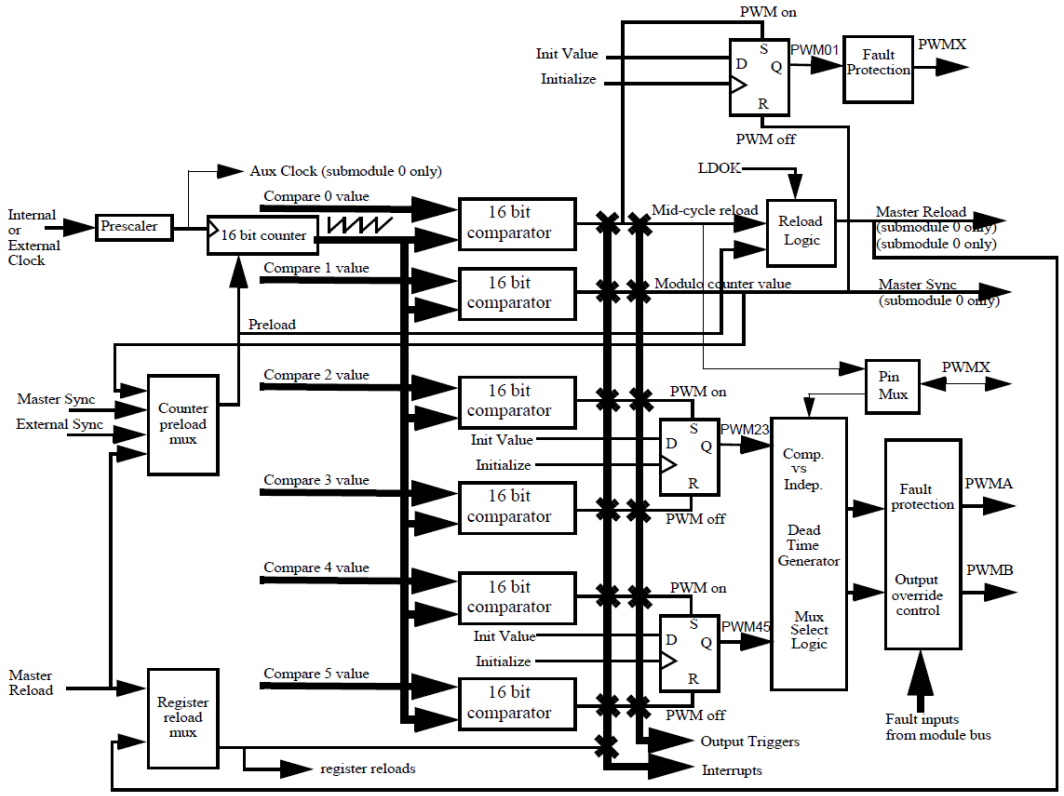
- eCTU makes the ADC sampling Flexible
- Less CPU load in ADC operation
- CRC function helps monitoring the eCTU settings to confirm the integrity

The enhanced CTU contains below features

- Receives up to 8 input trigger events from other IPs such as PWM, Timers, external pins
- Generates up to 8 internal events to trigger ADC sequences
- Support of 4 ADCs
- Each internal trigger event can generate ADC commands to start conversion
- Support of single-mode conversion and multi-mode conversion
- 8 FIFOs to store converted ADC data
- Up to 64 ADC command registers to support various conversion sequences
- Motor function iMonitor using 32-bit CRC

SPC574S (Sphaero)

FlexPWM/Motor Control Subsystems



- Suitable for different kinds of Driver IC
- flexible dead time for safety and efficiency
- flexible form of PWM can be used in specific Motor Control Solution with eCTU (Single shunt for example)
- Enhanced capture can used for Sensors (Hall/Encoder for example)

The FlexPWM contains below features

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWM outputs can operate as complimentary pairs or independent channels
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware
- Independently programmable PWM output polarity
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality

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Sphaero

Optimized for best Performance/MHz

Result in figures

Example: customer production application code benchmark result

+57% application performance increase

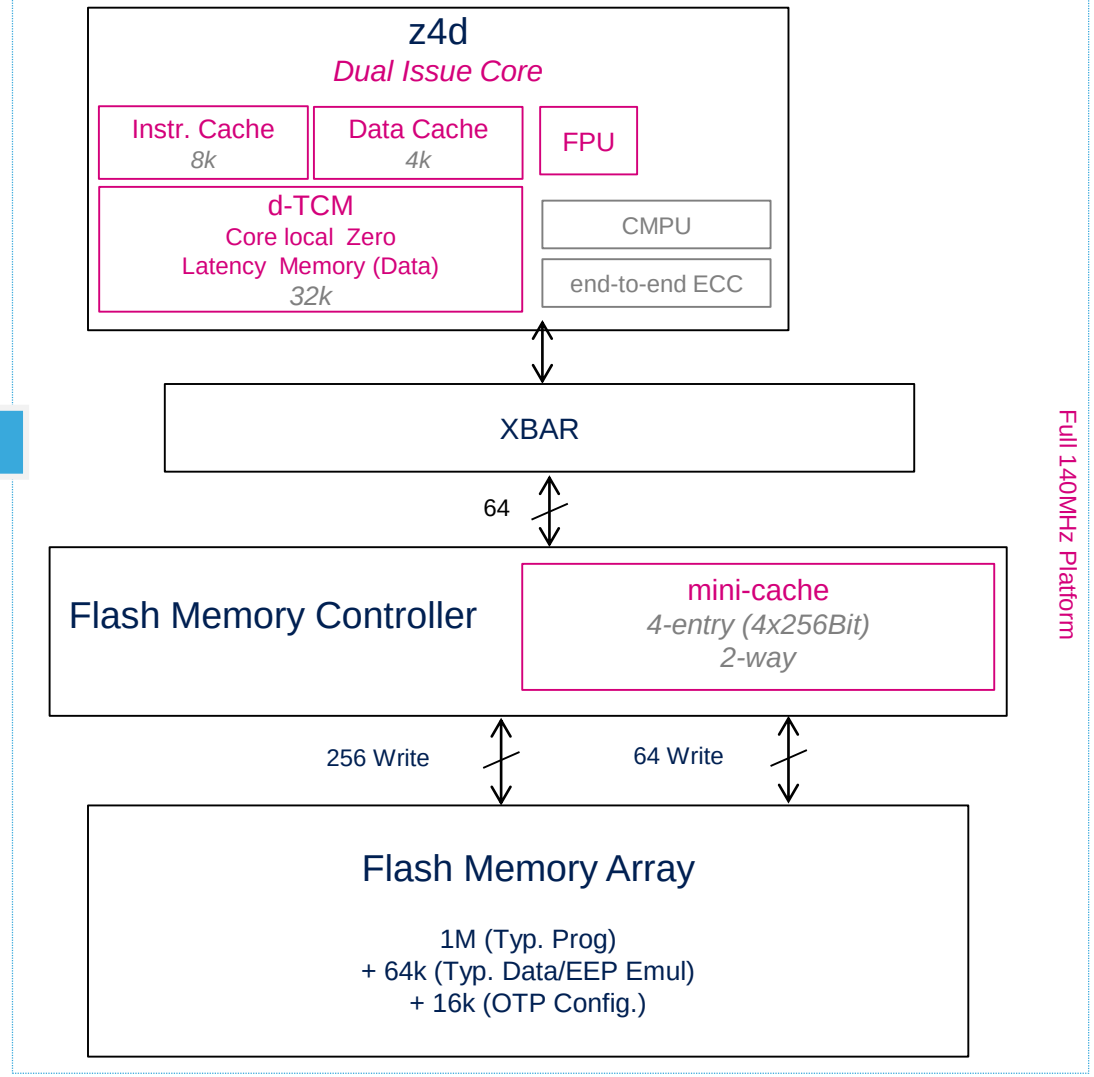
+17% frequency increase

SPC574S Sphaero
140MHz
zen420d core lockstep

less than:
~300mA LV + 50mA HV
FULL use case / 150°C Tj

SPC56EL Leopard
120MHz
zen446 core lockstep

less than:
~380mA LV + 40mA HV
FULL use case / 150°C Tj



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SPC57S Family

Supply Concept Summary

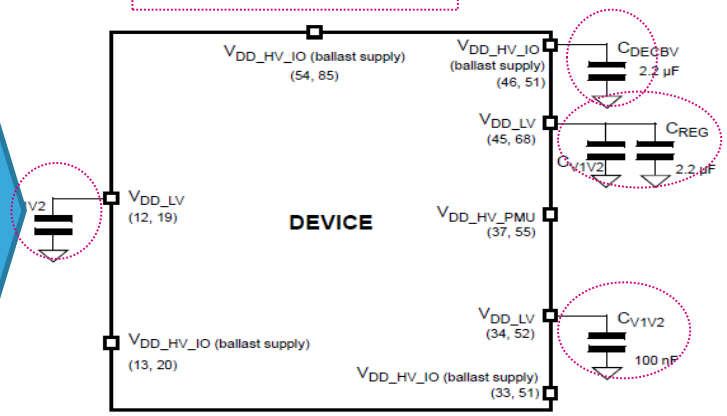
SPC574S only

Supply Modes

User Cost Optimized
Fully Integrated Regulator Mode
- Single 3.3V or 5V external supply
- NO external ballast
- Reduced decoupling capacitor

Optimized for Thermal Performance
External Regulator Mode
- External 3.3V or 5V supply
- External 1.2V supply

Reduced BOM



reduced decoupl. Cap.

SPC574S only

Supply related SEooC features
- On-chip over- & under-voltage monitors on HV & LV

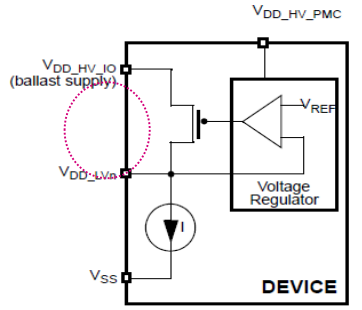
ASILD SEooC

SPC574S only

Advanced Features

Support for mixed 3.3V / 5V Domains
Independant Domains
- Typically 5V ADC and 3.3V IOs

Supply Fault Tolerance
Redundant Supplies
- Reduced funtionality upon fail on one of the reduncant supply



Integrated ballast wo. impacting thermal (ePad)

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Sphaero Start-up Enablement Package

Documents

- Official ST website
  - Reference Manual
  - Data Sheet
  - Technical Note, Application Note
- Training Slides and other FAQs
- Safety Application Guide, FMEDA , DFA, safety assessment report

Software Package

- SPC5 Studio
  - Low level driver
  - Application library and examples
- AUTOSAR
  - MCAL by ST
  - RTE and BSW provided by 3rd parties
- Core self test

Sphaero **EVA Board**

- Sphaero Mother Boards
  - 2 kinds of daughter card

IDE

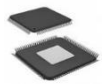
- SPC5 Studio
- HighTec
- GHS
- Wind River

Debug tool

- UDE STK
- Lauterbach Trace 32
- Isystem

In mass production

L9396
System Basis Chip



TQFP64EP

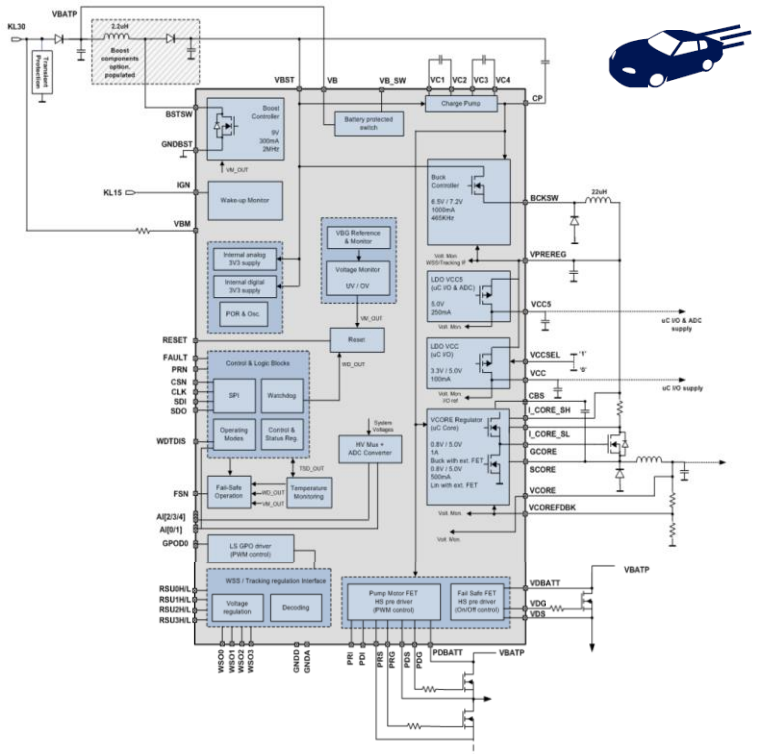
Key Highlight

- Ready for ASIL-D system
- Designed for safety relevant applications
- Flexible solution to 3 configurable voltage rails
- Boost-Buck topology for start-stop systems, cold cranking pulses and weak battery conditions
- BOM selection optimized for output current needs
- Low emission design

Availability

- In production

Block Diagram



Technical information

- Boost Converter, 9V, up to 0.3A - 2MHz with spread spectrum
- Buck Converter, 6.5V/7.2V, up to 1.0A – 465KHz with spread spectrum
- LDO VCC5 (5V +/-2%, 250mA), LDO VCC (3.3V / 5V +/-2%, 100mA), VCORE (0.8V to 5.0V +/-2% - µC core supply, max 1000mA in switching mode, max 750mA in linear mode)
- 4-ch WSS regulated interface / 2 tracking regulators (120mA)
- Integrated 10-bit ADC
- HS pre-drivers for fail safe relay and for motor pump
- Configurable Watchdog (Time-out / Window / Periods) & configurable Fail-Safe Functionality
- Fail-Safe Output (FSN), Wake-up input
- LS general purpose with PWM control
- Voltage monitoring UV/OV on all regulated rails
- Temp. monitoring and Thermal Shutdown
- 32 bit SPI with 3-bit CRC
- AEC Q100 qualified

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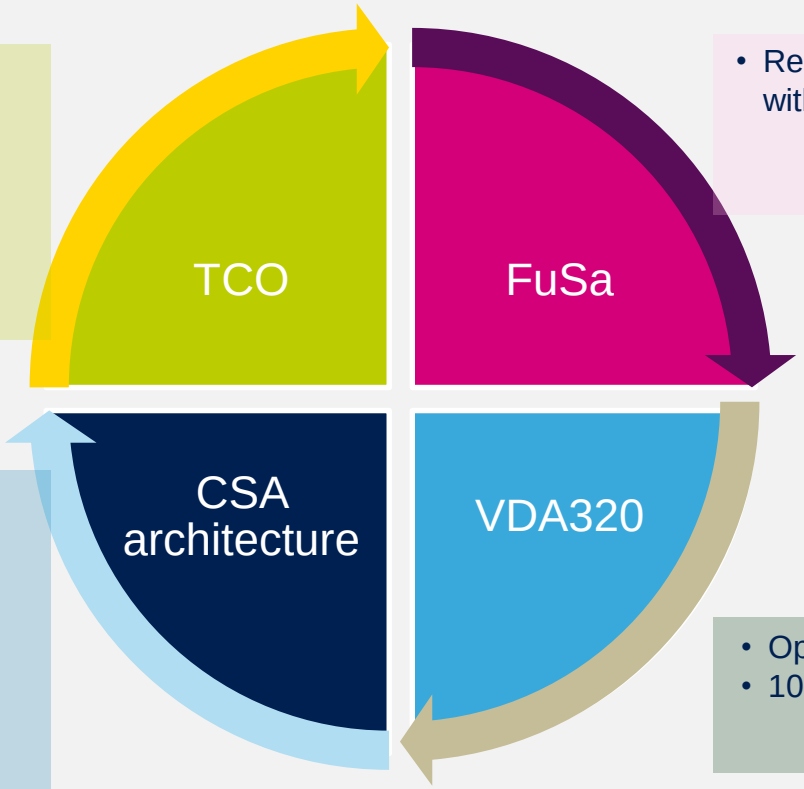
L9908
Brushless Motor Pre-driver IC

Innovation on four major pillars

- TQFP48EP
- Optimized pin count thanks to integrated smart logic for current sensing
- -14V robustness



- Redundant proof concept to achieve ASIL D target without the need to duplicate all ICs in the system

- 3 x integrated CSAs (low side)
- AD2A structure for improved performances vs 2 floating CSAs or standard analog architecture
- Programmable phase current streaming sampling
- Phase current feedback available via SPI

- Operating range up to 75V on motor supply pin
- 100V Power component class

L9908 Supporting Package

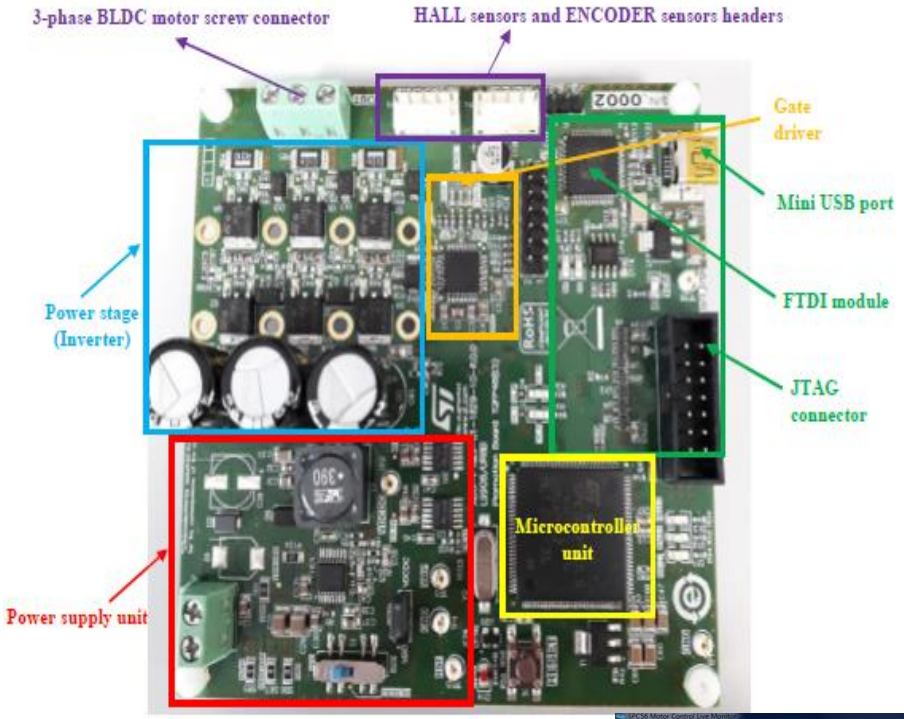
Demo Board/GUI

Demo Board/GUI

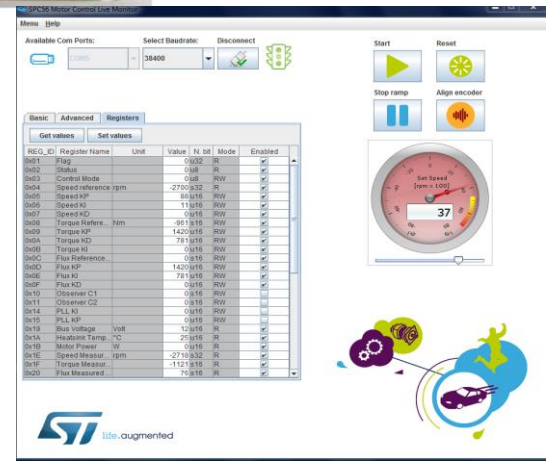
- An environment to build motor control application by using L9908 gate driver :
- Works with 12V, 24V and 48V battery applications
- Low level driver and MCTK for FOC ready
- Demo board GUI ready

Board Features

- Micro
  - As the master in charge of executing and managing the motor control application
  - Used SPC560P50L5, a 32-bit Power Architecture MCU
  - PWM input
  - Configuration and Diagnostic of L9908 via SPI
- Inverter
  - 6 Power Mosfet (STD105N10F7AG N-Channel Power MOS 100 V, 6.8 mOhm typ., 80 A- in DPAK package)
- USB
  - Possibility to use an external USB converter, in order to control the SPI
  - Communication by PC via USB, by jumpers setting.



L9908 promotion board overview



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PSSO36

TQFP48EP

L9305 – Stonemountain

4 Channel Current Controlled Valve Driver

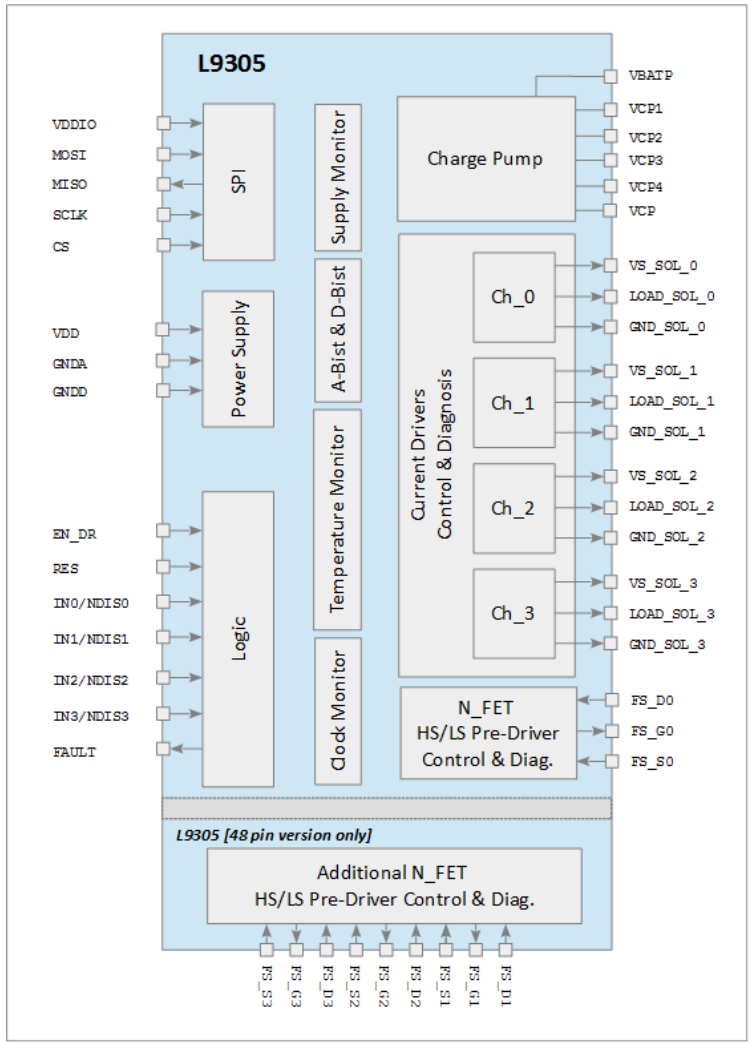
Key Highlight

- 3mA accuracy and Internal sensing I path immune to aging
- No ECU final line calibration needed
- Redundancy of the whole I regulation path
- Real time echo of the regulated current availble on SPI register
- Programmable triangular & square dither
- Full ISO26262 compliant, ASIL-D systems ready

Availability

- In production

Block Diagram



Technical information

- 4 independent LSD/HSD current controlled drivers
  - Integrated Current Sense Path
  - Current Accuracy (in normal range)
    - ± 3mA in 0 to 1.2A range
    - ± 1% in 1.2A to 1.5A range
  - Current Accuracy (in extended range)
    - ± 20mA in 0 to 0.5A range
    - ± 4% in 0.5A to 2A range
  - Max Driver RDSON 400mΩ @ 175 ° C
  - 13 bit Current Set-point Resolution
  - Variable and Fixed Frequency Current Control Algorithm
  - Programmable Dither Function
  - Selectable Driver Slew Rate Control
- 1 or 4 Fail safe pre-drivers with VDS monitoring
- Redundant Safe Enable Path
- Advanced Diagnosis and Monitoring
- Temperature Sensor and Monitoring
- 32 bit SPI (5 bit CRC)

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ST OBC/DCDC Solution Introduction

Jacob LIN

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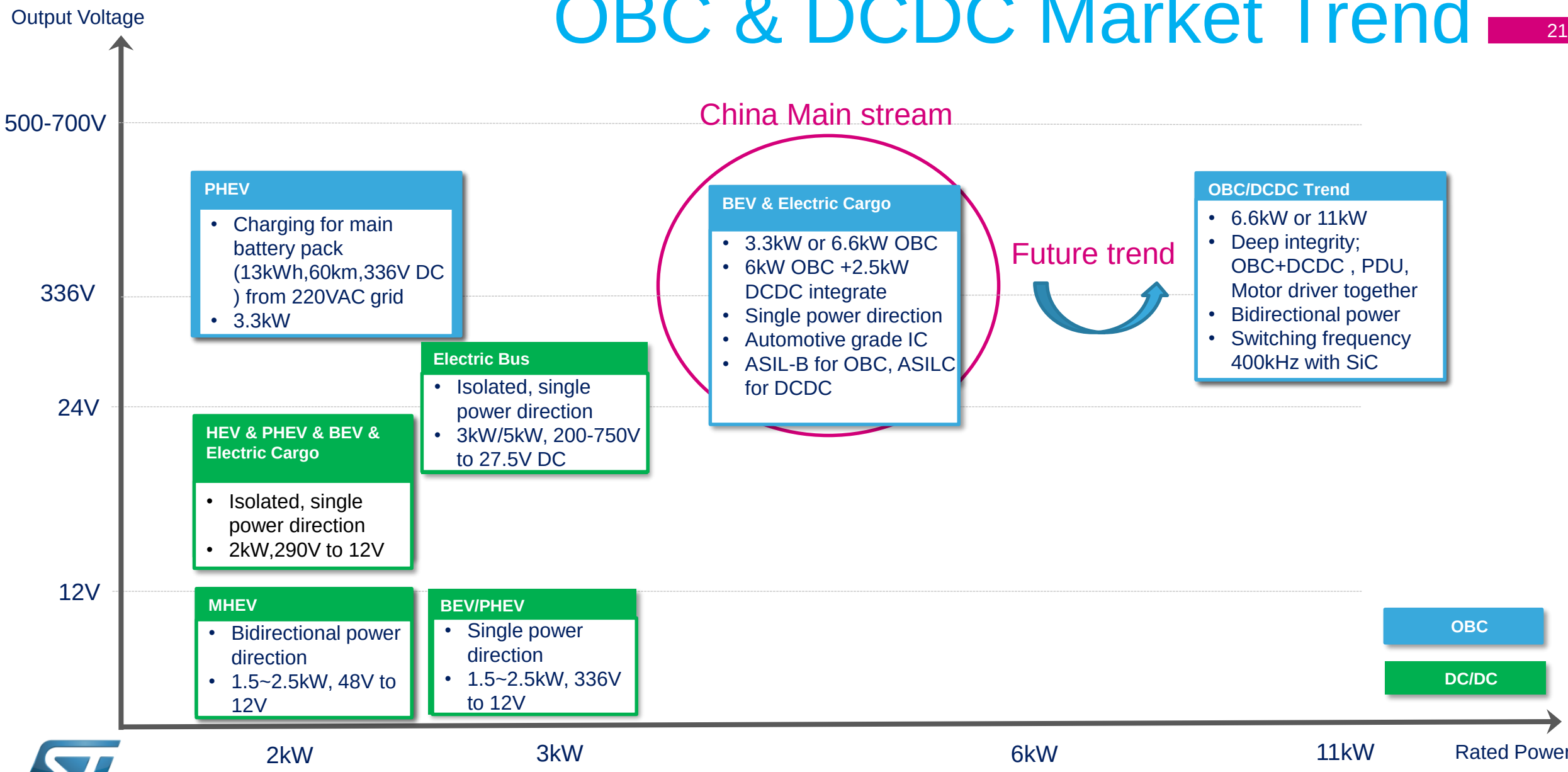
OBC & DCDC Market Trend



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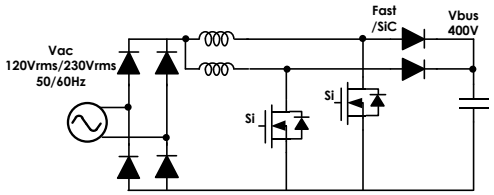
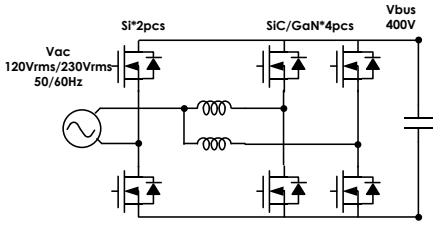
Typical topology for OBC/DCDC

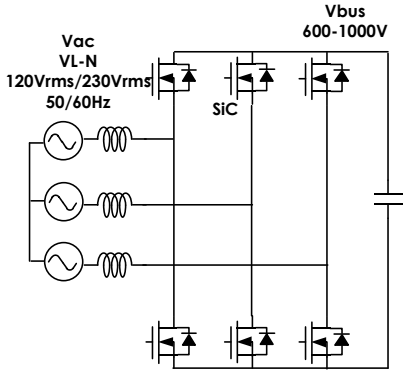
AC-DC topology for OBC



- Diode bridge based PFC
- Single power direction
- 3.3kW/6.6kW typical
- 60~100kHz PWM

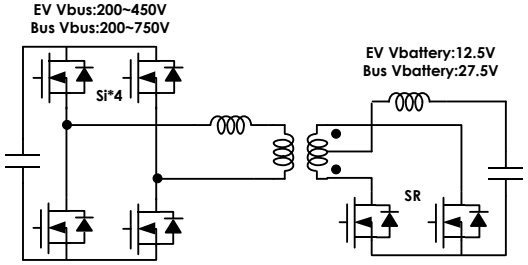


- Totem pole PFC
- Bi-direction power direction
- 3.3kW/6.6kW
- Si 100kHz PWM, SiC/GaN higher

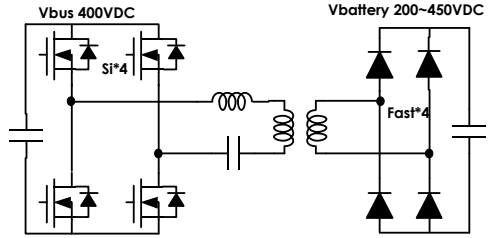


- Three phase PWM PFC
- Bi-direction power direction
- 11kW
- SiC MOSFET, 67~100kHz PWM

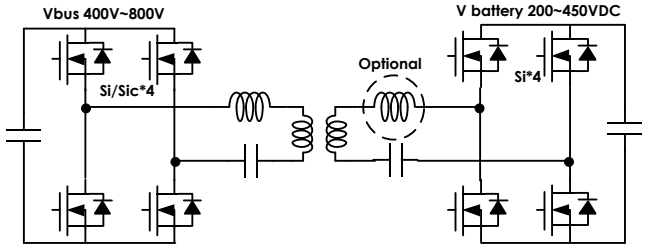
DCDC topology for OBC/DCDC



- Phase shift full bridge PSFB
- Single power direction
- 1.5~2.5kW typical
- 100kHz PWM



- Full bridge LLC
- Single power direction
- 3.3kW/6.6kW
- Si MOSFET, 100~300kHz



- Full bridge CLLC
- Bi-direction power
- 3.3kW/6.6kW
- Si MOSFET, 100~300kHz

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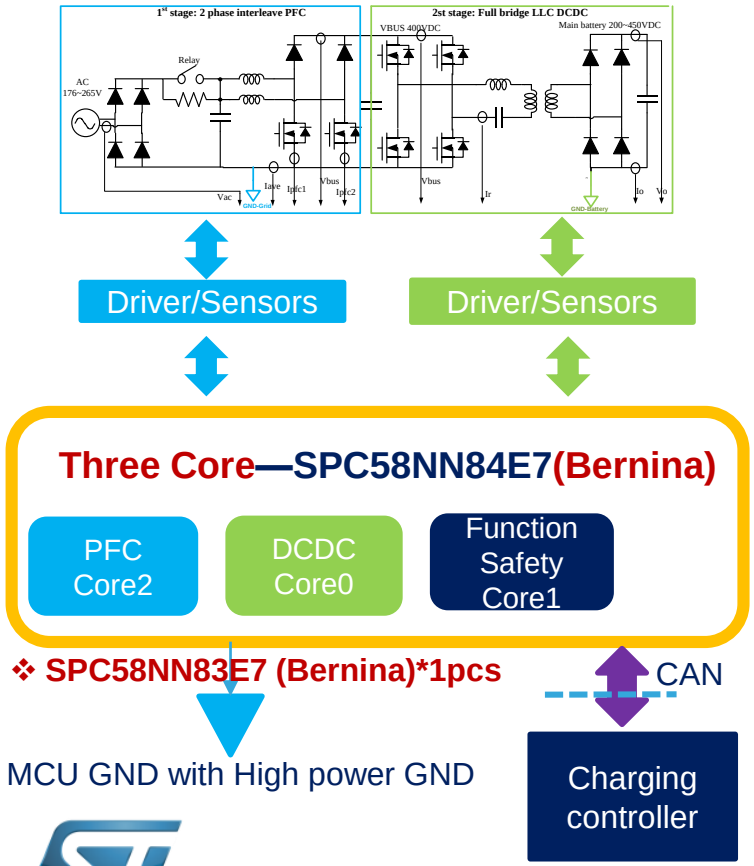
OBC System Solution Proposal

ST **Suggested** OBC solution

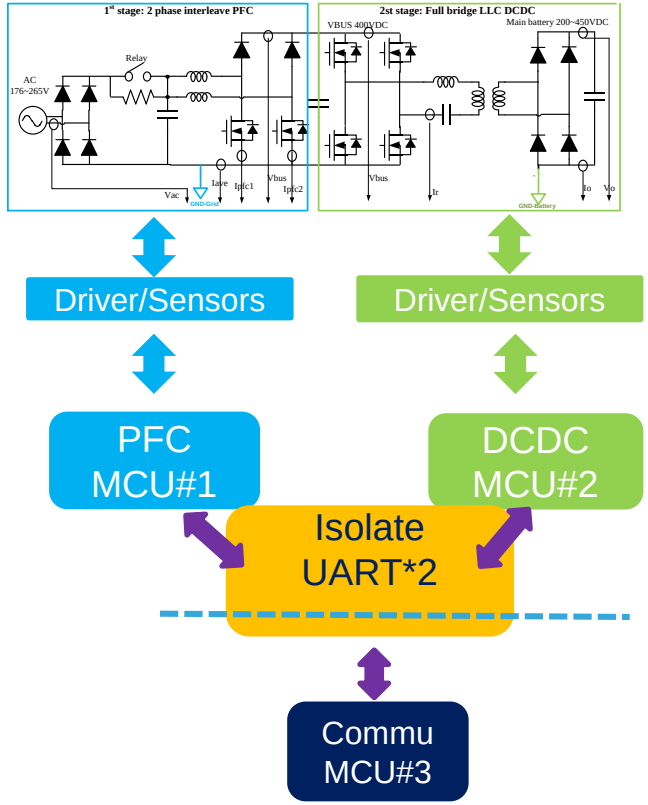
- **One MCU with three core**
  - Core0 for PFC
  - Core1 for DCDC
  - Core2 for Safety/Commu
- **Few** isolated sensors/gate drivers



❖ SPC560Pxx (Pictus)*1pcs

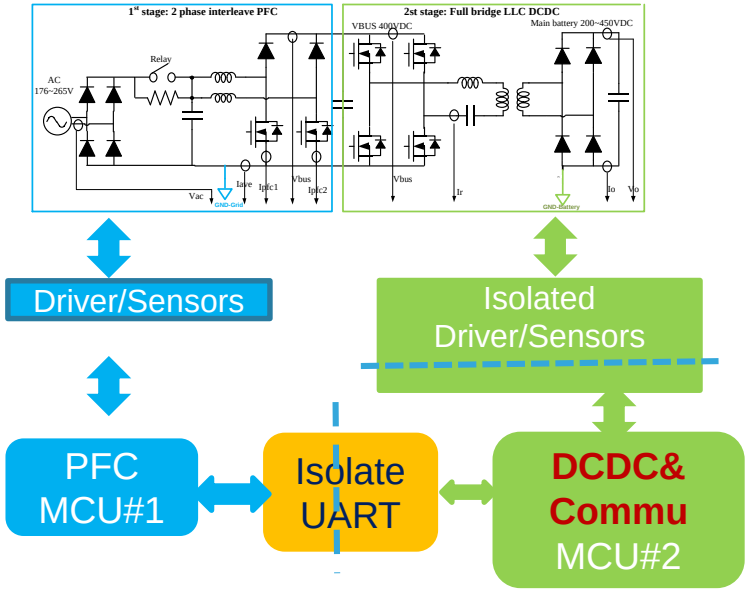
Optional OBC solution1

- **Three independent MCU**
  - MCU1 for PFC
  - MCU2 for DCDC
  - MCU3 for communication
- **Few** isolated sensors/gate drivers



Optional OBC structure2

- **Two independent MCU**
  - MCU1 for PFC
  - MCU2 for DCDC & communication
- **More** isolated sensors/gate drivers



	ST's OBC solution	Competitor's OBC solution1	Competitor's OBC solution2
Frequency	100~300kHz	100~300kHz	100~300kHz
Rated power	3.3kW/6.6kW	3.3kW/6.6kW	3.3kW/6.6kW
MCU	2	3	2
Isolated CAN/UART transceiver	1	2	1
Isolated sensors	2	1	3
Isolated drivers	0	2	2

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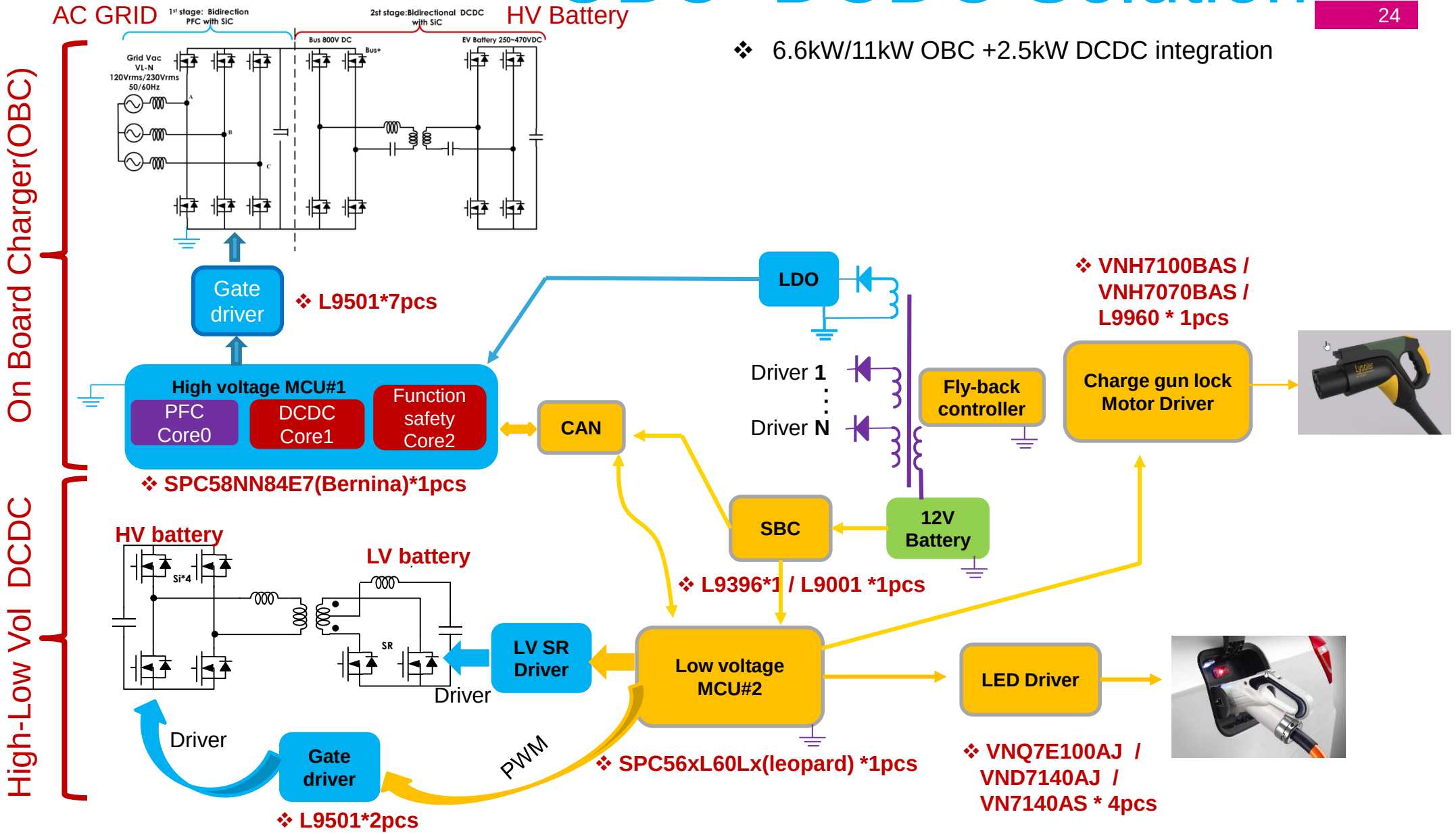
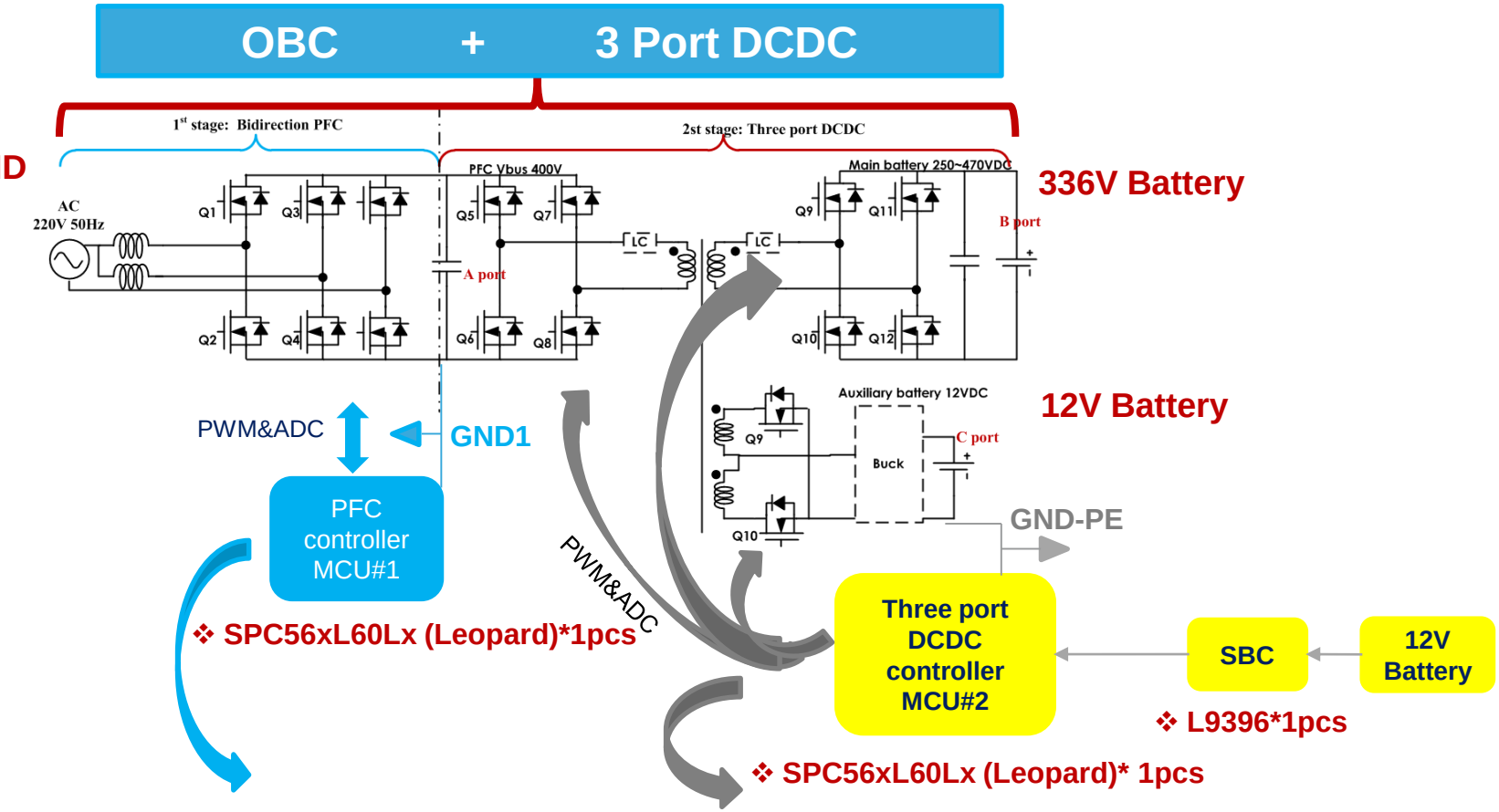
OBC+DCDC Solution

- 6.6kW/11kW OBC +2.5kW DCDC integration



OBC+DCDC Integration Solution Proposal

- A to B:Grid to Vehicle mode(G2V)
- B to A:Vehicle to Grid Mode(V2G)
- B to C:Traction to Vehicle mode(T2A)



- OBC PFC controller
  - AC grid to Battery, G2V mode
  - Battery to AC grid, V2G mode

- Three port DCDC controller
  - Main battery charging DCDC control
  - Auxiliary battery charging DCDC control
  - Battery discharging DCDC control

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Recommended ST MCU's Key Resources

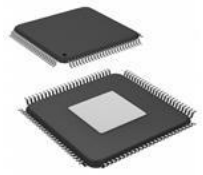
ST PPC MCU family	Safety family			High Performance family
MCU Part No.	SPC560Pxx	SPC56xL60Lx	SPC574SxEx	SPC58NN84E7
Series	Pictus	Leopard	Sphaero	Bernina
Safety	AEC-Q100	ASIL-D	ASIL-D	ASIL-D
Main Core No.& frequency	64MHz*1	120MHz*1	140MHz*1	200MHz*3
FPU	NO	YES	YES	YES
Package	LQFP64/100	LQFP100/144	eTQFP100/144	QFP176/BGA292
ADC module	10bit SARADC*1	2*12bit SAR ADC	8*12 bit SARADC	10bit SARADC*2;12bit SARADC*5
ADC conversion speed	1us/ch	1us/ch	1us/ch	1.18us/ch
PWM module	2xFlexPWM	2xFlexPWM	4x FlexPWM (12ch)	GTMV3
PWM clock	120MHz	120MHz	120MHz	200MHz
Dead time/phase shift hardware module	Yes	Yes	Yes	Yes
PWM resolution	0.083%/100kHz; 0.21%/250kHz	0.083%/100kHz; 0.21%/250kHz	0.083%/100kHz; 0.21%/250kHz	0.05%/100kHz; 0.125%/250kHz
CAN/CANFD	2xFlexCAN	2xFlexCAN	3xCAN-FD	7*CAN-FD
Flash memory	256KB/512KB	768kB/1MB	1M/1.5MB	6MB

Automotive Multiple Power Supply IC

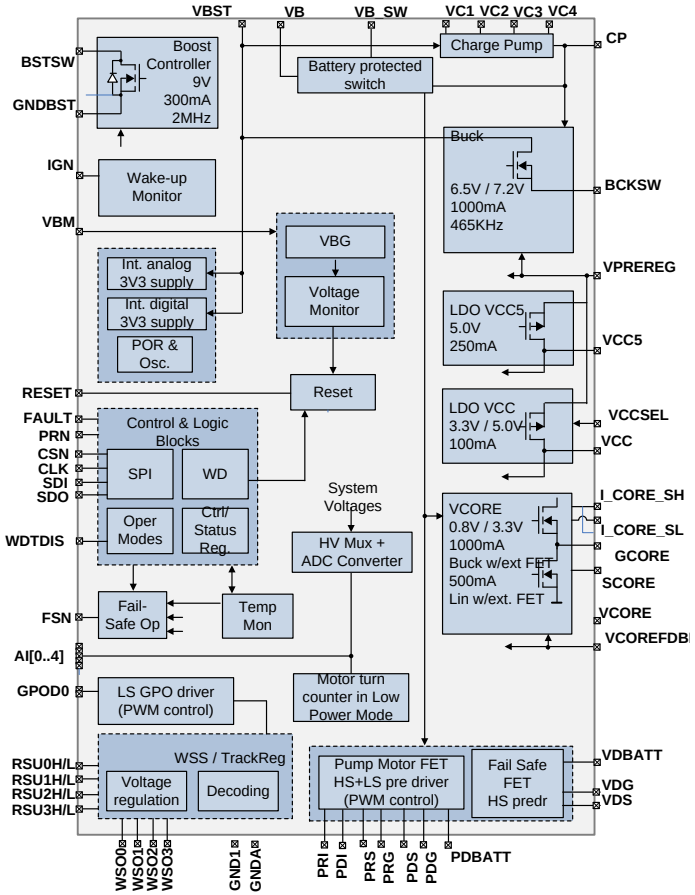
SBC L9396

Technical information

- Boost Converter, 9V, up to 0.3A - 2MHz with spread spectrum
- Buck Converter, 6.5V/7.2V, up to 1.0A – 465KHz with spread spectrum
- LDO VCC5 (5V +/-2%, 250mA), LDO VCC (3.3V / 5V +/-2%, 100mA), VCORE (0.8V / 3.3V +/-2% - µC core supply, max 1000mA in switching mode, max 500mA in linear mode)
- 4 WSS regulated interface /2 tracking regulators (120mA)
- Integrated 10-bit ADC
- HS pre-drivers for fail safe relay and for motor pump
- Configurable Watchdog (Time-out / Window / Periods) & configurable Fail-Safe Functionality
- Fail-Safe Output (FSN), Wake-up input
- Voltage monitoring UV/OV on all regulated rails
- Temp. monitoring and Thermal Shutdown



TQFP64EP



Timing information

- Commercial samples : available
- In production

Key Value

- Designed for **ISO26262 compliance**
- **Flexible solution** to 3 configurable voltage rails
- Boost - Buck topology for low battery functionality for **Start/Stop systems**
- **BOM** selection **optimized** on output current needs
- **Low emission** design

- ☑ *Application Note*
- ☑ *Demo board w/ GUI*
- ☑ *Safety Manual*
- ☑ *FMEDA / DFA*

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ST Motor Control Ics for DC Motor

VIPower™ VNH Family

Under Development

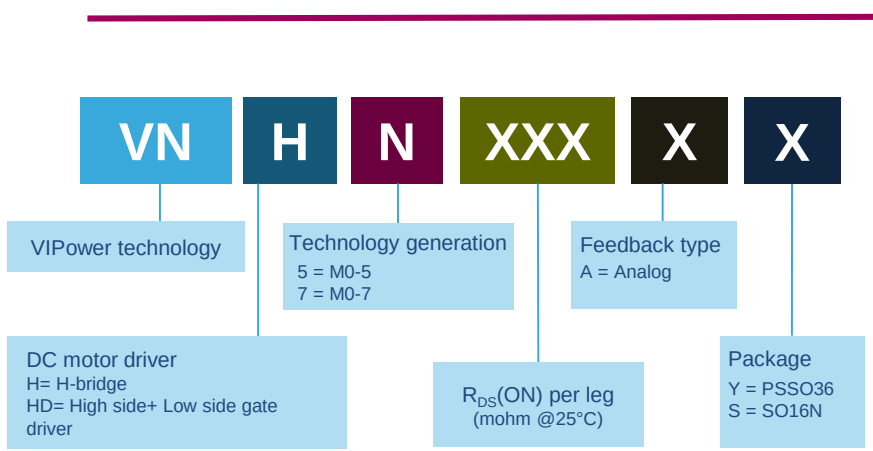
* Power stage only

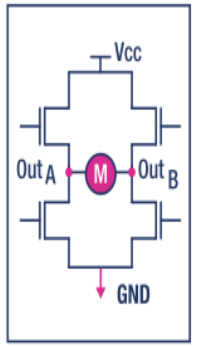
1. Indicator lighting:

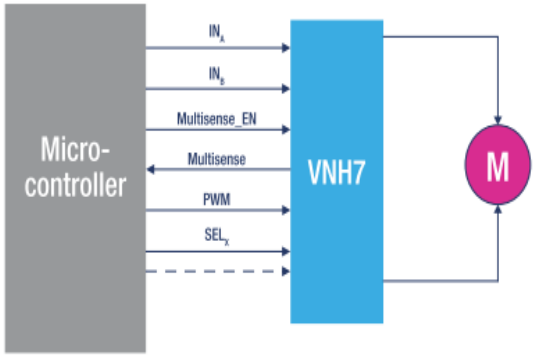
VNQ7E100AJ / VND7140AJ / VN7140AS

2.E-Lock:

VNH7100BASTR / VNH5200ASTR-E / VNH7070BAS







Typical application diagram

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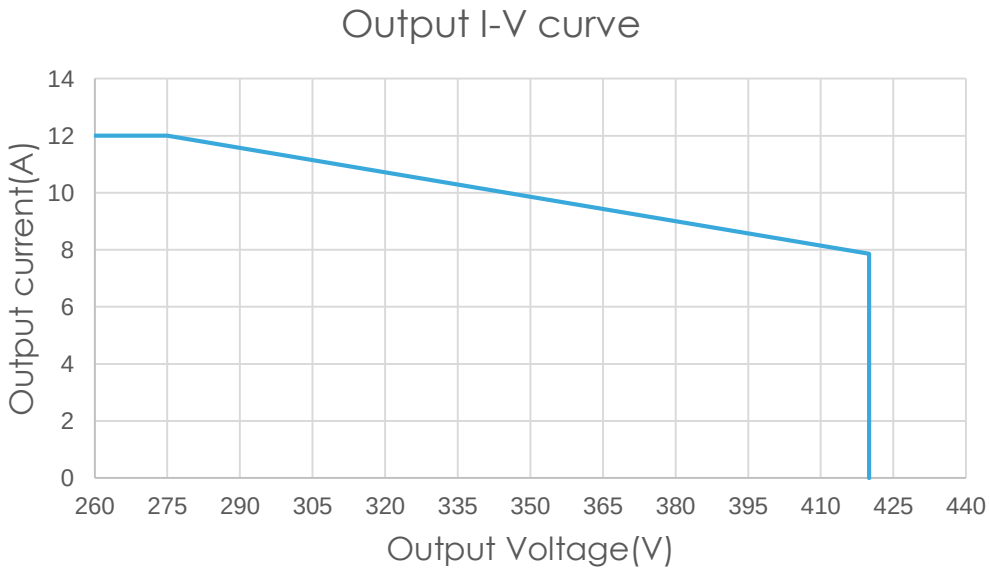
3.3kW OBC DEMO based on SPC58NN84E7

OBC DEMO technical specify

Input Voltage	176~264V AC 50Hz@220V
PFC output voltage	390~410VDC @400VDC
Power factor	>0.98@Rated power,220VAC
LLC output voltage	260~420VDC@320VDC
LLC output current	0~12.5A@10.3A
Rated output power	0-3.3kW@3.3kW
PFC stage efficiency	>98%@Rated point
LLC stage efficiency	>98@Rated point
Overall efficiency	>96%@Rated point
Operating mode	Constant voltage/current
PFC frequency	60kHz
DCDC frequency	**100-250kHz(140kHz)**
Protection	software/hardware
Communication	CAN
Operating Temp	-40 to 85 ℃
Output Current ripple	<5%
Output Voltage ripple	<1%
Cooling method	forced air cooling

DEMO output curve



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3.3kW OBC Demo Test Image

PFC stage

Controller:

- **SPC58NN84E7*1pcs**
- **ASIL-D**
- **200MHz core*3**

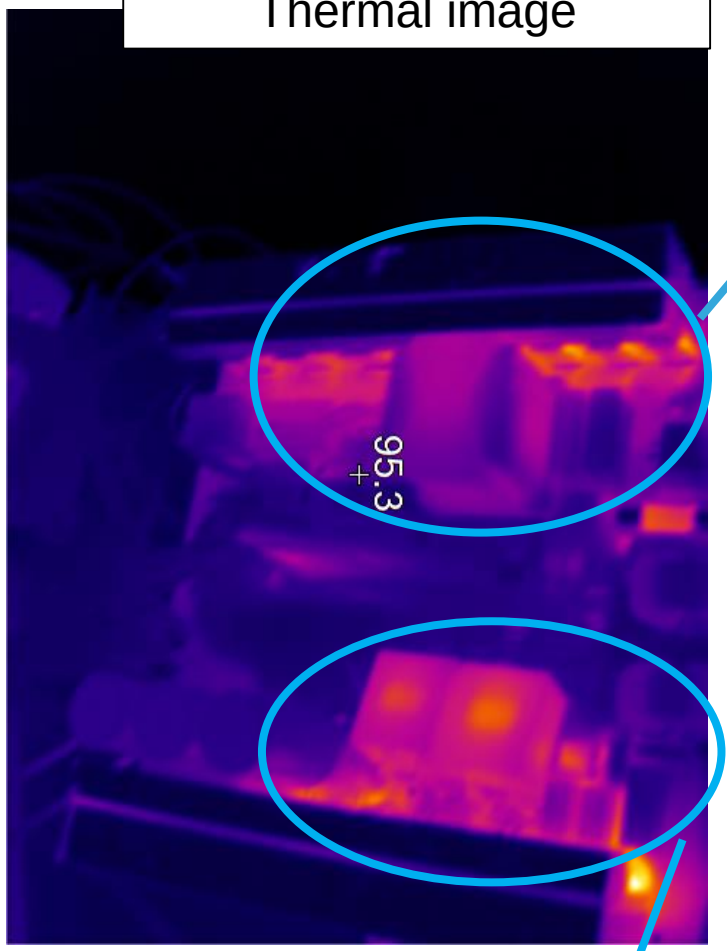
DCDC stage

Main parameter

- AC input:176~265VAC
- Bus voltage:390~410VDC
- Battery voltage:260-420V
- Rated power:3.3kW
- Long*width*height=250*250*55mm

3.3kW OBC demo image

Thermal image



DCDC Thermal Image

PFC Thermal Image

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ST BMS Solution in Electric Vehicle

Fred DING

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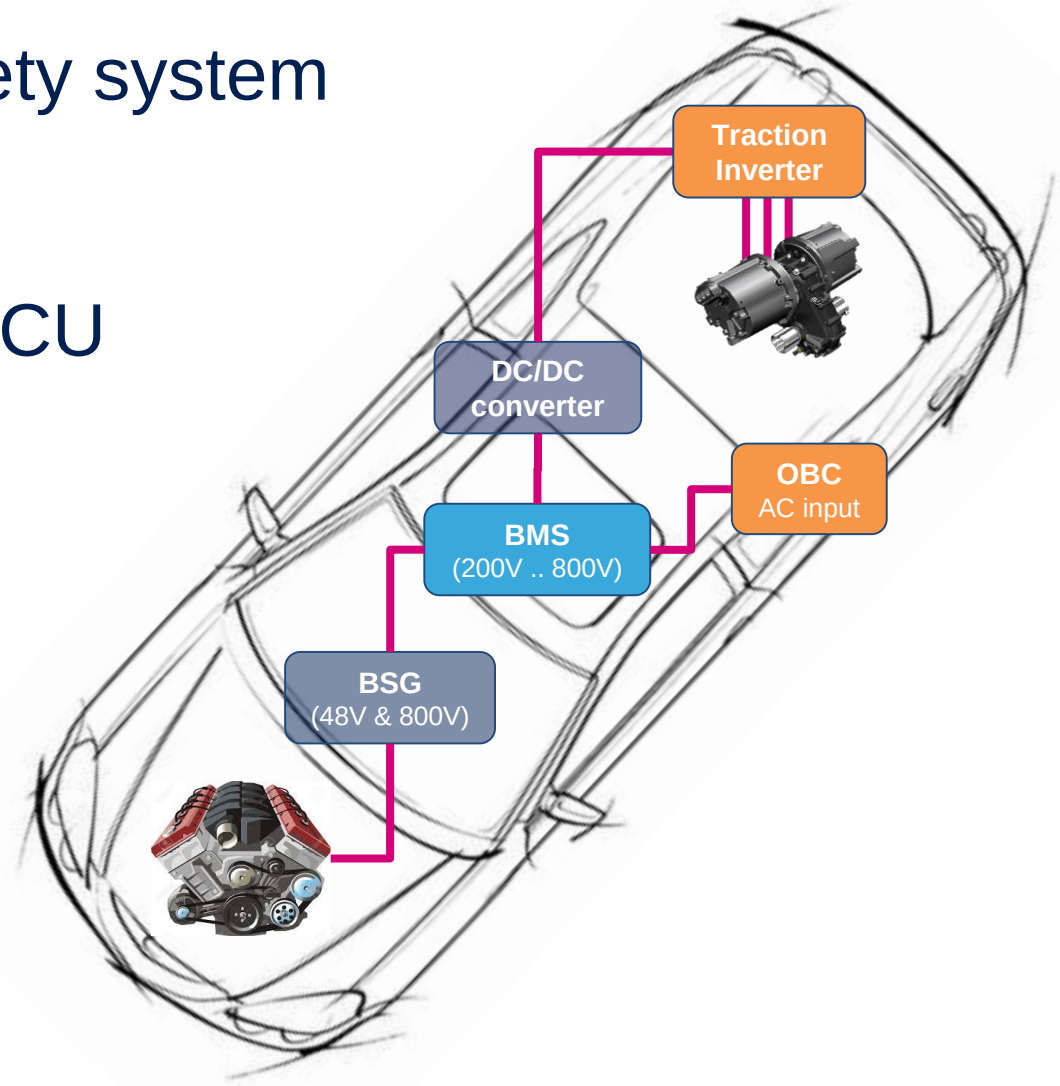
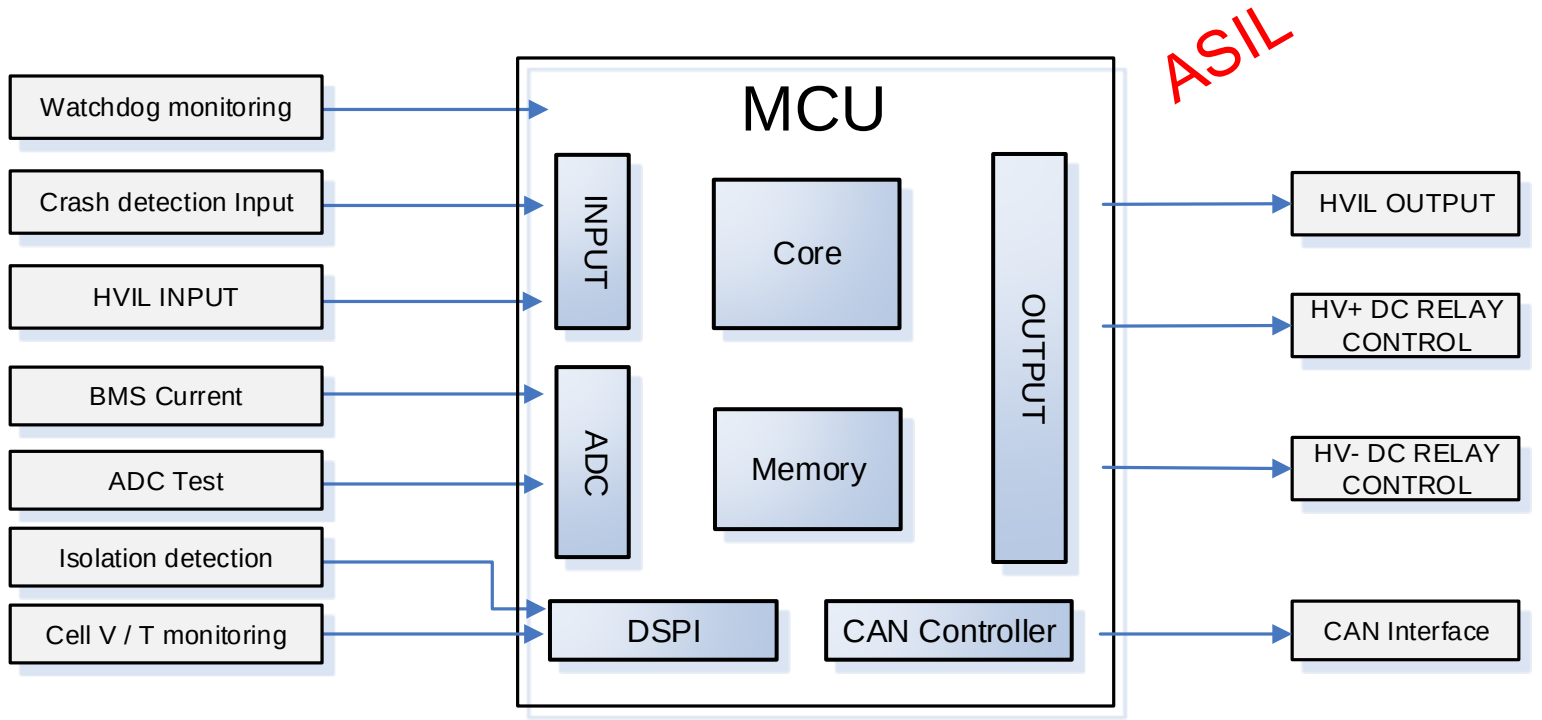
Automotive Battery Management System Trend

- High reliability and functional safety system
- Part of function integration with VCU



BMS - Functional Safety System

- BMS Hardware Safety Architecture
  - Input
  - Output
  - Monitoring
- Microcontroller is the key system element for implementing and fulfilling the ASIL oriented BMS system requirement.



ASIL-D MCU for Safety Critical Applications

Safety

Next generation safety concept

Enhanced Safety (DMA, Core-peripheral path, peripheral specific e.g. ADC	reduced cost of safety (smarter than just replication (e.g. E2E ECC)

Increased Availability

e.g. E2E ECC, MEMU, FCCU

Highly enhanced ADC subsystem

Cross Triggering Unit - automomous PWM/ADC gen.

Enh'd safety: Supervisor ADCs	Up to 8ADC for dedicated ADC/phase, simultaneous sampling of all 2x3 phases

Optimized Supply Concept

Fully integrated (Single 3.3V or 5V supply)

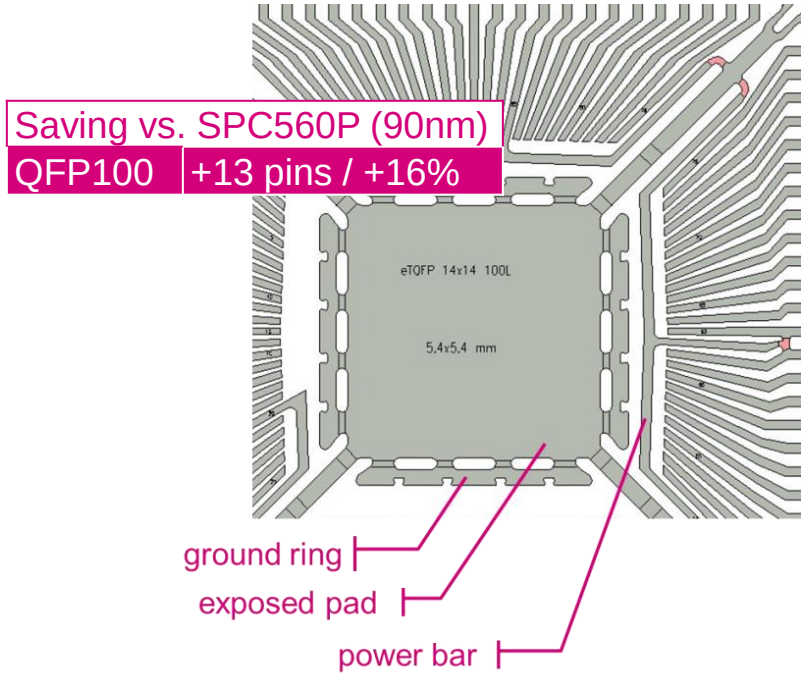
Optimized for User – Min. external circuitry

No external ballast transistor

Advanced Packaging

High efficiency pinout

Advanced QFP technology
Exposed pad/power bars/ground rings



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Sphaero SPC574S

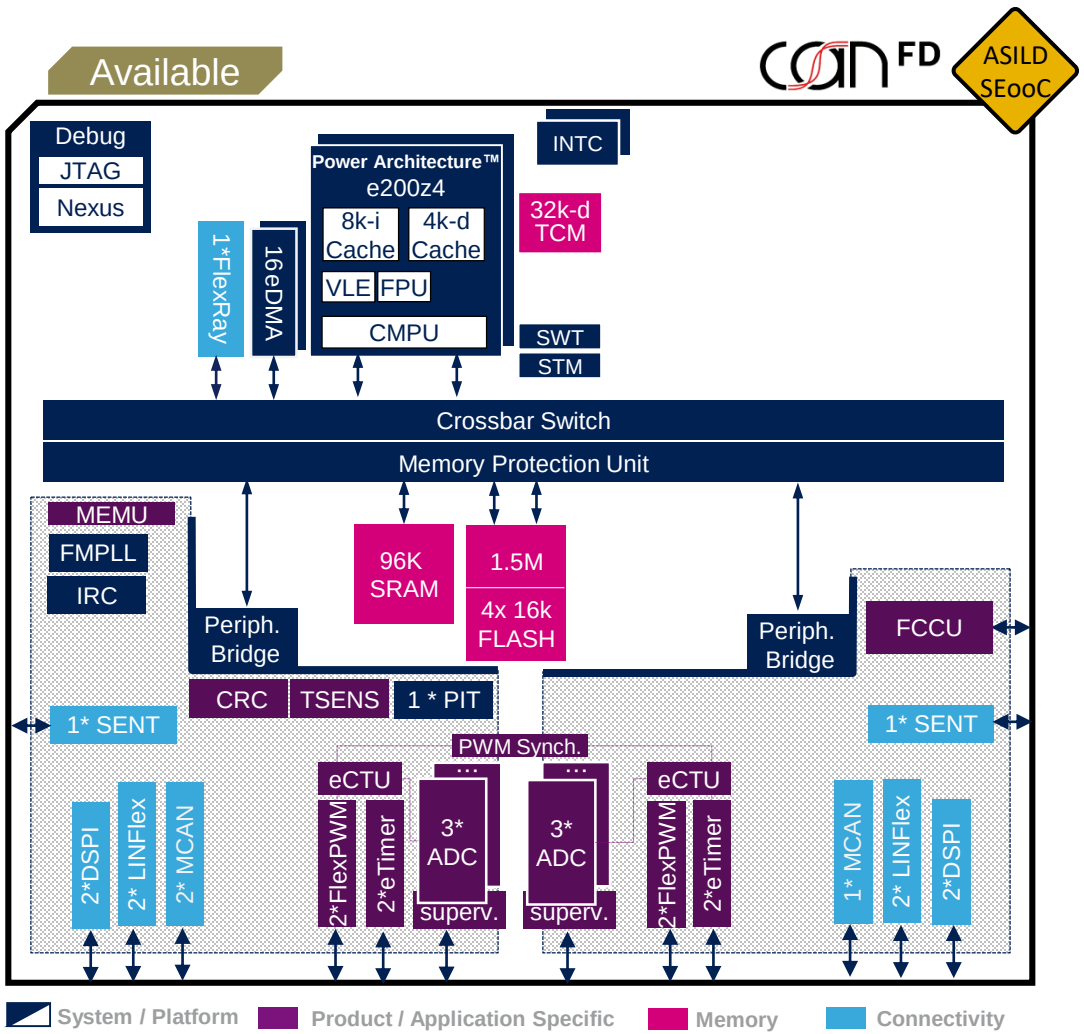
Superset Block Diagram

Core
- Up to 140 MHz Power Architecture™ ISA e200z4 Core (VLE)
  - Dual Issue Core with Floating Point Unit
  - 12k Cache (8k-Instruction Cache, 4k-Data Cache)
  - 32k TCM (32k d-RAM)
- ASILD SEooC *(see technical safety concept)*

Memory
- 1.5Mbyte + 4x16k Flash with ECC *(1 RWW)*
- 128k RAM with ECC (96k SRAM + TCM)
- Crossbar with MPU (16 regions)

I/O
- 1 x FlexRay Dual Channel with 128MB (optional)
- 3x MCAN *with ISO CAN-FD*
- 4 x LINFlex *(3x master only)*
- 4 x DSPI
- 2 x SENT (2x3ch overall)
- 2 x FlexPWM (4x3ch each) + 2 x FlexPWM (2ch each)
- 4 x eTimer (6ch each)
- ADC – 2x (3+1)x 12Bit, 18/32/33Ch. (on QFP100/144/BGA)
  - fast 10Bit conversion & supervisor ADC concept
- 2 x ADC enh´d cross triggering unit (eCTU)

System
- 16Ch eDMA
- CRC Unit
- Fault Collection & Control Unit
- 8 channel PIT
- Software watchdog timer (inc. window mode, flow monitoring)
- 3.3V or 5V advanced supply (internal or external logic supply)
- FM-PLL, FlexRay PLL and 16MHz internal RC OSC
- Nexus Class 3+ / JTAG (2 pin or 5 pin)
- 100-144 pins LQFP package (0.5mm pitch)
- -40ºC - + 150ºC Tj



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Velvety SPC570S

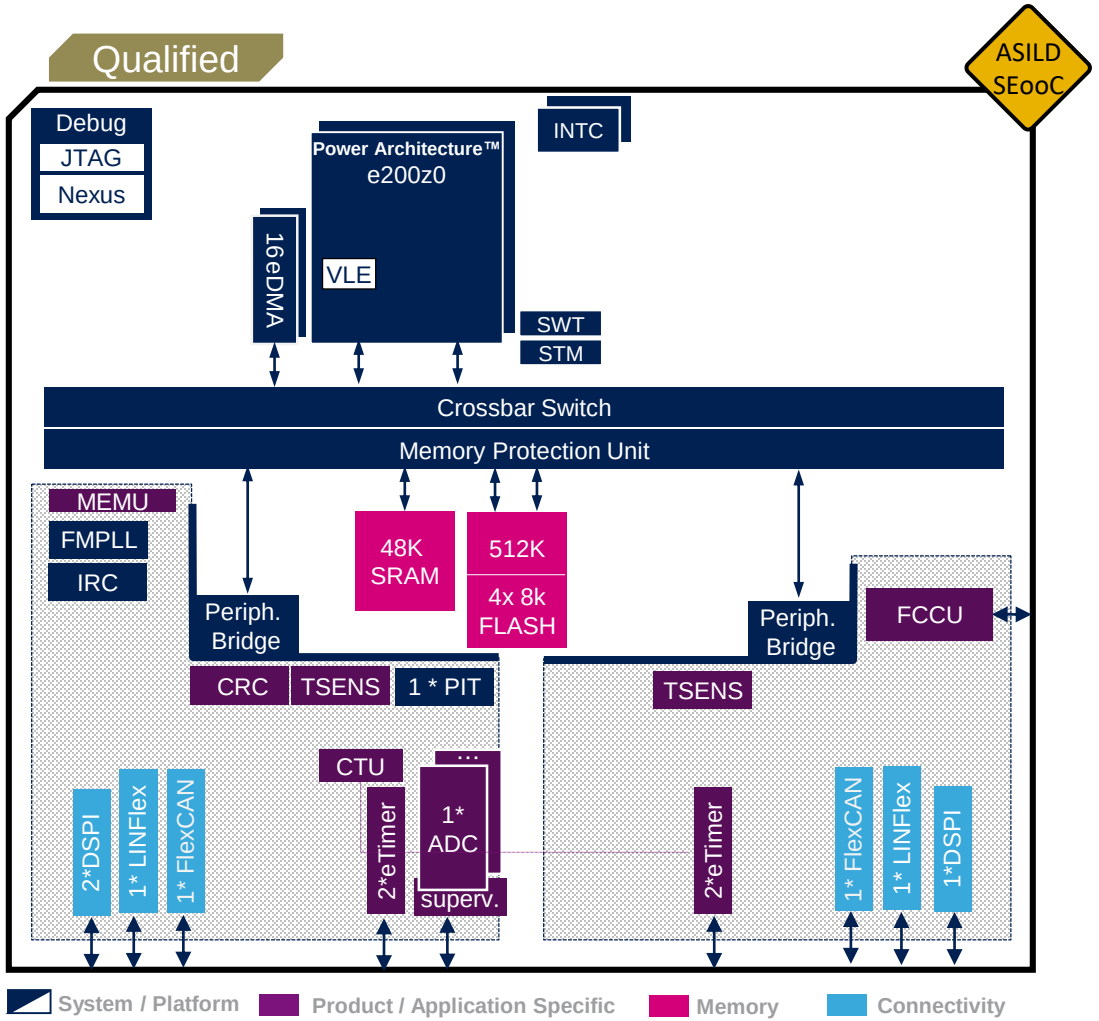
Superset Block Diagram

Core
- Up to 80 MHz Power Architecture™ ISA e200z0 Core (VLE)
- ASILD SEooC *(see technical safety concept)*

Memory
- 512k byte Flash with ECC
- 4x8k Data Flash with ECC *(1 RWW partition)*
- 48k SRAM with ECC
- Crossbar with MPU (8 regions) w. process ID support

I/O
- 2x FlexCAN with 32MB
- 2 x LINFlex
- 4x DSPI
- 4 x eTimer (6ch each)
- ADC – 1+1 x 12Bit, up to 16Ch.
  - fast 10Bit conversion & supervisor ADC concept
- 1 x ADC cross triggering unit (CTU)

System
- 16ch eDMA (lockstep)
- CRC Unit (2Ch.)
- Fault Collection & Control Unit
- Software watchdog timer (inc. window mode, flow monitoring)
- Temperature Sensor
- 3.3V or 5Vsingle supply
- FM-PLL and 16MHz internal RC OSC
- Nexus Class 3 / JTAG (2 pin or 5 pin) / Trace Port (4MDO)
- 64/100 pins LQFP package ePAD
- -40ºC - + 165°C Tj



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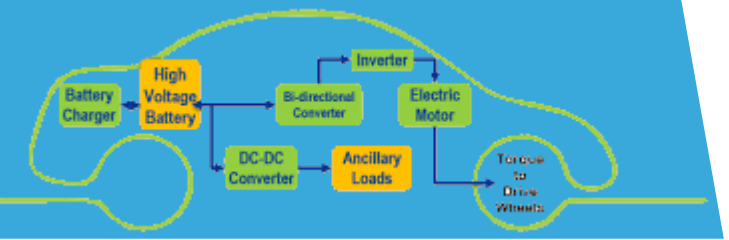
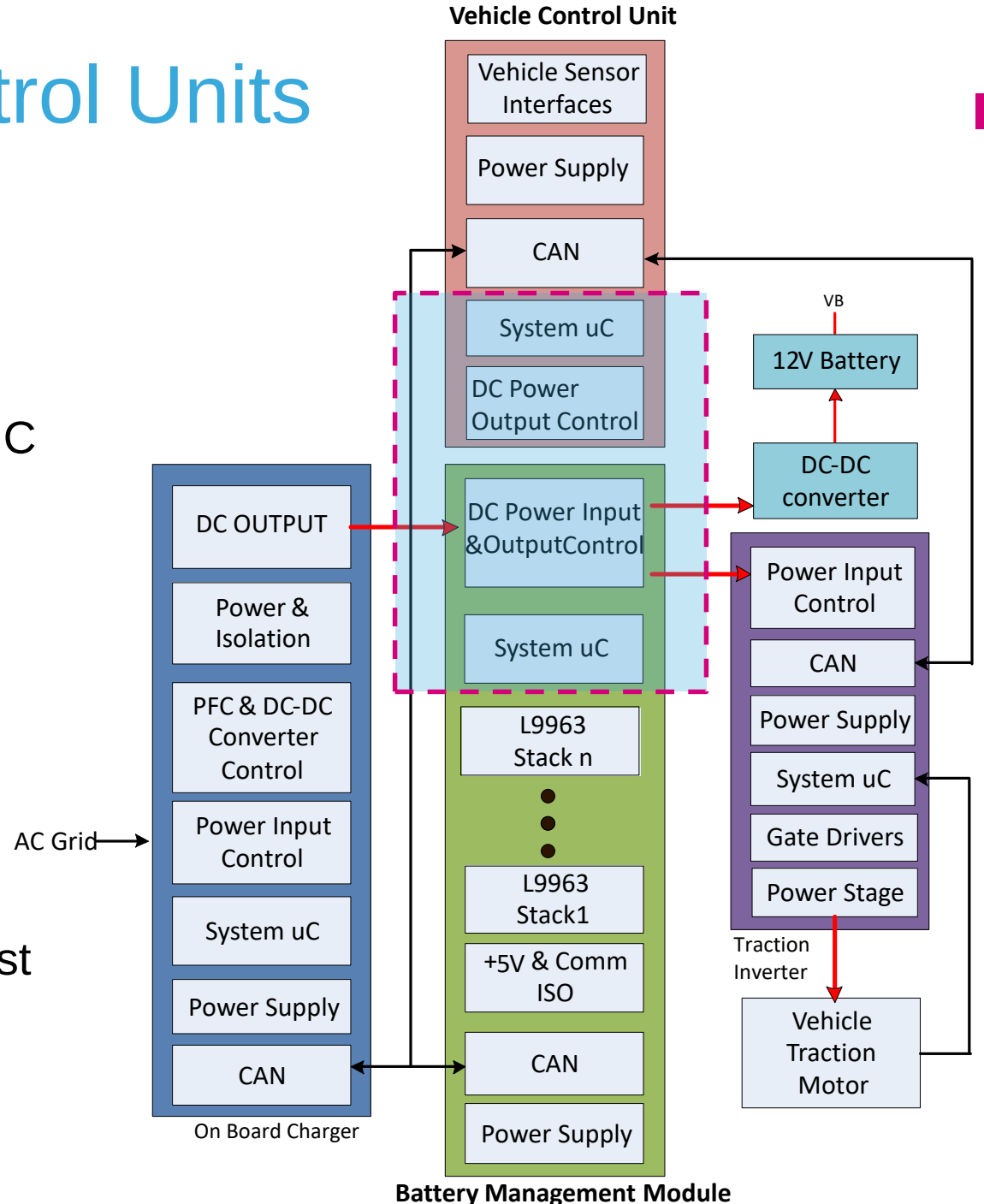
EV Systems Control Units

- **BMS**
- **Vehicle Control Unit**
- OBC
- DC-DC
- Traction Inverter

Trend for new DCM

- Integrated part of BMC and inverter function, such as SoC/SoH calculation, torque calculation, DC relay control and so on
- Advantage on
  - System control
  - System total cost





Chorus 6M SPC58NG84

Superset Block Diagram

Core

- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 16k Local i-RAM, 64k Local d-RAM
  - Lock Step (optional)
- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 16k Local i-RAM, 64k Local d-RAM
- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Floating Point Unit & LSP(DSP)
  - 8k-Instruction Cache
  - 16k Local i-RAM, 32k Local d-RAM

Memory

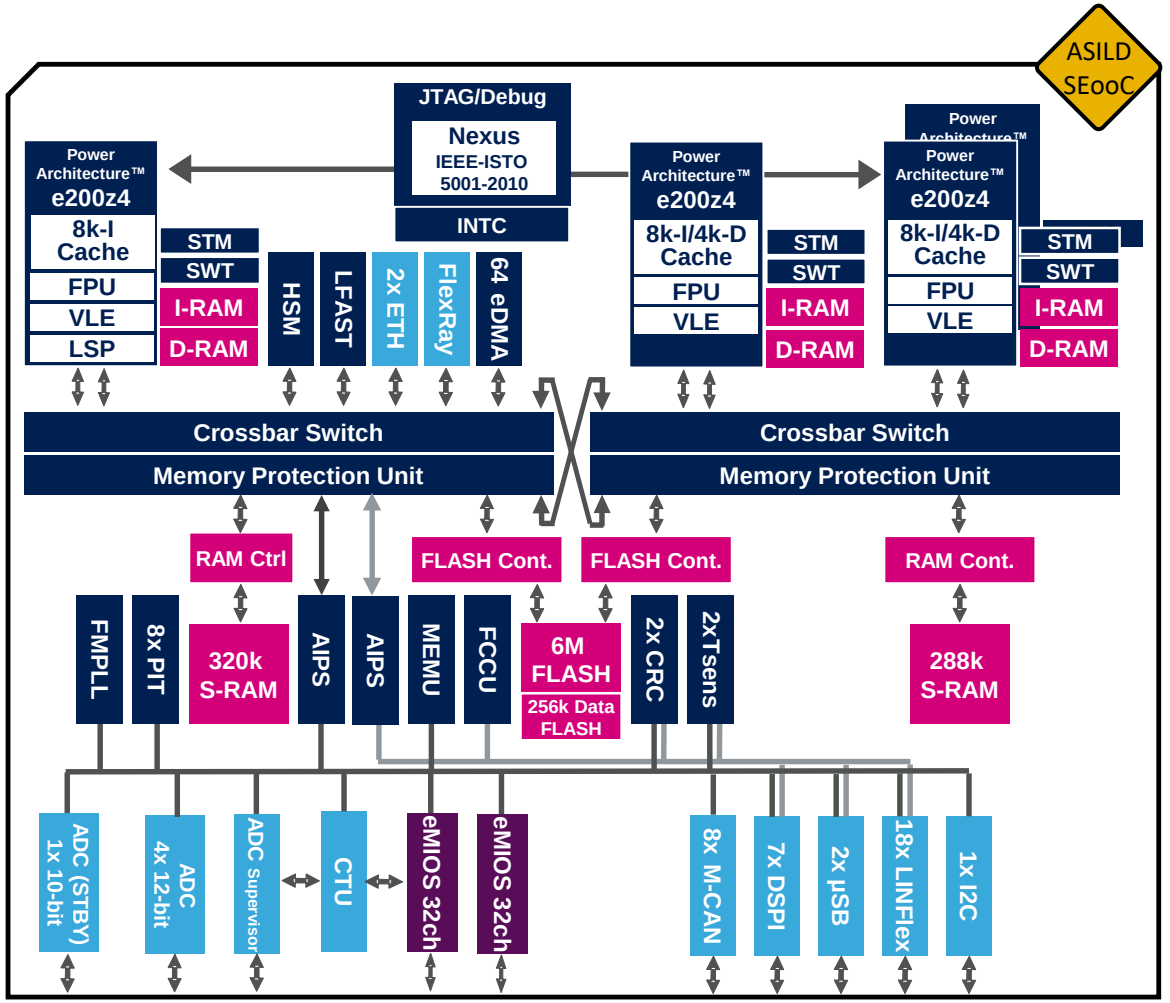
- **6M byte RWW Flash with ECC**
  - 4x64k Data Flash with ECC
- **768kRAM** (608k SRAM + 160k d-RAM) **with ECC**
  - Including 256k Standby

I/O

- **8 x MCAN / FD-CAN**
- **18 x LINFlex**
- **2 x Ethernet** (100Mb/s, time stamping, AVB, IPv4 Checksum)
- **Dual Channel FlexRay** (10MB/s, 128 buffers)
- **10 x DSPI, 1 x I2C**
- **2x 32ch eMIOS**
- **64ch CTU** (Cross Triggering Unit)
- **86 channel ADC**
  - 4x 12-bit ADC
  - 1x 12-bit ADC Supervisor
  - 1x 10-bit Standby ADC

System

- **SSWU** (Smart Standby Wake-up)
- **Security Module: HSM** (Evita Medium)
- **FM-PLL**
- **MPU**
- **64 Channel eDMA Controller**
- **2 x CRC Unit**
- **Fault Collection & Control Unit (incl. error pin)**
- **8 x PIT / 1x STM / 1x RTC/API**
- **1x LFAST (Interprocessor bus)**
- **Nexus IEEE-ISTO 5001-2010 Class 3+** (Aurora interface)



System Platform | Memory | Timer | Peripherals

Freq. max	Voltage	Temp.	ASIL	I/O	Package
180MHz	5V / 3.3V	-40 / +125°C	D	205	144/176/292

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