Best-in-Class Standard-Cell Libraries for High-Performance, Low-Power and High-Density SoC Design in 28nm FD-SOI Technology

White Paper

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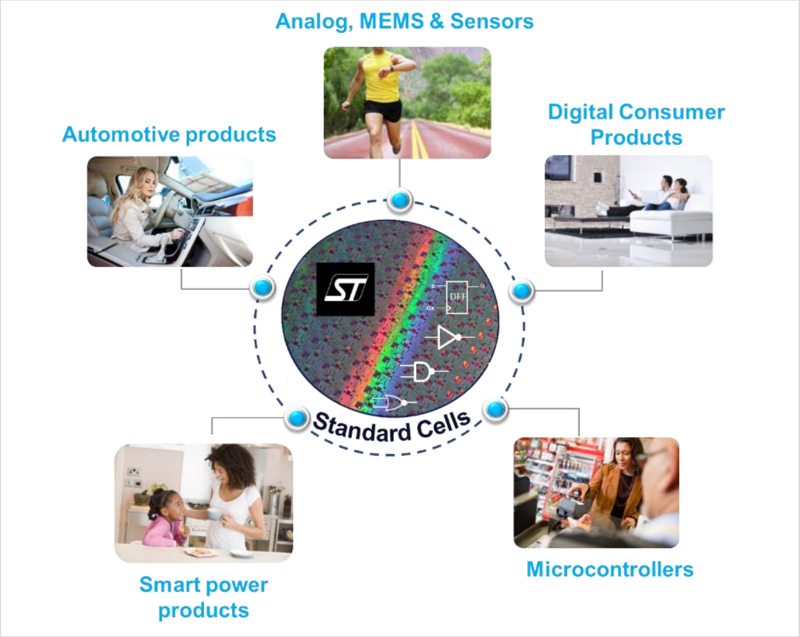
Introduction

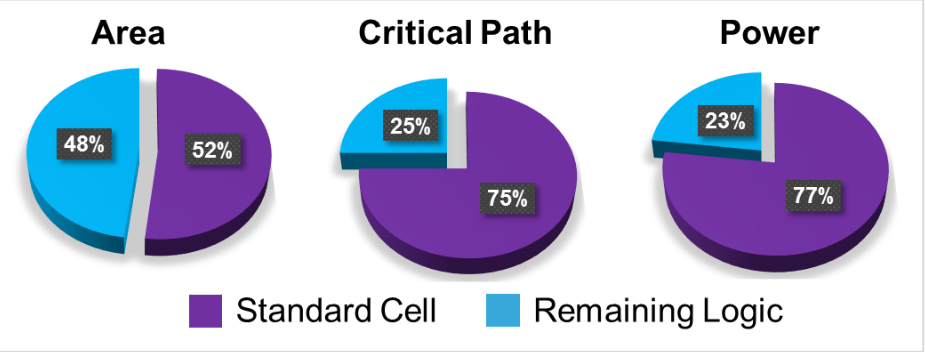
Standard-cells are crucial elements of all SoC/ASIC designs, constituting a dominant portion of the design, both in terms of the device count of the chip, as well as in die area. STMicroelectronics' standard-cell libraries address SoC/ASIC requirements in multiple market segments.

Figure 1: Pervasiveness of STMicroelectronics' standard cells across multiple market segments



Standard-cell performance in the timing critical paths of designs, and their energy efficiency in terms of leakage and dynamic power, have a direct bearing on the PPA (performance, power, and area) and cost of the chip. The PPA of a chip is tightly coupled to the PPA of the standard cells it contains. Such correlation is prominently observed in various chips, one of which, a consumer chip implemented in STMicroelectronics' 28nm FD-SOI technology, is illustrated below.

Figure 2: Contribution of standard cells in the PPA of a consumer chip in 28nm FD-SOI technology

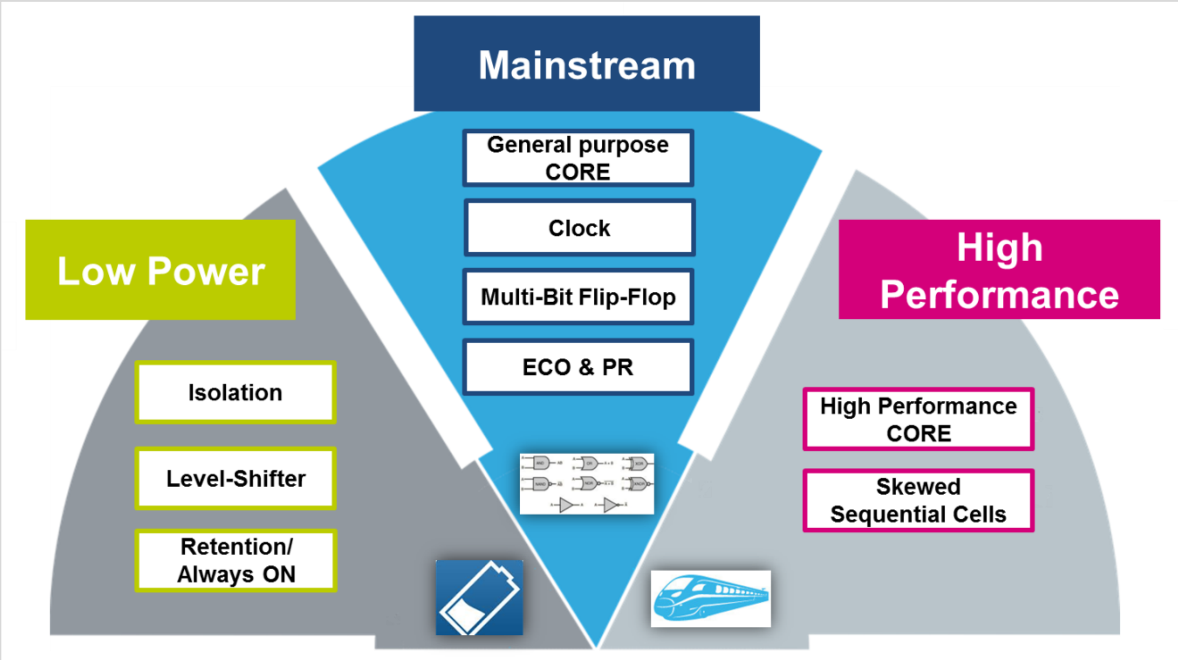


The 28nm FD-SOI technology creates a crucial inflection point in the technology roadmap of the industry because it offers a **unique sweet spot** enabling **ultra-low-power**, **low-voltage**, **high-performance** and **cost-effective** SoC solutions using a single technology node. 28nm FD-SOI brings immense flexibility in terms of operating **voltage range across 0.6V – 1.1V**, and **body-bias techniques** to obtain any application's ideal balance between performance and leakage. Being a planar technology, FD-SOI ensures easy portability of bulk designs, and seamless usage of classical EDA flows. FD-SOI also makes possible a comprehensive integration not limited to advanced digital CMOS, but also RF, high-performance analog, and embedded nonvolatile memories, thereby perfectly addressing **IoT, consumer multimedia, networking infrastructure, smartphone and mobile, and automotive market** requirements.

28nm FD-SOI Standard-Cell Library Offer

STMicroelectronics offers a wide-ranged standard-cell library portfolio in the ground-breaking 28nm FD-SOI technology. The standard-cells designed in 28nm FD-SOI offer unique advantages to various SoC/ASIC applications. The mainstream standard-cell library offer is augmented by specialized offers for low-power and high-performance applications.

Figure 3: Application-oriented standard cell offer in 28nm FD-SOI technology



Multiple Architectures

The 28nm FD-SOI standard-cell library offer supports multiple architecture for **best optimization** in **performance**, **power**, **and area** requirements of SoC/ASIC designs. The offer includes **a High-Performance Architecture: 12-Track** and **a High-Density Architecture: 8-Track**, for varied customer application requirements.

Figure 4: Multi architecture in 28nm FD-SOI technology

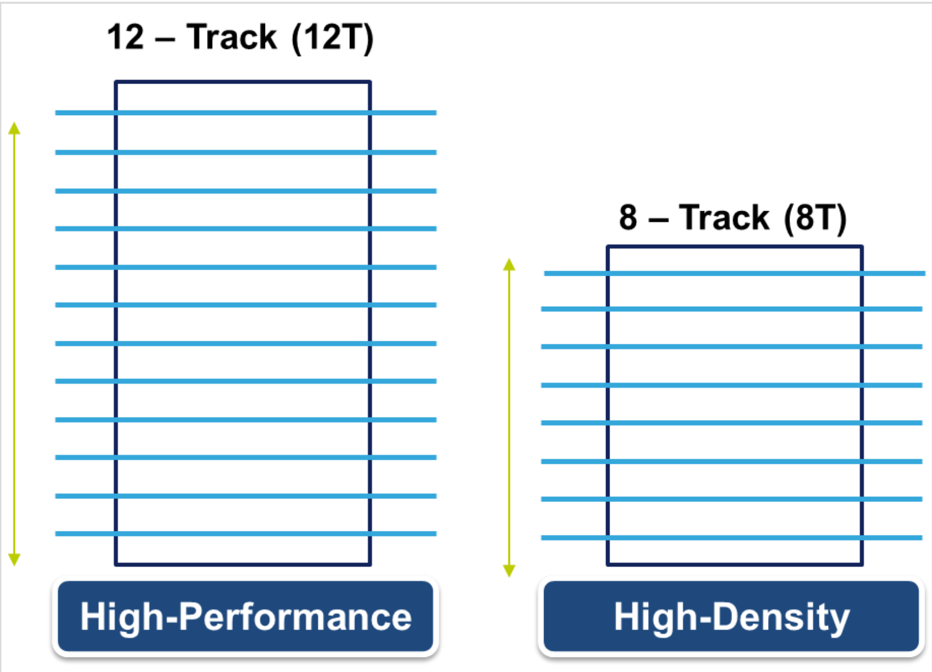
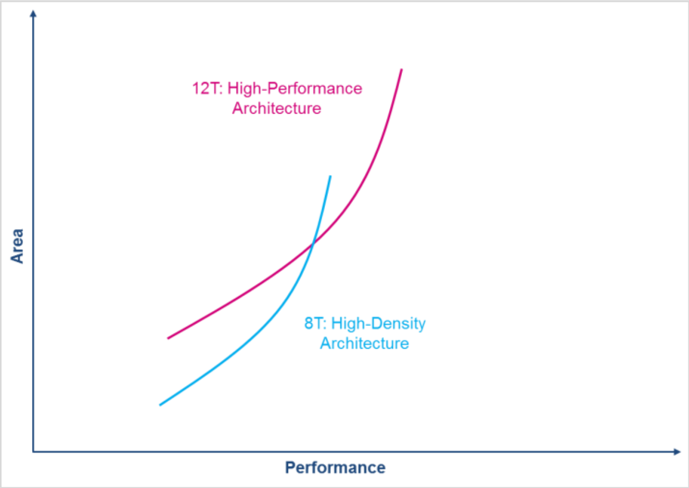


Figure 5: Performance vs Area comparison across multiple architectures



Multi-Channel Length Variants

The Poly-biased library cells offer further **reduction in leakage**. STMicroelectronics 28nm FD-SOI technology **allows to modulate the effective channel length of logic transistors** for authorized poly-to-contact pitch. The bias number (**PB0, PB4, PB10, PB16**) indicates the additional value to the minimal channel length.

Figure 6: Multiple channel lengths (poly biasing) support in 28nm FD-SOI standard cells

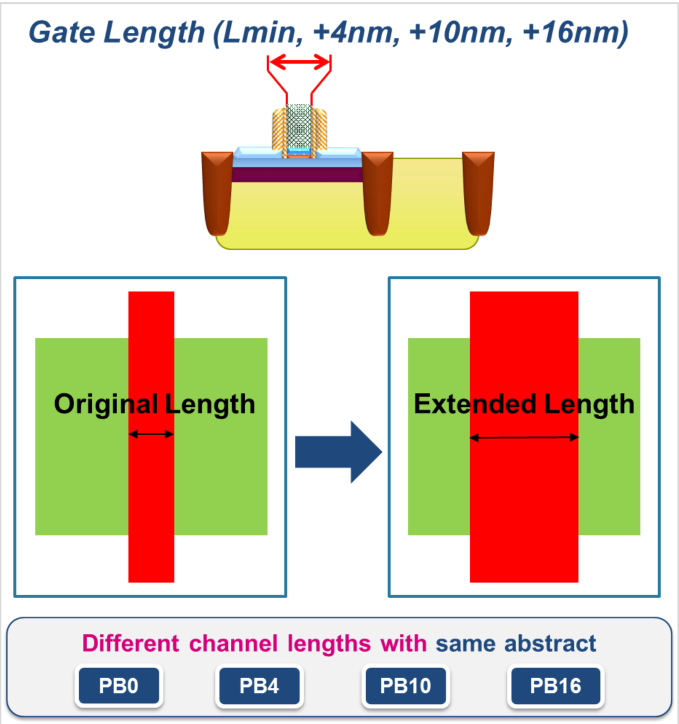


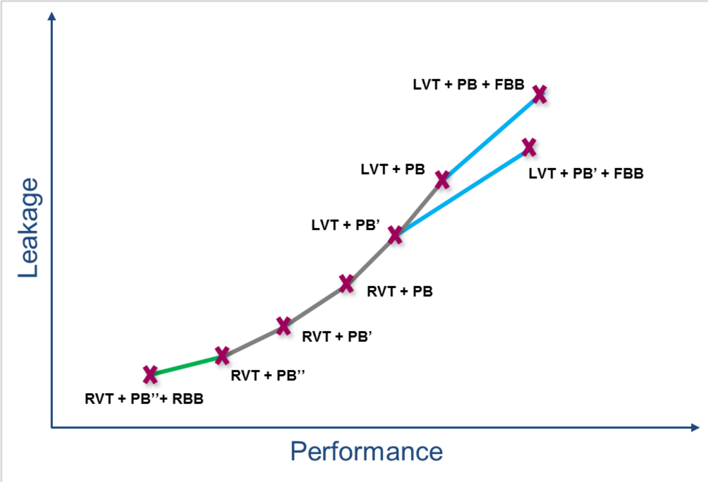
Table 1: Leakage reduction achieved by poly-biasing in 28nm FD-SOI technology

Gate Length (Lgate)	Poly-Bias Options	Leakage Reduction
L_{min} (+0 nm)	PB0	**1**
+4nm	PB4	**x4**
+10nm	PB10	**x10**
+16nm	PB16	**x30**

Multi-Threshold Voltage (V_T) Support

To strike the **best trade-off between leakage power** and **speed**, **Multi-Threshold-Voltage (V_T) libraries** are offered with **Regular- V_T (RVT)** and **Low- V_T (LVT)** flavors. The RVT flavor leverages the regular well technology, whereas the LVT flavor leverages the patented flip-well technology.

Figure 7: Effect of multi-channel length & multi-threshold voltage in 28nm FD-SOI standard cells

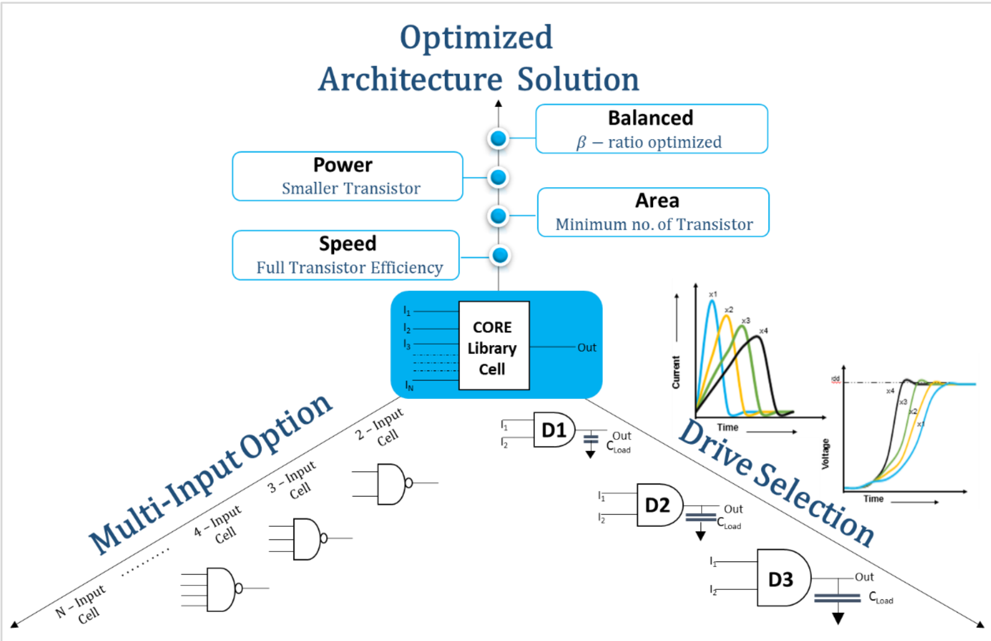


Mainstream Libraries

CORE Library

STMicroelectronics offers mainstream **CORE libraries** for **combinational** and **sequential** logic. The **CORE cells are classified** based upon **multi-input functions**, **optimized architectures**, and **drive options**. **CORE cells are optimized** for **speed**, **power**, **area**, and **balanced timing arcs**. The rich functionality of the library offers **input cells with one to 6 inputs**, each having a **wide range of drive options**. Overall, such a rich portfolio of standard-cells offers tremendous flexibility to SoC/ASIC designers to optimize their designs.

Figure 8: ST's rich portfolio of 28nm FD-SOI standard cells

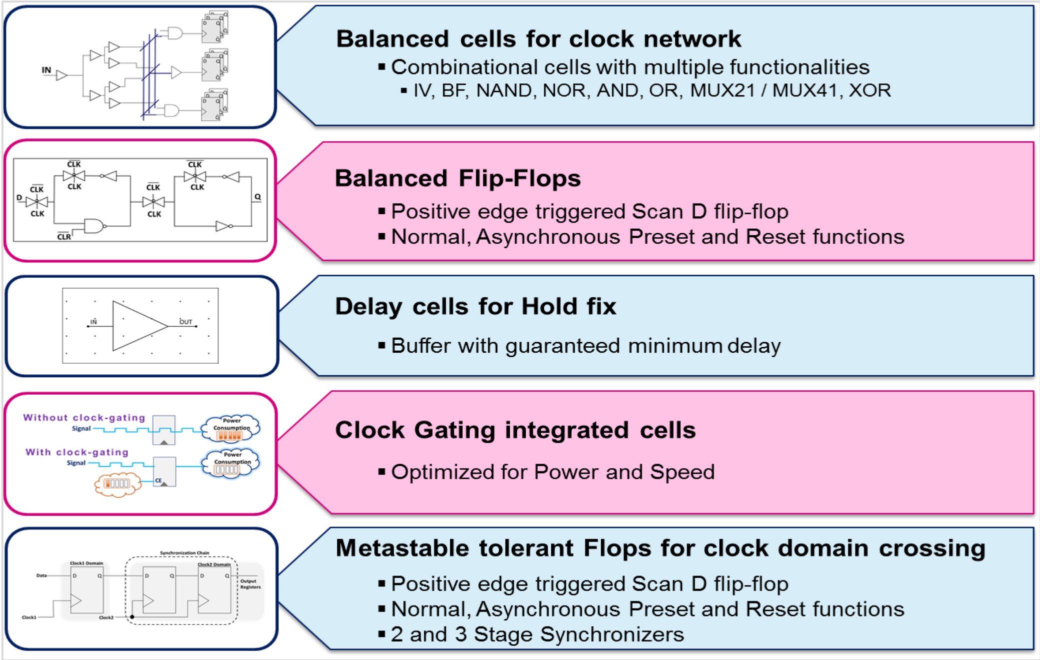


STMicroelectronics 28nm FD-SOI CORE library is competitive in the industry in terms of PPA. Details are furnished under **"Industry Benchmark PPA metrics,"** the last section of this literature.

CLOCK Library

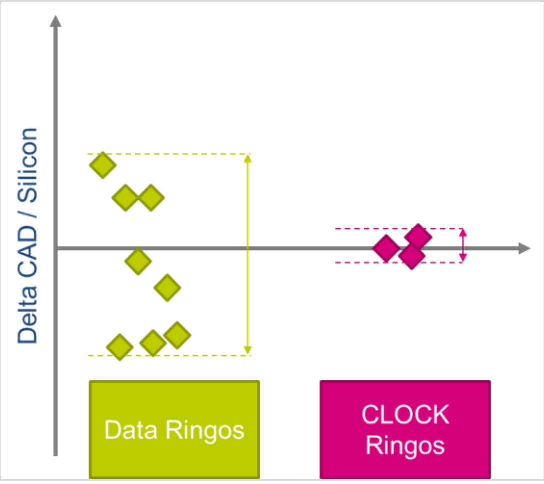
The specialized Clock (CLK) library offers a portfolio of (a) Balanced combinational cells for a clock network, (b) Balanced flip-flops, (c) Buffers with guaranteed minimum delay for hold-fix, (d) Clock Gating cells optimized for power and speed, and (e) Meta-stable tolerant flip-flops: for clock-domain crossing.

Figure 9: ST's rich portfolio of specialized clock cells



Also, Clock cells provide low variability, which is a key expectation during the Sign-off process of SoC design.

Figure 10: Low variability in Clock cells



PR & ECO Library

The library includes cells for specific purposes: Power Rail & Well Continuity, Antenna Protection, Supply Decoupling, etc. It also includes Mask Programmable ECO cells.
SoC/ASIC designs more often than not require to undergo Engineering Change Orders (ECOs) to manage last-minute updates, change in chip specifications or design fixes post tape-out. These requirements can potentially increase the implementation schedule and cost, particularly if a full mask re-spin is mandated. To overcome such costly re-spins, STMicroelectronics offers Mask-Programmable ECO Libraries, where changes can be implemented by changing metal layers only (while base layers remain fixed) thus avoiding full mask-set reorder, and reducing implementation time and cost.

Figure 11: Effective white-space utilization using PR & ECO library in 28nm FD-SOI

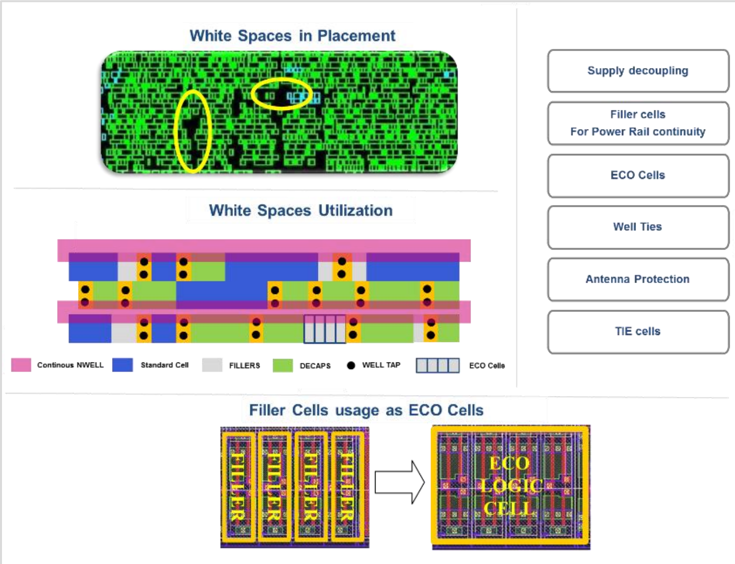


Table 2: Mainstream Library: Rich functionality portfolio*

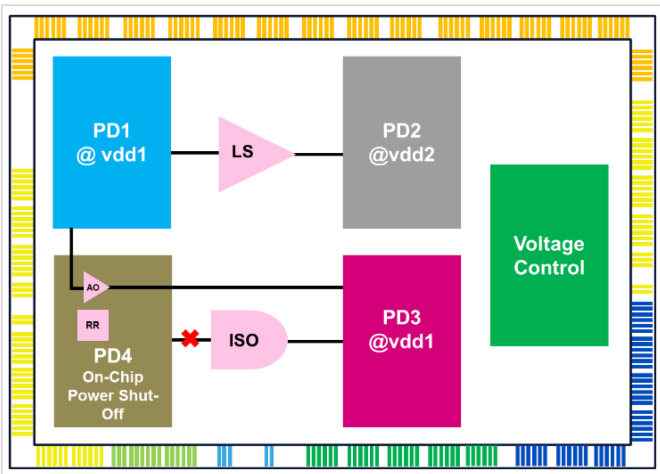
Cell Type	Functions / Optimizations	Cells
Buffer / Inverter	10	120
AND / NAND / OR / NOR	40	340
XOR / XNOR	10	60
Complex Boolean Gates (AOI / OAI)	62	400
Arithmetic Cells	7	20
Multiplexers	9	50
Latches, D Flip-Flops (Scan, Non-scan)	40	160
Clock Gating Cells	2	30
Tie / Antenna / Filler / Decap	-	40
Total	**180**	**1220**

**** This cell offer is for Single Track and Single Poly-bias library variants***

Libraries for Low-Power Applications

FD-SOI technology is inherently low power oriented. On top of this technology benefit, the design techniques supported in FD-SOI provide further leverage in terms of energy efficiency. The standard cell libraries support low-power design techniques such as clock gating, power gating, multiple power domains etc. through specialized cells.

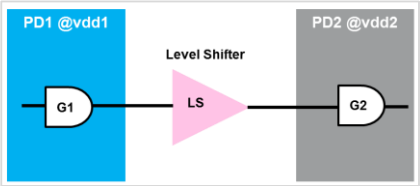
Figure 12: Low-power-application Standard cell in a SoC



Level Shifter

Level-shifter cells are required to shift the input-signal voltage to the receiving domain's voltage level, when signals cross from one voltage domain to another voltage domain and both domain voltages are not the same. In STMicroelectronics' library, both **High-to-Low** and **Low-to-High voltage shifter cells are supported**.

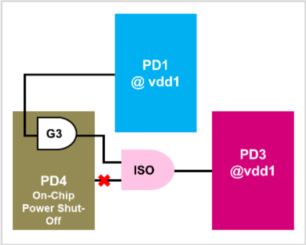
Figure 13: Level shifter cell



Isolation cells

Isolation cells are required in the interface between shut-down and powered-up blocks to ensure that there are no floating inputs to active powered up blocks, which could result in crowbar currents. These cells clamp the output node to a known voltage. STMicroelectronics offers the following types of Isolation cells in its library:
(a) Clamp the signal to "0", **(b) Clamp the signal to "1"**, and **(c) Clamp the signal to last value.**

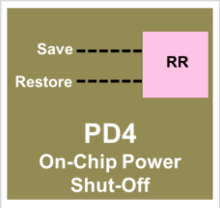
Figure 14: Isolation cell



Retention Registers

Retention Register cells are used to **hold the register states before power down** and these states can be **restored from these cells on power up**. Retention Register cells are special flip-flops with multiple power supplies. STMicroelectronics offers various types of retention register techniques like **Slave-alive / Balloon Architecture**.

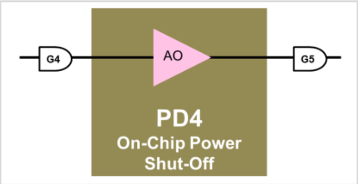
Figure 15: Retention Register cell



Always-ON

Always-ON are special cells that remain **always powered up** irrespective of their placement in Shut-down blocks. These cells are normally used to drive long nets through or from Shut-down blocks to active-powered blocks. STMicroelectronics library supports Always-ON Inverters and Buffers.

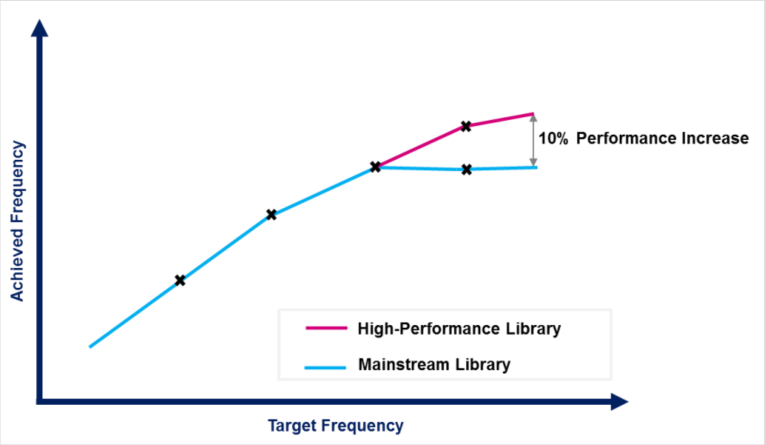
Figure 16: Always-ON cell



High-Performance Library

STMicroelectronics offers High-Performance libraries in 28nm FD-SOI technology, for designing high-speed application SoCs. **High-performance cells enhance speed by about 10% over mainstream cells**.

Figure 17: High-Performance library vs Mainstream library

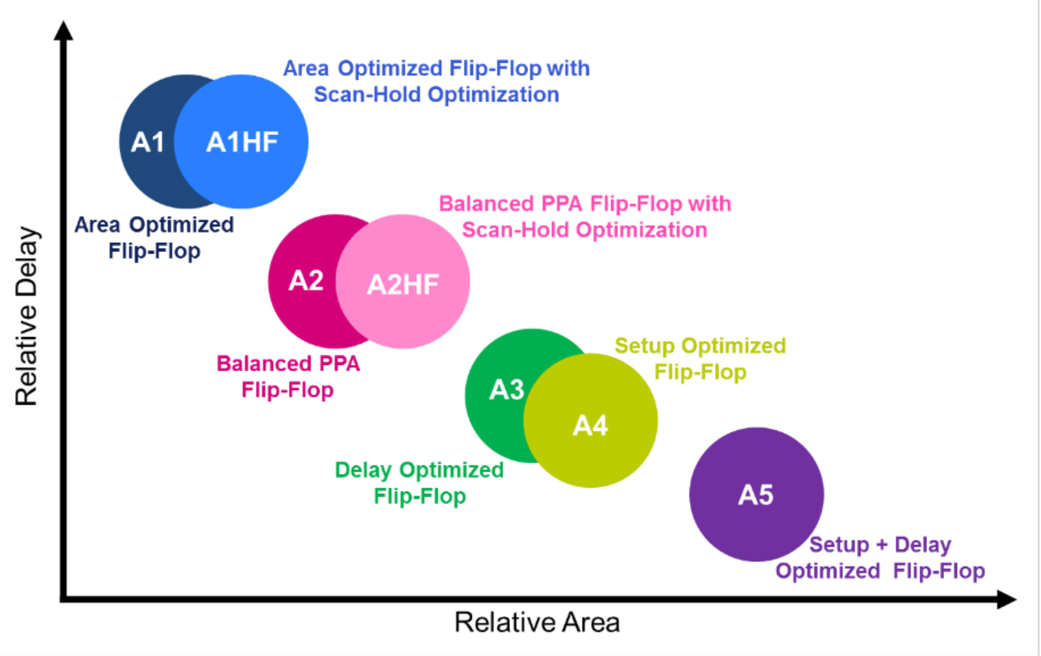


The CORE **combinational logic cells are further optimized for speed, leveraging optimizations in (a) beta-ratio**, **(b) drive**, **(c) stage-ratios**, and **(d) unbalanced paths**. **Sequential cells are optimized for (a) setup-time**, **(b) delay-time**, and **(c) setup + delay-time.** These flip-flops bring good leverage in terms of timing closure in the timing-critical logic paths for high-speed operation.

Flip-Flop Offer

The 28nm FD-SOI library offers a wide variety of flip-flops that allow users to find the best trade-off based on design requirements and constraints.

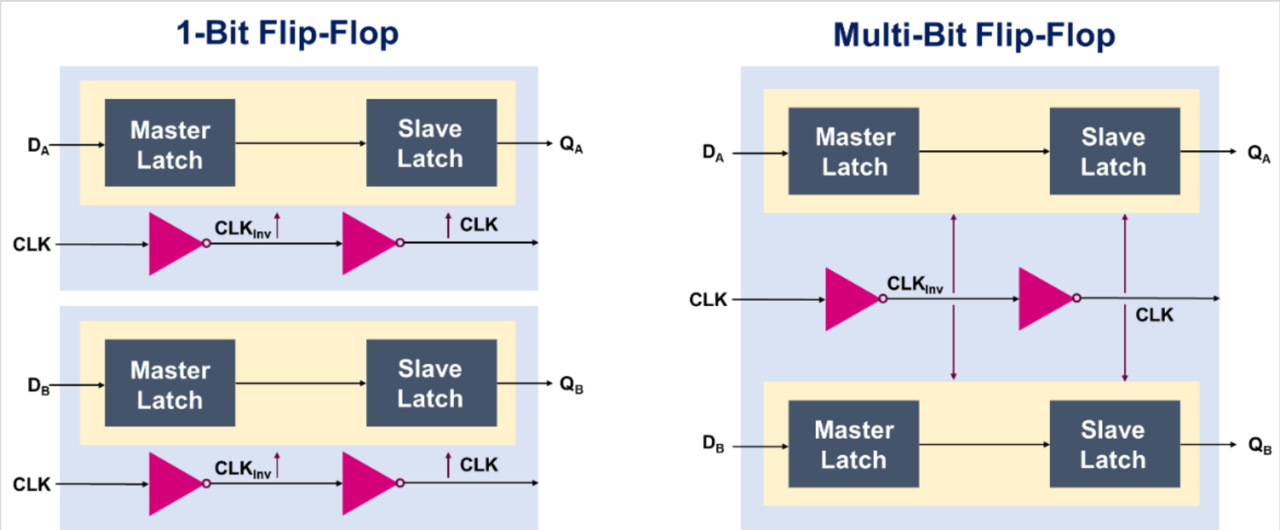
Figure 18: Enriched Flip-Flop offer for competitive PPA



Multi-Bit Flip-Flops

The **Multi-Bit Flip-Flop** in 28nm FD-SOI technology is one of the innovative approaches to meet design requirements for SoC/ASIC designs. Multi-Bit Flip-Flops employ an approach to clock power-saving technique that merges 1-bit flip-flops in the design. Using Multi-Bit Flip-Flops, **clock-tree load is reduced** significantly, resulting in **reduced overall dynamic power in the clock tree**. **Area** and **leakage power are also reduced by sharing Clock Inverters**. STMicroelectronics libraries support various kinds of **Multi-Bit Flip-Flops** having **multiple bit depth**.

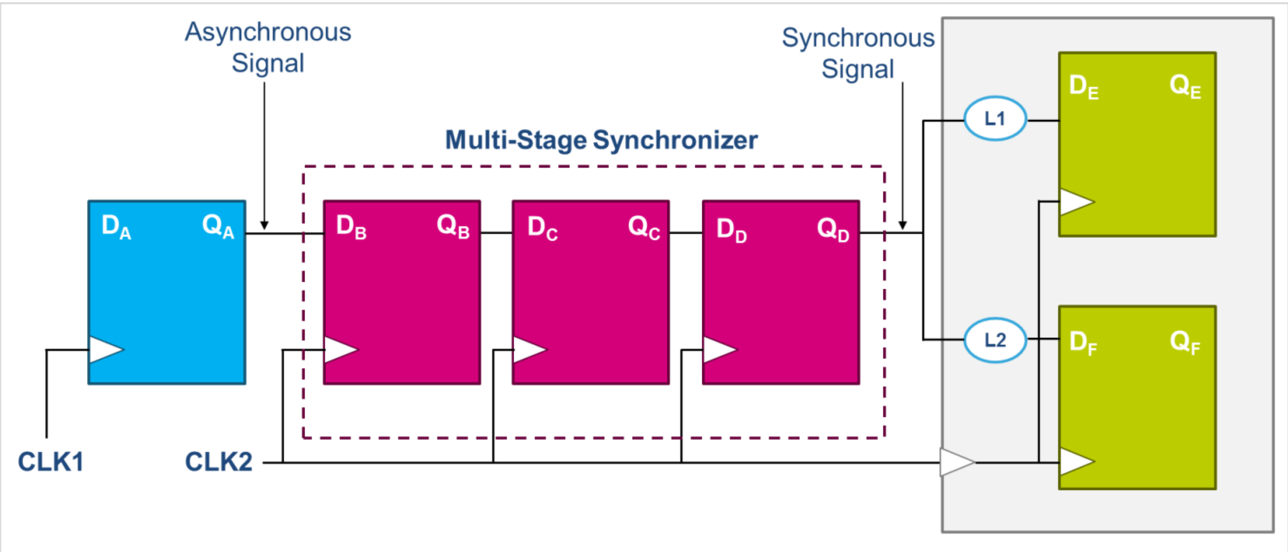
Figure 19: Multi-Bit Flip Flop in 28nm FD-SOI for higher PPA



Multi-Stage Synchronizer

Synchronizers are used to mitigate the effects of metastability in multiple-clock-domain SoC/ASICs. In a Multi-Stage Synchronizer, multiple flip-flops are cascaded with no combinational logic in between, thereby extending the time available for metastability resolution, resulting in longer/better **Mean Time between Failure (MTBF)**. STMicroelectronics library offers **2-Stage** and **3-Stage Synchronizers**.

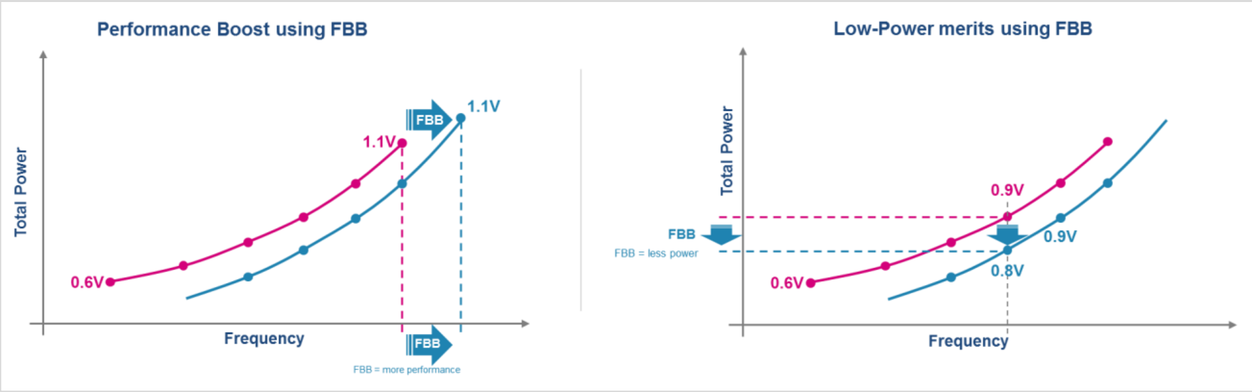
Figure 20: Multi-Stage Synchronizer



Body-Biasing Feature in 28nm FD-SOI Standard Cells

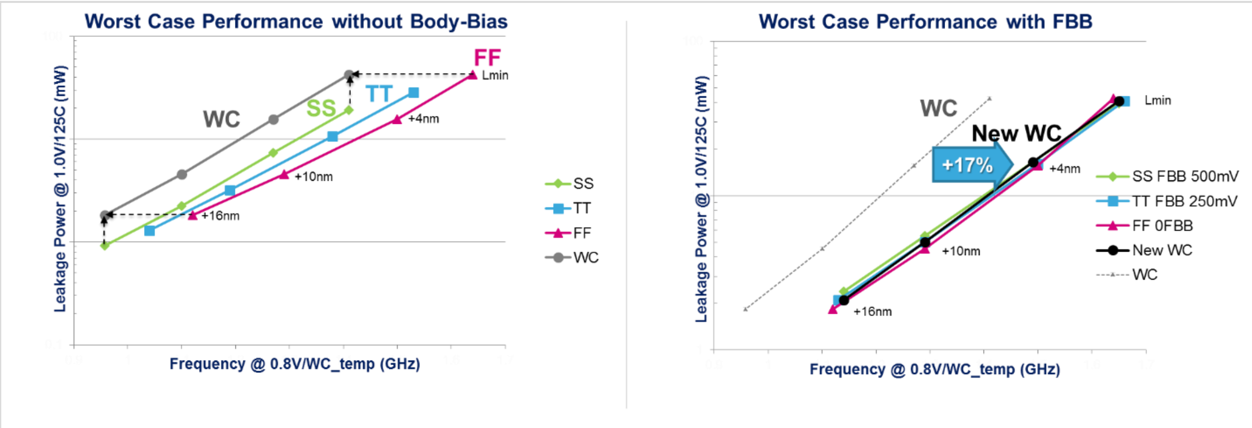
Body-Biasing is an **extremely powerful feature** available in **FD-SOI technology as compared to Bulk**, **and also equally easy to implement**. This feature is enabled in STMicroelectronics 28nm FD-SOI technology Standard-cells. The Body-Biasing option serves as an effective knob in optimizing performance and power. Due to an ultra-thin buried oxide (BOX), Body-Biasing is very effective in controlling the transistor channel, allowing a much wider range of biasing that can be modulated dynamically during transistor operation.

Figure 21: High-performance and Low-power merits in 28nm FD-SOI technology using body-bias



Body-Biasing in FD-SOI gives additional benefits in **Process Compensation,** by enabling designers to reduce margins at design levels.

Figure 22: Process compensation in 28nm FD-SOI technology using body-bias



For each gate length, the **worst-case (WC) performance trend is built** using **slowest (SS)** and **leakiest (FF)** process corners. By enabling the **Body-Biasing feature in 28nm FD-SOI technology**, **SS** and **FF** process spreads are masked together, thereby **recovering performance by 17%** with **no dynamic power penalty**.

Industry Benchmark PPA Metrics

ST's 28nm FD-SOI digital logic offer has super enhanced Power, Performance and Area (PPA) metrics proven in industry benchmarks and in various customer designs.

A recent benchmarking done by a customer has shown that the **28nm FD-SOI 8T** ultra-optimized offer from STMicroelectronics gives the best area and dynamic-power results at similar leakage and speed as compared to a competitor's **7T library 28nm HKMG bulk technology**. Using the ST 8T library, the design had **11.39% lower power consumption** and used **4.41% less area** than the **7T library**.

Table 3: ST 8T ultra optimized library's industry benchmark in terms of area and power at same performance

Case (500 MHz)	Area (μm^2)	Total Power (μW)
28nm FD-SOI 8T STMicroelectronics	22559	5381
28nm HKMG 7T External (Reference)	23555	5994
Gain / Loss	**4.41%**	**11.39%**

Another independent benchmark of **ST 8T library** vs. **a 9T library in 28nm HKMG bulk technology** from competition confirms a **10.06% area advantage**. In conclusion, the **ST 8T library in 28nm FD-SOI** facilitates the best-in-class PPA in the industry.

Table 4: ST 8T ultra optimized library's industry benchmark in terms of Area

Case	Area (μm^2)
28nm FD-SOI 8T STMicroelectronics	356721
28nm HKMG 9T External (Reference)	392642
Gain / Loss	**10.06%**

Conclusion

STMicroelectronics 28nm FD-SOI-technology standard cells bring enormous flexibility to SoC/ASIC designers through diverse architectures, poly-biasing options, and multi-threshold voltage variants. The mainstream offer is augmented with specific offers for high-performance and low-power applications. An enriched flip-flop offer enables users to exercise a wide range of scenarios within their design requirements. Additionally, the Body-Biasing feature enables further optimization in performance and leakage. Also, the 28nm FD-SOI Standard Cells bring confirmed competitive advantage through industry benchmark performance, power and area advantages as proven on real SoC/ASIC designs.

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