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28nm FD-SOI Technology Catalog



FD-SOI



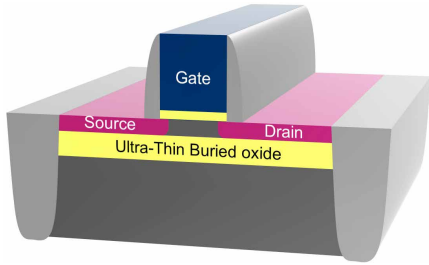
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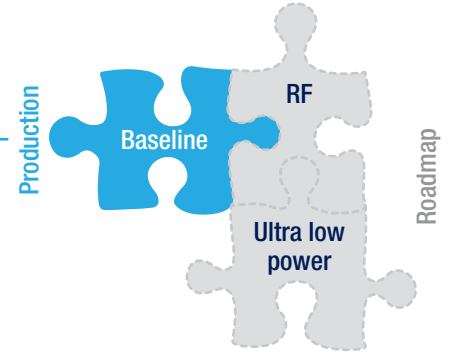
FD-SOI Technology



The unique advantages of 28nm FD-SOI technology, allow SoC/ASIC designers to gain full benefit of best-in-class Performance, Power, and Area (PPA) in a single process-technology flavor without having to choose multiple technology variants.

- Power and energy efficiency**
Ultra low leakage, wide Body-Bias & operating voltage range
- Analog performance**
for mixed signal & RF design
- Robustness**
for mission critical applications
- Cost effective platform**

FD-SOI



A few of the advantages of 28nm FD-SOI technology:

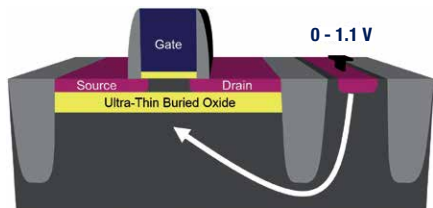
- At 28nm, FD-SOI requires fewer mask steps because it is a simpler process.
- In UTBB FD-SOI technology, the channel is quite thin, so it can be effectively controlled by the Gate, which results in lower leakage power (in static/stand-by power). For design optimization and flexibility, **multiple Threshold Voltage (V_T)** flavors of the transistor are available, including:
 - RVT device for regular- V_T or standard- V_T circuits,
 - LVT device for low- V_T high-speed circuits.
- **Body-Biasing** is an effective feature in FD-SOI to control the V_T of the transistor to leverage device electrostatics for speed and leakage optimization.
- **Wide operating voltage range**, for different applications with competitive PPA advantages:
 - Very low V_{DD} for ultra-low power applications,
 - Reduced V_{DD} for competitive speed at reasonable power consumption,
 - Nominal V_{DD} for high-performance applications.
- **Excellent device electrostatics**, (a) low leakage, leveraging Ultra-Thin Body and Box (UTBB) technology, (b) faster operation, due to the fully depleted channel, and (c) remarkable reliability

APPLICATION BENEFITS BY MARKET SEGMENT

Internet of Things, Wearable	Automotive
<ul style="list-style-type: none"> • Ultra-low-voltage operation • FBB optimizes power/performance • Efficient RF and analog integration 	<ul style="list-style-type: none"> • Well-managed leakage in high-temperature environments • High reliability thanks to highly-efficient memories
Networking Infrastructure	Consumer Multimedia
<ul style="list-style-type: none"> • Energy-efficient multicore • Adapt performance & power to workload via FBB • Excellent performance in memories 	<ul style="list-style-type: none"> • Optimized SoC integration (Mixed-signal & RF) • Energy-efficient SoC under all thermal conditions • Optimized leakage in idle mode

THE BODY-BIAS (BB) ADVANTAGE

Effective lever to optimize between higher performance and lower leakage



BODY-BIASING: AN EXTREMELY POWERFUL AND FLEXIBLE CONCEPT IN FD-SOI

Body-biasing, also often referred to as back biasing, controls the threshold voltage (V_T) of a transistor to optimize:

- Drive current (for higher performance) at the expense of increased leakage current (Forward Back Bias, FBB)
- Or, leakage current, with somewhat lower performance (Reverse Back Bias, RBB)

Body-biasing facilitates a wide Dynamic Voltage Frequency Scaling (DVFS) range (0.7 V – 1.1 V)

- Performance boost wherever needed
- Reduce power consumption at a given performance requirement
- Process compensation reducing the margins to be taken at design
- Seamless inclusion in the EDA flow

FOUNDATION IP/LIBRARIES PORTFOLIO

Standard-Cells

- Multiple Architectures
- Multiple Channel-length (Poly-Biasing) options
- Multiple- V_T options
- Rich portfolio of cells

IO

- Wide portfolio for various applications
- Optimized for Core/Pad Limited chip configurations
- Differentiating solutions for Low Power and Area Efficiency
- Programmability for varied board/package and loading environment

Memories

- Low V_{min}
- Low Power options
- Mono & Dual rail compilers
- Soft-Error Rate (SER) robustness

Clock Generators

- Wide-Portfolio
- Various Patented Architectures
- Best-in-Class Performance, Power, Area

Data Convertors (ADC & DAC)

- Multiple Architectures
- Wide Resolution range (up to 24 bits)
- High-Speed (up to 64 Gsps)
- Best-in-Class Performance, Power, Area

Specific IPs

- Body-Bias Generator
- OTP Security IP (Fuse)
- Process Monitoring Block (PMB), Thermal and Voltage Sensors
- Regulators
- Power Management IPs

STANDARD-CELLS

STMicroelectronics offers a broad portfolio of standard-cell libraries in 28nm FD-SOI technology. The standard-cells designed in 28nm FD-SOI offer unique advantages to various SoC/ASIC applications. The mainstream standard-cell library is augmented by specialized libraries for low-power and high-performance applications.

Low Power	Mainstream	High-Performance
<ul style="list-style-type: none"> • Isolation • Level-Shifter • Retention/Always-ON 	<ul style="list-style-type: none"> • General Purpose CORE • Multi-Bit Flip-Flop • Clock • ECO & PR 	<ul style="list-style-type: none"> • High-Performance CORE • Skewed Sequential Cells

The Mainstream library and Low-Power library are available with both RVT and LVT threshold-voltage support in 12-Track (12T) and 8-Track (8T) architectures. The High-Performance library has both 12T & 8T architectures and LVT threshold-voltage options.

...Classification based on application
 Multiple tracks and architectures (12T/8T)
 Multi-threshold voltage (V_t) support (LVT/RVT)
 Multi-channel length variants (Poly-Bias P0/P4/P10/P16)

	Library	8 Track		12 Track	
		LVT	RVT	LVT	RVT
Low-Power	CORI (Core Isolation Library)	•	•	•	•
	CORR (Core Retention Register Library)	•	•	•	•
	SHIFT (Level Shifter Library)	•	•	•	•
	CORBF (Core Multi-Bit Flip-Flop Library)	•	•	-	-
	SYNC (Synchronizer Library)	•	•	•	-
	CDMPR (Place & Route Library with CDM Protection)	-	-	•	•
	CDMSHIFT (Level Shifter Library with CDM Protection)	-	-	•	•
Mainstream	CORE (Core Library)	•	•	•	•
	CLK (Clock Library)	•	•	•	•
	PR (Place & Route Library)	•	•	•	•
	ECO (Engineering Change Order Library)	•	•	•	•
High-Performance	CORHP (High-Performance Core Library)	•	-	•	-
	CORXT (Library with High-Speed Flip-Flops)	•	-	•	-

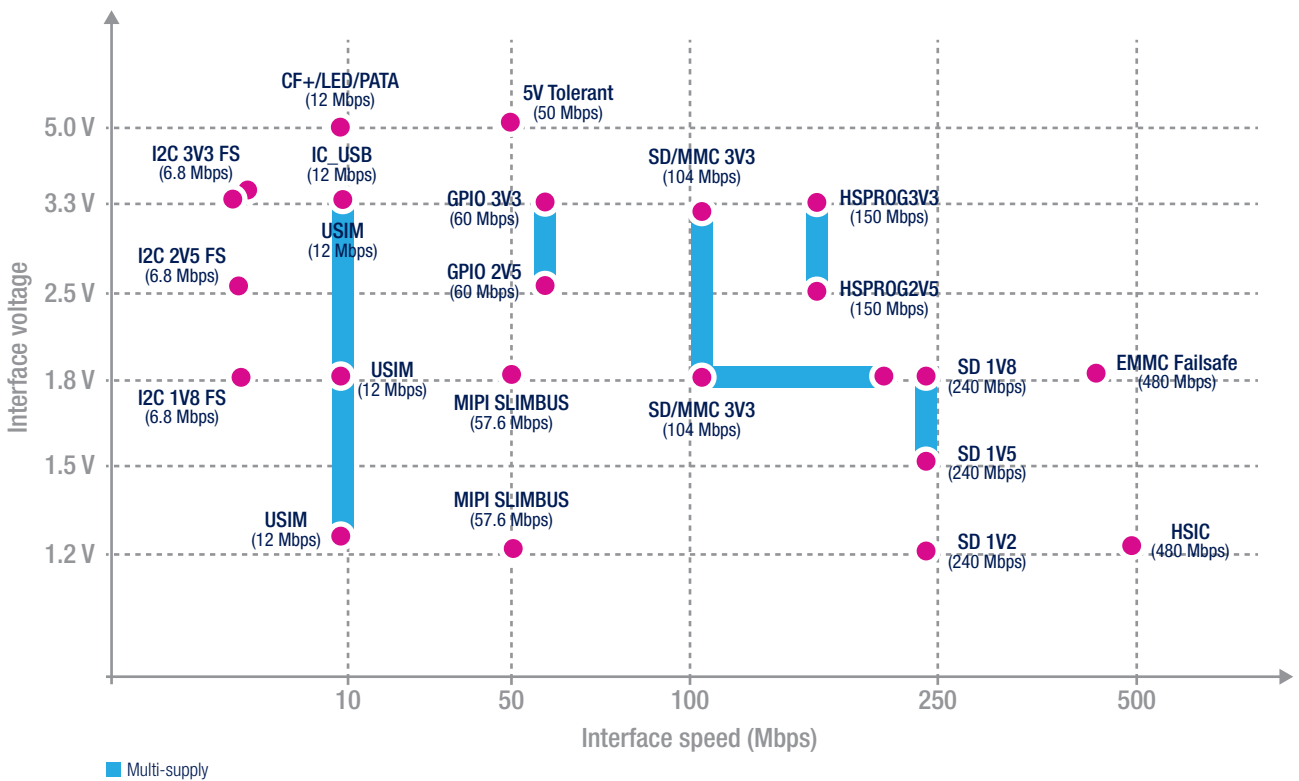
* Other electrical parameters will be disclosed under NDA

IO

28nm FD-SOI IO library enables flexible, effective and reliable interfacing in SoC design with state-of-the-art features and PPA advantages. Special approaches, such as the compensation strategy, flexibility between compensated and uncompensated IO, and ESD solutions, provide differentiation in SoC/ASIC designs with applications ranging from low-power hand-held devices to high-performance computing.

The IO solutions consists of versatile cells with multiple features:

- Wide range of functionalities: **interface functionalities**, dedicated IO functionalities to serve **analog IP blocks, power-supply provisioning** to an SoC, or provision of **reliable ESD protection**
- **Multiple Metal Stacks options, Multiple Supply Voltages, and Chip-Layout Configurations** (Core-Limited, Pad-Limited, and Pad-in-Core)
- **Differentiating solutions:** No intermediate supply required in 3.3 V IO, significantly fewer supply pads using compensation strategy, multiple patents in IO design
- IO offer **supports a variety of industry standards** like I²C, USB, GPIO, MIPI Slimbus, SDMMC, HSPROG, EMMC and other specific high-speed IO interfaces
- Advanced ESD protection compliant to **IEC 61000-4-2** are available on request



Interface/Application	Library name	IO standard	IO supply	Features/Specification
General Purpose UART, JTAG	GPIO 1V8 1.8 V Programmable IO, Non-PVT Compensated	JESD76/JESD8-7	1.8 V	<ul style="list-style-type: none"> • 8-Level-Drive Programmability • 1V8 Failsafe and Non-Failsafe • Support 1V5 and 1V2 operation
	GPIO 3V3 3.3 V Programmable IO, Non-PVT Compensated	JESD76/JESD8-B	3.3 V	<ul style="list-style-type: none"> • 4-Level-Drive Programmability • 3.3 V Failsafe and Non-Failsafe
	GPIO 1V8_3V3 1.8 V & 3.3 V Programmable IO, Non-PVT Compensated	JESD76/JESD8-7 JESD8-B	1.8 V 3.3 V	<ul style="list-style-type: none"> • 3.3 V Failsafe cell • Two-level drive/slew options
	2V5_3V3 2.5 V & 3.3 V Programmable IO, Non-PVT Compensated	JESD80/JESD8-5 JESD76/JESD8-B	2.5 V 3.3 V	<ul style="list-style-type: none"> • 4-Level-Speed programmability
	TESTMUX 1V8 1.8 V High-Performance IO, PVT Compensated	JESD76/JESD8-7	1.8 V	<ul style="list-style-type: none"> • 2-Level-Drive programmability • Cells with 2/4 /6/8 mA drives • Support 1.5 V and 1.2 V operation
	PROG 1V8 1.8 V High-Performance IO, PVT Compensated	JESD76/JESD8-7	1.8 V	<ul style="list-style-type: none"> • Isolation & Retention feature • 2-Level-Drive programmability • Non-Failsafe and Failsafe cells • Support 1V5 and 1V2 operation
PVT Compensation Block	COMPENSATION1V8 PVT Compensated	-	1.8 V	<ul style="list-style-type: none"> • Library for PVT compensation at 1.8 V
	REFCOMPENSATION1V83V3 PVT Compensated	-	1.8 V 3.3 V	<ul style="list-style-type: none"> • Library for PVT compensation at 1.8 V & 3.3 V
Printer/LED	SRC 3V3 Large transmission length slew rate controlled 3.3 V IO	JESD76/JESD8-B	3.3 V	<ul style="list-style-type: none"> • Support critical Signal Integrity requirements • Support 6" to 24" trace length
SPI/SD/MMC/EMMC/Flash	SDMMC 1V8_3V3 1.8 V & 3.3 V SDMMC IO	SD3.01/JESD84 A44	1.8 V 3.3 V	<ul style="list-style-type: none"> • Support Type A (33Ω) and Type B (50Ω) driver
	EMMC 1V8 1.8 V EMMC Failsafe IO	JESD84 B50	1.8 V	<ul style="list-style-type: none"> • Support eMMC TYPE0(50), TYPE1 (33), TYPE2 (66), and TYPE3 (100) • Supports eMMC HS200 mode and eMMC HS400 mode • Support SDR and DDR
Digital Audio/MultiDrop	SLIMBUS 1V8 1.8 V Slimbus IO	MIPI Slimbus 1.1	1.8 V	<ul style="list-style-type: none"> • Isolation and Retention feature • 20 cm trace length support
Interchip USB	HSIC 1V2 1.2 V HSIC IO	High Speed Interchip USB 1.0	1.2 V	<ul style="list-style-type: none"> • Slew rate and Impedance control • 10 cm transmission line support • Jitter less than 365ps
HDMI/PMBus/ANDBus/Addressing/SMBus/IPMI/LCD Drivers/RTC	I ² C 1V8 1.8 V I ² C Failsafe Open Drain IO	NXP UM10204	1.8 V	<ul style="list-style-type: none"> • Support Standard Mode (100 KHz), Fast Mode (400 KHz), Fast Plus Mode (1 MHz) • Programmable built-in bus pull-up resistor
	I ² C 1V8 3V3TTFS 1.8 V I ² C IO with 3.3 V tolerant and failsafe		1.8 V	<ul style="list-style-type: none"> • Support Standard Mode (100 KHz), Fast Mode (400 KHz), Fast Plus Mode (1 MHz)
	I ² C 3V3 3.3 V I ² C Failsafe Open Drain IO		1.8 V	<ul style="list-style-type: none"> • Support I²C and SM Bus Mode • Support I²C Standard Mode (100 KHz) and Fast Mode (400 KHz)
	I ² C 3V3 5VFSFT 3.3 V I ² C IO with 5 V Failsafe and tolerant Open Drain feature		3.3 V	<ul style="list-style-type: none"> • Support I²C Standard Mode (100 KHz) and Fast Mode (400 KHz)
PMBus/ANDBus/Reset/SMBus/LCD Drivers	OD 3V3 Open Drain failsafe 3.3 V IO	JESD76/JESD8-B	3.3 V	<ul style="list-style-type: none"> • Bidirectional cell (200 KHz), Output cell (850 KHz) • 4 mA/8 mA output drive cell
Video	5VFSFT 5 V Failsafe Tolerant 3.3 V IO	JESD36	3.3 V	<ul style="list-style-type: none"> • 4 mA drive push-pull IO • 40 MHz
Analog Library	ANAF_ANA		1.0 V 1.8 V 3.3 V	<ul style="list-style-type: none"> • Analog IO cells with minimized parasitic capacitance • Includes basic cells enabling an optimized analog IO ring construction
	ANAF_ANA6V		1.0 V 1.8 V 3.3 V	<ul style="list-style-type: none"> • Analog Fail-Safe pad with 6 V signal protection • Restricted to USB20TG application only
	ANAF_3V3FS		1.0 V 1.8 V 3.3 V	<ul style="list-style-type: none"> • Fail-safe ANA pad with 3.3 V and 5.0 V signal protection
	ANAF_ANA_1V8FS		1.8 V	<ul style="list-style-type: none"> • 1.8 V Fail-Safe ANA pad
ESD, & Supplies Library	BASIC		1.8 V 3.3 V	<ul style="list-style-type: none"> • Includes Basic cells enabling the IO ring construction in Core-Limited, Pad-Limited or Pad in Core configurations
	CORESUPPLY		1.0 V 1.8 V 3.3 V	<ul style="list-style-type: none"> • Dedicated Core Supply cells and ESD Core-Clamp
	CDMKIT		1.1 V 1.8 V	<ul style="list-style-type: none"> • Optimized CDM protections
Packaging Library	BUMP		NA	<ul style="list-style-type: none"> • Available with three classes of BUMP cells • Provides Flip-Chip strategy to an IO library for high pin count

* Other electrical parameters will be disclosed under NDA

MEMORIES

28nm FD-SOI embedded memory offers versatility to designers by allowing them to choose from a wide portfolio of compilers, with its advantage of high performance and energy efficiency, along with high reliability and robustness. FD-SOI memories provide best-in-class PPA and figures of merit. The offer includes High-Performance, Low-Leakage, and Low-Voltage SRAMs and ROMs, along with special memories.

Low Leakage (LoLeak)	High Performance (HiPerf)	Body Bias Options	Special Memories
Single Port High Density	Single Port High Density	Single Port High Density	High Density Dual Port Register
Single Port Register	Single Port Register	Single Port Register	
Read Only Memory	Dual Port High Density	Dual Port High Density	
	Dual Port Register	Dual Port Register	

The compilers are further complemented by a rich variety of features, including:

- **Body-biasing** feature support for process compensation and performance boost
- **Low-power** features using input gating, standby, periphery shutdown and array retention, and Embedded switches
- **Multiple power rail** feature for operating-voltage reduction
- **Multiple bank options** offering interesting **timing-power-density-leakage trade-offs**
- **Multiple mux options** to select or modify the aspect ratio
- **Speed mode** selection to adjust the margins depending on the voltage of operation
- **Margin control** for self-time and reset operation
- **Redundancy** to improve the yield at the production level
- **Bit masks** to preserve the content
- **Embedded Test features** including BIST mux, scan chains, and synchronous bypass to reduce test time and improve test coverage
- **Neutron Soft Error Rate (SER)** less than 10 FIT/Mb and Immunity to Alpha SER
- **Patented well structures** to enable Ultra-Low-Voltage Operation.

	Compiler Name	Description
Low leakage memory	SPHD_LOLEAK	Single-port high-density compiler with best density, leakage trade-off
	SPREG_LOLEAK	Single-port register file optimized for leakage, speed, and density
	ROM_LOLEAK	Static ROM mainstream compiler
High performance memory	DPHD_HIPERF	Dual-port compiler targeted for high-performance, density, and low-power applications
	SPHD_HIPERF	Single-port high-density compiler with best density and speed trade-off
	DPREG_HIPERF	Dual-port dual-rail register file with high-performance bitcell
	SPREG_HIPERF	Single-port register file with high performance for Cache RAM applications
BODYBIAS Memory	SPHD_BODYBIAS	Single-port high-density compiler supporting forward body bias
	SPREG_BODYBIAS	Single-port register file supporting forward body bias for high-performance applications
	DPHD_BODYBIAS	Dual-port compiler targeted for high-performance, density, and low-power applications
	DPREG_BODYBIAS	Dual-port dual-rail register file with high-performance bitcell
Special Memory	PRF2HD_BODYBIAS	Area-optimised, dual-port register file using single-port bitcell

* Other electrical parameters will be disclosed under NDA

PHASE LOCKED-LOOP (PLL)

Phase Locked-Loop (PLLs) are clock generators for frequency synthesis. The standard offer (highly customizable) is supplemented with high-performance, spread-spectrum and fractional-PLL offers.

Standard PLL

- Generates multiples of input frequency (Frequency Synthesis)
- Highly customizable

Spread Spectrum PLL

- Spreads energy of output to a band around it
- Reduces Electromagnetic Interference (EMI)

Fractional PLL

- Generates output, which is a fractional multiple of input frequency

High Performance PLL

- Low jitter, low power, low area PLLs
- LC VCO based PLLs

The 28nm FD-SOI PLL offer has various features:

- **On-the-fly switching** (on request)
- **No dependence on supply sequence** (In absence of analog or digital supply, the PLL is automatically in power-down mode)
- **Multiple operating modes:** Normal, power-down, VCO stand-alone, Bypass
- **Automatic Bandwidth tracking**
- **Compatibility with all metal stacks** (uses only 5 thin metals)
- **Clock de-skewing** by acting as a negative delay element to compensated clock-tree delay

Name	Input Frequency		Output Frequency (MHz)		VCO Frequency (MHz)	
	Min	Max	Min	Max	Min	Max
PLL_FF_308MHZ	32.768 KHz	32.768 KHz	26	307.2	307.2	312.01
PLL_PF_960MHZ_B	1.92 MHz	93 MHz	480.960	480.960	960	960
PLL_PF_960MHZ_32K	32.768 KHz	32.768 KHz	153.6	319.98	921.26	959.98
PLL_PF_1066MHZ	195 MHz	1066 MHz	195	1066	780	1066
PLL_PF_1200MHZ	9.6 MHz	350 MHz	9.52	1248	600	1248
PLL_PF_2132MHZ_7P	19.2 MHz	52 MHz	754 (7 phase)	2132 (7 phase)	754	2132
PLL_PF_3000MHZ_FR	24 MHz	40 MHz	31.25	3000	1500	3000
PLL_PF_3401MHZ	10 MHz	340 MHz	106.25	3400	1700	3400
PLL_PF_4600MHZ_SSCG_FR	4.0 MHz	350 MHz	19.05	3000	2400	6000
PLL_PF_3200MHZ_SSCG_FR	4.0 MHz	350 MHz	12.7	1600	1600	3200
PLL_PF_5000MHZ_SSCG_FR	24 MHz	40 MHz	39.06	2500	2500	5000
PLL_PF_480MHZ_6P (for USB2.0)	2 MHz	93 MHz	480 (6 phase)	480 (6 phase)	480	480
PLL_PF_6400MHZ	6 MHz	210 MHz	50	3200	3200	6400
PLL_PF_4000MHZ	2 MHz	372 MHz	31.25	2000	2000	4000
PLL_PF_2920MHZ_8P	9.6 MHz	403 MHz	1152 (8 phase)	2920 (8 phase)	1152	2920

* Area & Power will be disclosed under NDA

OSCILLATORS

In 28nm FD-SOI Technology, a comprehensive portfolio of oscillators is available enabling area competitiveness, multiple metal-stack compatibility and wide frequency ranges. The oscillators support various modes of operation.

ON-CHIP CRYSTAL (XTAL) OSCILLATOR FEATURES:

- Frequency Range: 32 KHz, 24 MHz - 30 MHz
- Compatible with Multiple-Metallization
- Modes Supported: Oscillation Mode, IDDQ Mode, Force through Mode, Startup Test Mode, Bypass Mode

ON-CHIP RC OSCILLATOR FEATURES:

- Frequency Range: 30 MHz, 45 MHz, 90 MHz
- Metal Stack: 7 or 8
- Modes Supported: Raw Frequency Mode, Calibration Mode, Tracking Mode, IDDQ Mode, Bypass Mode

Oscillators*	Frequency	XTAL parameters		
		Max R _m	Max C ₀	C _A /C _B
32 KHz XTAL Oscillator				
C28SOI_OSC_XO_32K_ULP_LLR_EG	32.768 KHz	50 KΩ	3.0 pF	18 pF ± 20%
C28SOI_OSC_XO_32K_LR_EG	32.768 KHz	50 KΩ	3.5 pF	28 pF - 32 pF
24 MHz to 30 MHz XTAL Oscillator				
C28SOI_OSC_XOA_24M_LR_EG	24 - 30 MHz	50 Ω	5 pF	18 pF ± 20%
C28SOI_OSC_XOA_30M_LR_EG	24 - 30 MHz	50 Ω	5 pF	17 pF ± 10%
			7 pF	26 pF ± 10%
			9 pF	30 pF ± 10%
RC Oscillator (FLL based)				
C28SOI_RCOSCI_30M_32K_TRAC_LR_EG	30 MHz 45 MHz 90 MHz	-	-	-

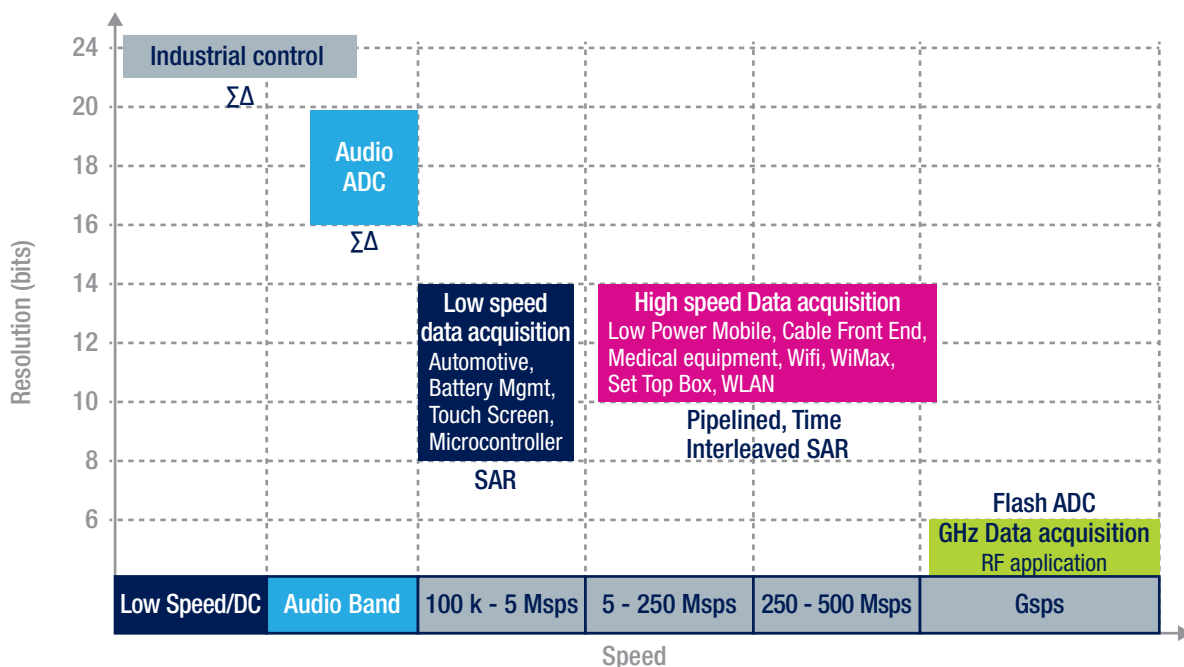
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ANALOG-TO-DIGITAL CONVERTORS (ADC)

In 28nm FD-SOI Technology, a broad portfolio of ADCs is available, supporting multiple resolutions and speed specifications.

The following features are supported in 28nm FD-SOI ADCs:

- Best-in-class PPA
- Multiple architectures available
- High speed (up to 64 Gsps)
- High Resolution (up to 24 bits)
- Available for various application and customizable on request



ADC	No of bits	Main features	Type
AD12PP160MIQ_10	12 Bits, ENOB 10 Bits	160Msps	Pipelined
AD12PP500M_10	12 Bits, ENOB 10 Bits	500Msps	Pipelined
AD10PP160MIQ_10	10 Bits, ENOB 9 Bits	160Msps	Pipelined
AD12PP5G_18	12 Bits, ENOB 10 Bits	5Gsps	Pipelined
AD12SA1MLA_18	12 Bits, ENOB 10 Bits	1Msps	SAR
AD9SA6G_18	9 Bits, ENOB 7.5 Bits	6Gsps	SAR
AD8SA64G_10	8 Bits, ENOB 6.5 Bits	64Gsps	SAR
AD14SA250K_18	14 Bits, ENOB 13 Bits	250Ksps	SAR

* Area & Power will be disclosed under NDA

Audio ADC	No of bits	Main features	Type
AD18ASDSE_18	18 Bits	SNR 98dB	Sigma Delta

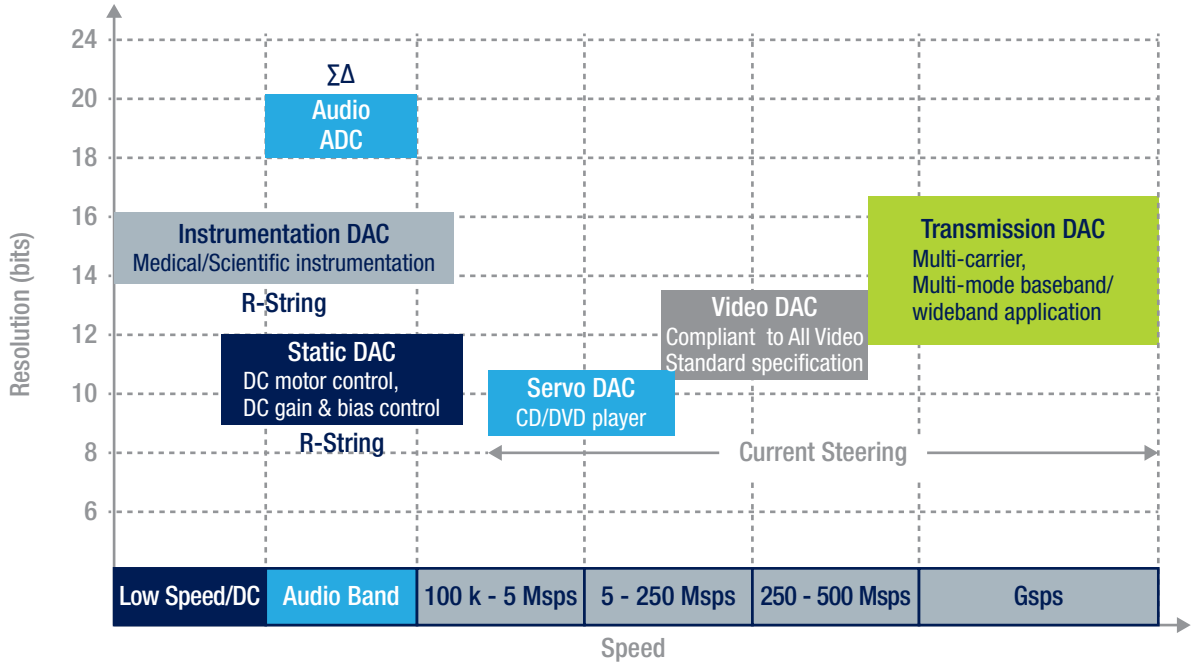
* Area & Power will be disclosed under NDA

DIGITAL-TO-ANALOG CONVERTORS (DAC)

ST's DAC portfolio for 28nm FD-SOI Technology, offers various resolutions and speed specifications for multiple applications.

The following features are supported in 28nm FD-SOI DACs:

- Best-in-class PPA
- Multiple architectures available
- High speed (up to 10 Gbps)
- High Resolution (up to 24 bits)
- Available for various application and customizable on request



DAC	No of bits	Main features	Type
DACI10HD3x1_1V8	10 Bits	Output current = 3.25 mA SFDR = 54 dBc @ 6 MHz	Current Steering
DA10HD6X4_18_C28SOI8M	10 Bits	Output current = 6 mA SFDR = 54 dBc @ 6 MHz Fs = 160 MHz	Current Steering
DAI10HD9X4CBLDET_1V8_EG8M	10 Bits	Output current = 8.7 mA SFDR = 54 dBc @ 6 MHz Fs = 160 MHz with cable detection	Current Steering
DACI10HF1DA3_1V8	10 Bits	Output current = 1.25 mA SFDR = 60 dBc @ Nyquist	Q-switching Current Steering
DACI10HD17T034X3_1V8_LL_R_EG8M	10 Bits	Output current = 17 mA to 34 mA SFDR = 54 dBc @ 6 MHz Fs = 160 MHz	Current Steering
DACI10HF10PC3_1V8_LL_R_EG8M	10 Bits	Output current = 1.25 mA SFDR = 60dBc @ 40 MHz Fs = 640MHz	Current Steering
DACI14HF3T020DA4CAL_1V8_EG8M	14 Bits	Output current = 3 mA to 20 mA SFDR = 70 dBc @ 210 MHz Fs = 750 MHz	Current Steering

* Area & Power will be disclosed under NDA

Audio DAC	No of bits	Main features	Type
DA24VASDLA_18	24 Bits	SNR 98 db	Sigma Delta

* Area & Power will be disclosed under NDA

EMBEDDED POWER-MANAGEMENT IPs

Embedded power-management IPs enable power optimization in SoC and ASIC designs through Body-Biasing, Power Switches, and Embedded Metrology cells.

Power Management IPs	Description
Body-Biasing IPs	
BBGEN_LLR_EG	Embedded Body Bias Generator with low power, low Vt and regular Vt process options
BBMUX21_LLR_EG	Embedded Body Bias Multiplexer with low power, low Vt and regular Vt process options
Power Switches	
EPOD_PLMEG_LLR_EG	Peripheral Embedded Power Distribution IP with Power Line Multiplexing feature and switch device EG
EPOD_PSWFBMP_LLR_EG	Peripheral Embedded Power Distribution IP with a switch device having Feedback and Modular Pre-charge features
Embedded Metrology Cells	
EMET_BE	Front-End embedded metrology structure
EMET_FE	Back-End embedded metrology structure

* Other electrical parameters will be disclosed under NDA

ONE-TIME-PROGRAMMABLE (OTP) IP: FUSE

OTP IP is a one-time programmable memory based on an anti-fuse cell with synchronous interface and dual-supply voltage. It is a non-volatile memory, with embedded programming capability and a specific programming sequence. In 28nm FD-SOI technology, memory cells support data storage using dielectric breakdown phenomena. All libraries embed a high-voltage charge pump and do not require an HV pad.

The OTP IP provides the following features in its 28nm FD-SOI technology variant:

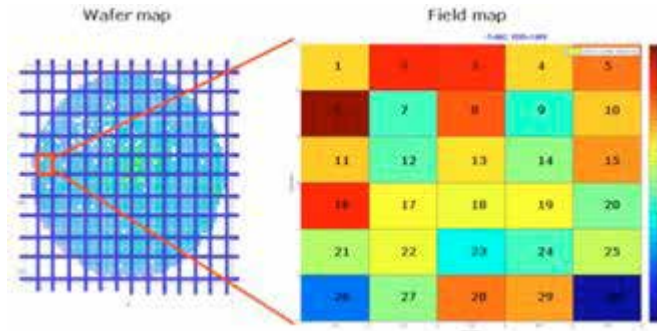
- **Dual supply:** 1.1 V & 1.8 V (includes an internal power switch)
- IPs in **multiple-metal stack** are respectively fully blocked
- **Storage capacity** of 1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16K bit.
- **Maximum clock frequency** (functional) is 120 MHz
- **Maximum clock frequency** (scan test) is 100 MHz
- **Mean programming time** is less than 10 us/bit
- **Programming lock** word-by-word.
- Static 16 bits data word available at power ON
- Word size:
 - **Standard with ECC correction:** 32 useful data by word (Default mode not incremental programming)
 - **No ECC, correction is done by redundancy:** 16 useful data by word (only for word requiring incremental data programming)

Library Name	Key Features/Specification
FU_OTP_LLR_EG	OTP anti-fuse library is designed in 28 nm FD-SOI technology

* Other electrical parameters will be disclosed under NDA

PROCESS-MONITORING BOX (PMB)

Process-Monitoring Sensors track the on-chip process fluctuations from fab-to-fab, wafer-to-wafer, and within-wafer using a unique die process ID to ensure the chip is within the pre-defined process limits (temperature monitoring, compensation and debug, and failure analysis).



	Library Name	Description
Sensors	GO2_LR_OD_18	Monitors the process of GO2 OD18 devices
	GO1_LL	Measures the SoC performance & helps to debug the failure analysis of chip, based on Low-Power & Low-Vt process option
	GO1_LR	Measures the SoC performance & helps to debug the failure analysis of chip, based on Low-Power & Regular-Vt process option
	CPR8T_LL	Contains 8-Track Critical-Path Replica (CPR) cells used for process compensation and voltage scaling
	CPR_LL	Contains 12-Track Critical-Path Replica (CPR) cells used for process compensation and voltage scaling, with three dedicated sensors, based on Low-Power & Low-Vt process option
	CPR_LR	Contains 12-Track Critical-Path Replica (CPR) cells used for process compensation and voltage scaling, with three dedicated sensors, based on Low-Power & Regular-Vt process option
	RCM5_COUP_LL	Monitors back-end process
Controllers	CONTROL8T_LL	8-Track Process-Monitoring Controller for on-chip compensation to save power, based on Low-Power & Low-Vt process option
	CONTROL_LL	12-Track Process-Monitoring Controller for on-chip compensation to save power, based on Low-Power & Low-Vt process option
	CONTROL_LR	12-Track Process-Monitoring Controller for on-chip compensation to save power, based on Low-Power & Regular-Vt process option
	CONTROL8T_LL_ASYNC	8-Track Process-Monitoring asynchronous controller with soft CPR, based on Low-Power & Low-Vt process option
	CONTROL8T_LR_ASYNC	8-Track Process-Monitoring asynchronous controller with soft CPR, based on Low-Power & Regular-Vt process option
	CONTROL_LR_ASYNC	12-Track Process-Monitoring asynchronous controller with soft CPR, based on Low-Power & Regular-Vt process option
	WRAPPER_LL	Contains controller logic for sensors used in process monitoring and on-chip compensation to save power

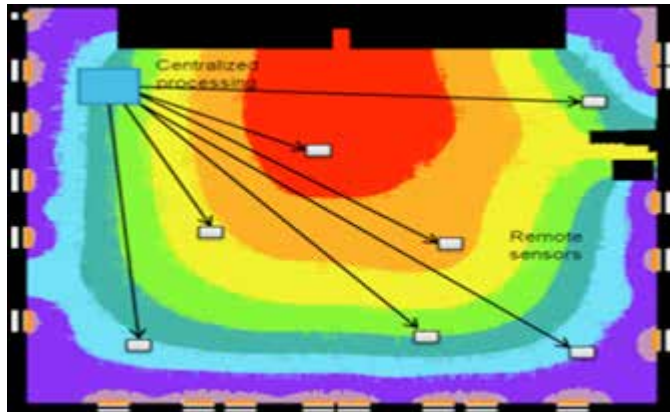
* Other electrical parameters will be disclosed under NDA

VOLTAGE & THERMAL SENSORS

Voltage Sensor library allows to embed voltage-measurement feature in SoC, and Thermal Sensor provides digital measurement of the junction temperature.

The advantages of using these sensors in 28nm FD-SOI technology are:

- Dynamic Frequency Scaling (DFVS) for high performance
- Thermal and Voltage profiling, security, thermal (fan) control
- IR-Drop Analysis, Smart power management



Sensor	Features/Specification
Low Area Temperature Sensor	<ul style="list-style-type: none"> • Measures on-chip temperature • Accuracy: ± 4 °C • Sense range: -40 °C to 125 °C • Suitable for small SOCs, safety features
High-Performance Distributed Voltage & Temperature Sensor	<ul style="list-style-type: none"> • Remote V & T sensing with centralized processing • Temperature accuracy: ± 1 °C over -40 °C to 125 °C • Voltage accuracy: ± 5 mV over 0.6 V - 1.25 V • Temperature-independent voltage-based calibration

* Other electrical parameters will be disclosed under NDA

LINEAR REGULATORS

28nm FD-SOI Linear Regulators offer flexibility to designers in terms of generated outputs from the required inputs thus delivering customized solutions, with other exciting features.

Regulator features in 28nm FD-SOI technology are:

- Customized solution for input & output voltages
- Configurable load current
- Low drop-out, <200 mV
- No external capacitance required
- Fast-transient response, High PSR
- Voltage-handling capacity higher than device breakdown
- Low-power mode for Standby
- Safety Features: Power-on-Reset, Supply monitoring, Over-current protection, Safe Startup

Regulator	Key Features/Specification
DC_LN_1V8TO1V0_PHY_EG	<ul style="list-style-type: none"> • Generates 1.0 V output from 3.3 V and 1.8 V inputs for various PHY IPs • Main input supply is from 3.3 V \pm10% and 1.8 V \pm 150 mV • Regulated output supply is 1.0 V \pm 100 mV
DC_LN_1V8TO1V0_USB_EG	<ul style="list-style-type: none"> • Supports main/input supply of 1.65 V - 1.95 V and digital regulated output supply: 1.0 V \pm100 mV • No off-chip capacitor required for regulator stability
DC_LN_1V81V0_STBY_LR_EG	<ul style="list-style-type: none"> • Generates multiple outputs (1.8 V, 1.0 V) from 3.3 V and 1.35 V inputs. • The regulated output supply is 1.0 V \pm 100 mV, which can be programmed down to 0.6 V, 1.8 V \pm 150 mV
DC_LN_2V51V81V0_LR_EG	<ul style="list-style-type: none"> • Generates multiple outputs (2.5 V, 1.8 V, 1.0 V) from 3.3 V and 1.35 V inputs. • Main/input supply1: 3.0 V - 3.6 V and DDR4 supply (1.2 V - 5% to 1.8 V + 10%) • Regulated output supply is 1.0 V \pm 100 mV, which can be programmed down

* Other electrical parameters will be disclosed under NDA

HIGH-SPEED SERIAL LINKS

A dedicated portfolio of High-Speed Serial Links is supported in 28nm FD-SOI technology.

Interfaces PHYs	Description
MIPIDPHY_MCNN_4MFAA_1500MBP_LR_EG	MIPI DPHY Master 4 DataLane
MIPIDPHY_SCNN_1SFAA_1500MBP_LR_EG	MIPI DPHY Slave 1 DataLane
MIPIDPHY_SCNN_2SFAA_1500MBPS_LR_EG	MIPI DPHY Slave 2 DataLane
USB2_1PHY	Physical layer of USB2 Host & Device ports
USB2_2PHY	Physical layer of USB2 Host & Device ports
USB2_3PHY	Physical layer of USB2 Host & Device ports
USB2PHY_S	Physical layer of USB2 Host & Device ports
OTG2	Adds host functionality to USB peripherals
HDMITX_3G4_1V8_LL_EG	Electrical layer of the HDMI Transmitter
HDMITX_6G0_1V8_LL_EG	Electrical layer of the HDMI Transmitter
MIPIDIGRF4GPHY_1TX2RX	Electrical layer of the DIGRF4G PHY transmitter and receiver
LVDS1V8_EG	Low Voltage Differential Signaling 1.8V IO in standard frame
DPTX_4L_IM5G4_1V8_LL_EG	Analog physical layer of DisplayPort transmitter
HDMIDPRX_5G4_3V3_LL_EG	DP/HDMI/DVI Combo Receiver

* Other electrical parameters will be disclosed under NDA

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