Repetitive voltage suppressors for overvoltage protection

The STRVS is the first TVS series to be specified against repetitive overvoltages in high temperature conditions

In applications, overvoltage constraints may not always come from lightning, electrical overstress or electrostatic discharge, but from the circuit itself. In such cases, standards do not apply.

Repetitive surges may raise protection device temperature. This is why protection devices must be selected according to their power capability at high junction temperatures and their clamping voltage specified at high temperature.

**KEY FEATURES**

- Application driven
  - 2 key parameters specified:
    - \( V_{CL} \) for multiple temperatures and peak current from 0 to 2 A
    - \( R_{D} \) for multiple temperatures and peak currents from 0 to 2 A
  - Application note supporting product selection
  - Improved power derating versus temperature

**TARGETED APPLICATIONS**

- MOSFET and IGBT protection in:
  - Solar inverters
  - SMPS and auxiliary power supplies
  - Smart metering
  - LED drivers

**KEY BENEFITS**

- Better Transil™ selection for cost optimization (oversizing avoided)
- Fixed and reliable clamping voltage not sensitive to output load
- Better protection with smaller package versus competition
- Reduced power consumption versus discrete protection (RC snubber)
- Customer design effort reduced
DESIGN NOTES
Design information and calculations are developed in detail in the application note “Design methodology of TVS in repetitive mode: STRVS”. Below, you will find a short summary of the steps to be considered.

1. \( V_{RM} \) selection
   The \( V_{RM} \) selected should be higher than the highest voltage at STRVS nodes during normal operating conditions.

2. \( V_{CL} \) @ 125 °C verification
   The designer should check that \( V_{CL} \) is low enough to protect the MOSFET during surges (assuming that 125 °C is the worst case application temperature).

3. STRVS temperature verification
   \( \bullet \) The power dissipated in the STRVS should be calculated.
   \( P_{step} = I_{peak} \times (3 \times V_{CL0} + 2 \times I_{peak} \times R_D) / 6 \)
   \( P_D = t \times f_{SW} \times P_{step} \)
   \( \bullet \) The calculated temperature has to be lower than 125 °C:
   \( T_{peak} = R_{th(j-a)} \times P_D + T_{amb} \)

APPLICATION KEY PARAMETERS

<table>
<thead>
<tr>
<th>Glossary</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{peak} ): Clamping voltage @ ( I_{peak} ) for a given temperature (25/85/125°C)</td>
<td></td>
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<tr>
<td>( V_{CL0} ): Voltage value where the ( R_D ) line crosses the 0 A axis</td>
<td></td>
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<tr>
<td>( R_D ): Dynamic resistance allowing designer to linearize the avalanche zone for ( 0 &lt; I &lt; I_{peak} )</td>
<td></td>
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<tr>
<td>( I_{peak} ): Maximum current flowing through the STRVS during each pulse</td>
<td></td>
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STRVS PROTECTION FOR ST COMPANION CHIPS
- VIPers
- HVLEDs
- Power MOSFETs
- ALTAIR

DEVICE SUMMARY

<table>
<thead>
<tr>
<th>Part number</th>
<th>( I_{max} ) max @ ( V_{max} ) (25 °C)</th>
<th>( V_{max} ) (typ. with ( I_{peak} = 1 ) mA)</th>
<th>Values @ 125 °C</th>
<th>Packages</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(µA)</td>
<td>(V)</td>
<td>(V)</td>
<td>( I_{max} ) (A)</td>
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<tr>
<td>STRVS118X02C(*)</td>
<td>0.2</td>
<td>85</td>
<td>100</td>
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<tr>
<td>STRVS142X02F(*)</td>
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<td>102</td>
<td>120</td>
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<tr>
<td>STRVS182X02F(*)</td>
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<td>150</td>
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<tr>
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<td>150</td>
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<td>154</td>
<td>180</td>
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<tr>
<td>STRVS252X02F(*)</td>
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<tr>
<td>STRVS280X02F(*)</td>
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<td>188</td>
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Note: (*): available in october 2012

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