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RHRPMPOL01

Rad-Hard Point-of-Load for Space Applications

7 A monolithic synchronous step-down regulator with high-precision internal voltage reference and integrated power MOSFETs for synchronous conversion.

Developed using Silicon-On-Insulator (SOI) technology, the RHRPMPOL01 offers good performance against Single-Event-Latchup (SEL) effect.
Housed in a FLATPACK-28 hermetic package, the device is designed to supply Field-Programmable Gate Arrays (FPGA), Digital Signal Processing (DSP), MCUs and Application-Specific Integrated Circuits (ASICs) for space applications.

KEY FEATURES

- 3.0 to 12 V input voltage range
- 0.8 V to (0.85 x VIN) output voltage range
- Up to 7 A output current

KEY BENEFITS

Large configurability to optimize design and reduce development time

- Programmable switching frequency from 100 kHz to 1 MHz
- Easy synchronization with 180° out-of-phase management (up to 2 ICs)
- Current-sharing configuration for higher load requirements

Maximum Protection

- Not-latched output over voltage protection
- Adjustable output overcurrent protection
- Input under-voltage protection
- Latched over-temperature protection

Radiation-hardened

- Total Ionizing Dose: 100 kRad
- Tested ELDRS-free
- SEL-free up to 70 MeV/mg/cm2 (@ Vcc up to 7 V)
- Proton free
- SEU-SEFI characterized up to Vcc 7V
- SET no performance degradation
- QMLV qualification ongoing

KEY APPLICATIONS

- Point-of-Load regulation
- FPGA, DSP, CPU and ASIC power supplies
- Low-voltage, high-density distributed power systems

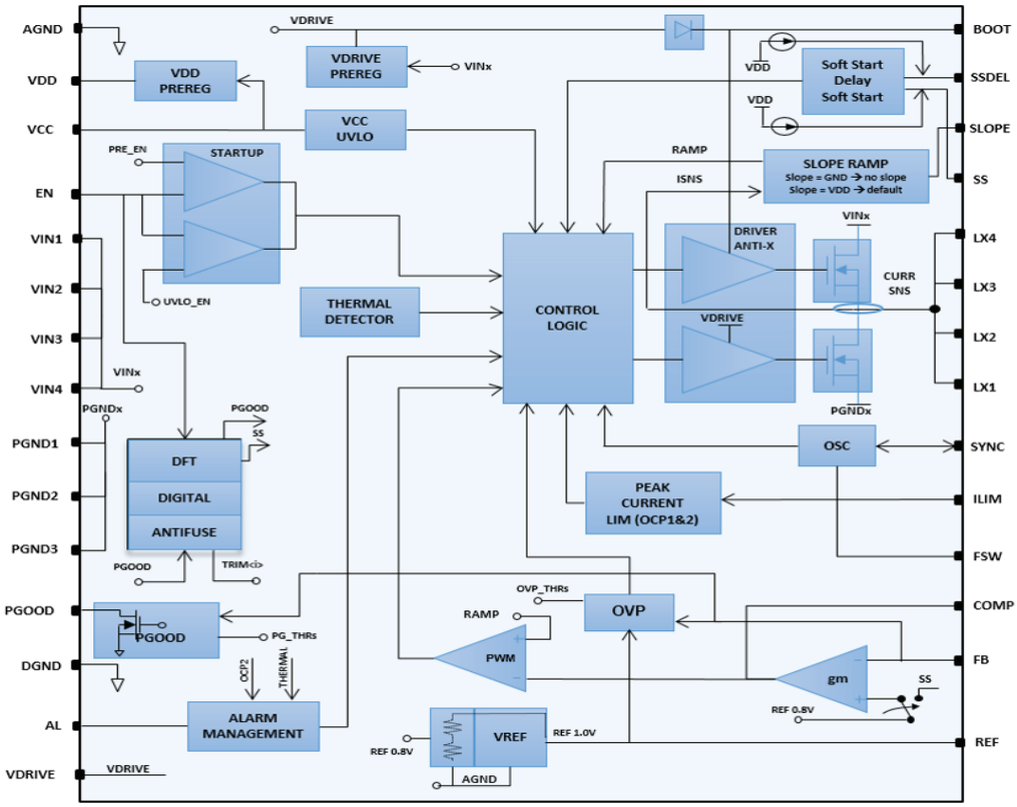
RHRPMPOL01

Synchronization & Interleaving

Two RHRPMPOL01 ASICs can each be configured in “master” or “slave” modes. The clock is synchronized by setting one IC as master (with a proper switching frequency) and the other as a slave, thus shorting its pin FSW to Ground (GND), and by connecting each device’s SYNC pin. The master device’s SYNC pin is configured as clock output and provides the internal switching clock frequency with a 180° phase-shifting.

If the device is defined as slave device, its SYNC pin is configured as clock input, and the device uses the clock signal received on the SYNC pin to synchronize its internal switching clock. Unlike interleaved configuration, the synchronized mode allows both devices to each have their own output and compensation network. Interleaved configuration doubles output current capability
and reduces the Root-Mean-Square (RMS) current absorption from the input filter.
More than two interleaved-configured devices (n devices, in general) can be connected to increase the output current capability even more. In this case, in order to ensure proper phase-shifting (360° per device), all devices must be configured in slave mode and be provided with an external clock signal.

RHRPMPOL01 BLOCK DIAGRAM



DEVICE SUMMARY

Order code	Quality Level	Package	Finishing	Packaging
RH-PMPOL01KPX	Evaluation Model	FLATPACK-28	Gold	Strip Pack
RH-PMPOL01KP1	Engineering Model	FLATPACK-28	Gold	Strip Pack

Note: QML-V qualification ongoing