The rising demand for data connectivity, cybersecurity and over-the-air updates of in-vehicle control units requires more processing power and uncompromised cybersecurity.

ST’s Telemaco3P system-on-chip provides a cost-effective solution for ensuring a secure connection between the vehicle and the cloud. Its asymmetric multi-core architecture provides powerful application processors as well as an independent CAN control subsystem with optimized power management. Its ISO 26262 silicon design, its embedded Hardware Security Module and automotive-grade qualification up to 105 °C ambient temperature, make it the best candidate for implementing a wide range of secure telematics applications supporting high-throughput wireless connectivity and over-the-air firmware upgrades.

**KEY FEATURES**
- Single or dual ARM Cortex A7 at 600 MHz (up to 2400 DMIPS)
- Embedded HSM implementing SHE+ extended specification
- Independent and isolated CAN subsystem on embedded ARM Cortex M3 with reserved eSRAM, running its dedicated RTOS
- 2 Gigabit Ethernet with AVB
- Multiple USB 2.0, SD/SDIO, CAN/CAN-FD, SPI, I2C, UART
- ASIL-B eligible
- Operating temperature range: -40 to +105 °C
- Integrated power management logic
- Power consumption in Standby: 20 μA
- Wake-up time < 50 ms

**SOFTWARE OFFERING**
- OS kernel and BSP: Linux / QNX
- Standard Yocto tools
- Pre-integrated open-source & 3rd party middleware for easy implementation
- Distributed RPMsg framework for secure inter process communication
- Bootloader toolset for custom / smart boot implementations
- FreeRTOS kernel and MCAL for AUTOSAR 4.2 on Cortex M3
- 3rd party support of Adaptive AUTOSAR on Cortex A7 cluster
**TELEMACO3P BLOCK DIAGRAM**

### Security
- HSM
- Crypto Kernel
- Mailbox
- Boot Code Authentication
- Tamper Detection

### Main CPU
- **L1-Cache**
  - CortexA7-600 MMU NEON FPU
- **L1-Cache**
  - CortexA7-600 MMU NEON FPU
- **L2 Cache**

### Connectivity
- 2x USB 2.0 / 1x HSIC
- SD/MMC/SDIO
- 2x Gigabit AVB Ethernet
- SPI
- I²C
- UART
- Gen. purpose ADCs
- I²S RXs/TXs

### Power Management
- Backup RAM
- SRCO
- PMU
- RTC
- Power On Reset
- Power Management Logic

### System
- **Interrupt controller**
  - Watchdog
  - JTAG
  - DMA
  - Timers/Counters
  - EFT
- **Microcontroller subsystem**
  - **Flash Cache 8 Kbytes**
  - **Cortex M3-200 Core**
  - CAN/CAN-FD
  - GPIO x16
  - Reserved eSRAM
  - Mailbox

### Microcontroller subsystem
- **3G**
- **LTE Modem**
- **V2X**
- **Tesla Automotive GNSS**
- **SRAM**
- **FLASH**

### External memory interfaces
- SPI NOR
- 16 bit // NAND
- 16-bit DDR3L 1066
- 16-bit LPDDR2 1333

### EXAMPLE SOLUTION

**Part number**
- **STA1375**
  - 1 A7 cores
  - 16-bit Memory Width
- **STA1385**
  - 2 A7 cores
  - 16-bit Memory Width

### OPERATING CONDITIONS
- **ARM_VDD**: 1.14V to 1.26V
- **VDD_IO_3V3**: 3.3V ±10%
- **VDD_IO_1V8**: 1.8V ±10%
- **VDDQ (DDR3)**: 1.35V ± 5%
- Operating temperature: -40/+105°C
- Automotive AEC-Q100 Grade 2 compliance

### PACKAGE INFORMATION
- 361-ball LFBGA (16 x 16 x 1.7 mm) package with 0.8 mm pitch

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