New System Solutions for Laser Printer Applications
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Introduction
Recently, the laser printer market has started to move away from custom OEM-designed \(^1\) formatter boards, where the brand manufacturer designs the complete system and outsources the mass production. Replacing this is an ODM \(^2\) approach, where external companies take charge of the entire system, including the design.

This trend began first in the low-end models, like host-based multifunction printers, but in the near future it will extend to the mid- and high-end models also, moving most of the system-level design from the brand manufacturer to external third parties, with expertise in specific areas.

This opens the market to companies with strong competence in ASICs and other areas needed to master the whole process and to offer a complete system solutions for laser printer brand manufacturers such as firmware, image processing, software, board design, test and qualification.

With a single external company undertaking the entire system design, the printer brand manufacturer is able to reduce the number of suppliers and take advantage of a tight synergy among different areas that consequently results in a shorter development time to launch new products on the market.

In order to be ready to provide best-in-class solutions, chip-design companies must establish strong partnerships with external companies with complementary skills, creating a team capable of producing a full working prototype of a formatter board, aimed at demonstrating the accumulated system level expertise.

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1 OEM : Original Equipment Manufacturer
2 ODM : Original Design Manufacturer
System description

In our lab, the initial goal was to replace the existing formatter board inside a laser printer bought on the market with a new one, entirely designed with a customized mass-market chip in order to achieve a higher level of integration and to reduce the overall cost of the BOM\(^3\) of the final board.

![Lab test bench and equipment](image)

**Fig. 2 – Lab test bench and equipment**

The reference printers were two low-end host based single function printer models:

- A monochrome printer with 600 x 660 dpi resolution, 20 ppm\(^4\), A4 paper format, costing less than $200
- A color printer with 600 x 600 dpi resolution, A4 paper format, costing around $450

We used the overall plastic chassis, the mechanics, and the complete laser engine of the two reference printers, in conjunction with the new formatter board, simply moving the flat cable of the original formatter.

![Formatter board replacement](image)

**Fig. 3 – Color (left) and B&W (right) formatter board replacement with our solution**

\(^3\) BOM: Bill of materials, a list of the components used on a board

\(^4\) ppm: pages per minute, average indicator of the speed of the printer
The prototype is based on a development board that includes an ARM9EJ-S® microprocessor, the standard and connectivity peripherals (DDR2 memory, USB 2.0 host and device, Ethernet IF, serial NOR Flash), and a Virtex 5 Xilinx® FPGA, used to implement the specific blocks needed to manage the serial interface and the laser engine controller.

The development board can be easily controlled by a run-time debugger on a PC, connected with a hyperterminal serial interface and supporting a JTAG debugger to allow firmware development.

![Diagram of the prototype system](image)

**Fig. 4 – The overall prototype system**

An adapter board was designed to connect the development board with the specific connectors required by black and white and color laser engines chosen for the test. The adapter fits these two models widespread on the market, but it can be easily modified to be compliant with other models, on customer demand.

**Hardware**

The core of the system is a SPEAr600 device that provides the main architecture built around the ARM9EJ-S® microprocessor and a set of standard peripherals connected with an AMBA bus. The following are the main features of the device:

- Dual ARM926 (DC 16KB, IC-16KB) running up to 333 MHz
- Memory controllers
  - DDR1/DDR2 controller
  - Serial Flash controller
  - Parallel NAND controller
- Connectivity
  - USB 2.0 device
  - 2 x USB 2.0 hosts
  - Ethernet 10/100/1000
  - UARTs, I²C, SPIs, IrDA
- Customizable logic: 600 Kgates + 128 KByte of SRAM memory
- Boot ROM: 32 KB
- Color LCD controller
- JPEG codec
- Spread spectrum clock
- ADC: 10-bit, 8 channels, 1 Ms/s
- 8 channels, general purpose DMA
- Real time clock, timers
- Multi-layer interconnect matrix

Additional application-specific blocks can be hooked to the main structure in a very flexible way: during the initial design and debug the new blocks can be implemented in an external FPGA connected to the bus via a port controller to synchronize the bus; then, in the final product, the blocks are moved into the customizable logic block, and the port controller is switched off.

![Image](image.png)

**Fig. 5 – The development board (right) and adapter for laser engine (left)**

The customization of the gates of the generic device for a specific target application can be quickly implemented with a metal layer turn, at half the cost and diffusion time required for a standard ASIC.

The main blocks implemented in the FPGA are the following:

- Four laser video outputs (LVO) drive the laser beam in the engine; one LVO is dedicated to each of the three primary colors and one for black. The data flow (4-bit per pixel in CMYK format) is transferred from the DDR memory to an internal 32 words buffer by a local DMA and then sent to the LVDS buffers on the board, to directly fire the lasers. The blocks are highly configurable to allow different paper size,
margins, and resolution, and they also include 16-words registers for resolution enhancement tables.

- The laser-jet interface (LJ IF) uses a 16-bit serial protocol (data/clock) to manage the communication between the ASIC and the laser engine. It transmits all the commands (to move paper, enable and fire the lasers to print) and receives the different status conditions from the laser engine (for example: paper empty, paper jam, toner low...) In addition, the block includes a clock pre-scaler to run at different frequencies and parity check, timeout and errors conditions management.

- The DMA with 4 independent datastreams, one for each color layer, is able to manage a full A4 format page in a single transfer, with data packets of 16-words burst. Also the DMA is highly configurable to meet most of the data management constraint from different engines.

- The interrupt controller manages seven interrupt sources generated by the blocks inside the FPGA (4 LVOs, LJ IF, DMA, GPIOs) and conveys them to the main controller/arbiter of the device.

- Thirty-two general-purpose configurable IO's to manage LEDs and buttons on the control panel or probe internal signals for debug purposes.

The FPGA was successfully tested up to 68 MHz frequency versus a target frequency of 66 MHz; in other words, a quarter of the microprocessor clock.

The blocks of the laser subsystem, designed for the demonstrator, are the starting point for the development of more complex IPs and can be easily enhanced with graphic accelerators and other customer-specific features.

Fig. 5 – FPGA with the laser printer specific blocks

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5 IP : Intellectual Property
**Firmware and software**

The structure of the firmware is conceived in the same modular way, in order to be reused as a basic backbone, onto which can be added other parts, specifically developed by customers.

The main subsystems are the following:

- Thread-X<sup>®</sup> real time operating system, with file system and top level scheduler
- Drivers of the main peripherals and connectivity like USB device, DDR memory controller, and DMA for data flow management.
- Laser video output for page format and laser firing control.
- Laser interface for full bi-directional communication protocol with the engine.

**Windows ® SDK Host**

<table>
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<tr>
<th>Printer Drivers</th>
<th>Host Printer Code</th>
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**Embedded Firmware**

- Real Time Operating System
- File System
- USB 20 Device
- Laser Video Output
- Scanner Subsystem
- JPEG Image Stages Subsystem
- PDL Language Subsystem
- FAX Subsystem

Complete Firmware Library

In addition, the firmware can be enhanced with other blocks available in the libraries of the whole device family to extend the connectivity to USB Host and Ethernet 10/100/1000 or to increase the printing quality and speed with more sophisticated image processing algorithms.

Finally, a simplified user interface running on the host manages a complete B&W and color software driver, developed from the standard Windows<sup>®</sup> SDK. It can support A4 and letter paper formats, color space conversion, and different half-toning algorithms, such as blue noise masks.

**A new family of devices for laser printer applications**

The whole system architecture, currently at FPGA level, is quickly portable onto silicon with a low-cost metal-layer customization for medium/low volume products or with a standard ASIC for high volume.

A new family of formatter boards, based on a unique highly configurable ASIC, assembled in three different SiPs<sup>6</sup> together with 2, 8, and 32 MB DRAM cuts, each of them with its own specific firmware and software, could address the needs of three potential products: a low-cost monochromatic printer, a color printer, and a network color single function laser printer.

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<sup>6</sup> SiP : System in Package, ASIC and memory dice in the same package
The assembly of the ASIC and different DDR memory cuts in a single package (SiP) gives high flexibility, allowing adaptation to different platform requirements using the same device. The target packages (TFBGA 148 + 16 12x12x1.2 or LFBA 168 + 25 15x15x1.7, depending on the number of pins required by the customer application) enable significant reduction of the cost.

In addition, the accurate placement of the memory controller logic, the delay line, and the pads (on the ASIC side) very close to the DDR memory dice, with short wire connections, remove most of the signal integrity issues on this critical interface and turn out in a simplified board design. The trials with the schematic of a case-study board, with medium level of complexity, demonstrate that it can be routed in a single layer.

**System Performance**

The extensive lab tests showed good results in terms of printing quality and speed. A complete test suite, with B&W and color pictures, text, drawings, and graphics was used to compare the output of the two printers under evaluation with our solution. The same test images were sent first to the printers with their own genuine formatter boards, firmware, and software drivers, and then the test was repeated replacing the whole system with our solution.
For monochrome pictures, text, and graphics our prototype ran at 7.5-8.5 ppm (depending on the kind of image) for a single page and 19 ppm for a continuous pipelined multiple page prints, which was the same speed of the first printer purchased on the market.

For color pictures and drawings, our solution ran at 2.6-2.7 ppm for both single page and multiple pages. The single page ppm count is the same as the reference printer, but for multiple pages, the ppm was just half the value of the reference printer.

The existing gap is due to the non-optimized management of the pipelined data flow in this specific condition. This is a temporary, well-understood limitation of the current prototype, and could be fixed as part of an overall review of the system during the definition of a new real product.

**Conclusion**

Taking advantage of the wide flexibility and full reliability of the existing platform, laser printer brand manufacturers, including those who have low-volume production and can’t afford the cost of a specific ASIC, can easily and quickly launch new products with performance in terms of image quality, speed, and ease of use, comparable with the best products on the market.

In addition, with the system solution approach, printer manufacturers are free to focus only on their specific product differentiators, since they can leverage and rely on an extensively-tested platform and get support from company’s experience in this area.

Our prototype and the complete development kit are available for customer demos and can be released for evaluation or initial development activity.