AN2344
Application Note

Power MOSFET avalanche characteristics and ratings

Introduction

Back in the mid-80s, power MOSFET manufacturers started to claim a new outstanding feature: Avalanche Ruggedness.

Suddenly, new families of devices evolved, all with this “new” feature. The implementation was quite simple: the vertical MOSFET structure has an integral body drain diode which cannot be eliminated. By changing some process and layout parameters, it is possible to guarantee the use of the clamping capability of this diode for withstanding accidental voltage/power surges beyond the nominal drain source voltage.

Rating ‘ruggedness’ in a datasheet was very difficult because of the great confusion regarding the meaning of this feature, as well as poor theoretical knowledge of it. Nonetheless, all of the Power MOSFET manufacturers started to produce avalanche-rated devices and propose datasheet ratings (although imperfect), to protect themselves and the end users from this incomplete knowledge.

Now, knowledge about a device’s behavior during avalanche conditions is greatly enhanced by a number of application notes and papers issued, which provide different explanations of avalanche ratings and behavior. This application note briefly reviews the MOSFET physics on avalanche behavior and supplies designers with tools and suggestions for dealing with avalanche issues.

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1 MOSFET fundamentals

Figure 1. shows a basic, simplified MOSFET structure. The actual MOSFET is an infinite parallel of these 'microscopic ' structures that work together, sharing the same Drain with all of the Gates which are connected together by a deposited polysilicon mesh, and all of the Sources are linked by the top metal layer.

In this case, the 'mesh' is the ST-patented, high voltage Mesh Overlay™ technology, which optimizes the body-drain junction shape as well as improves other aspects of the MOSFET structure. However, the overall concept of this vertical structure can be considered valid for various older technologies (e.g. cellular) as well.

During the ON state, while the gate source voltage is above the threshold, the conduction current is localized in the drain and the region below the gate (channel). During the OFF state, the voltage drop across the drain and source is sustained by the PN junction at reverse bias, and a very small current (leakage) flows through the junction.

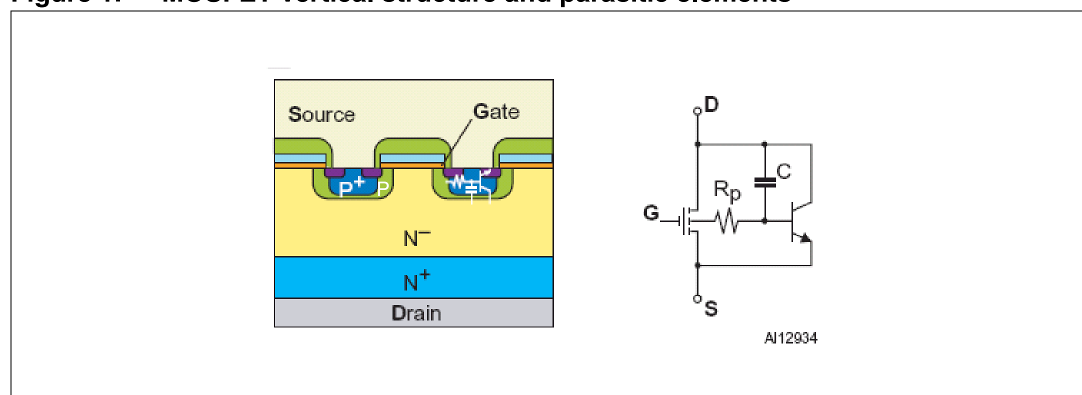
If the voltage increases too much and the electrical field reaches the critical value, the junction goes into breakdown, and the current starts to flow through the body region. If an overvoltage is applied to the junction, a current flows through it while the MOSFET limits the actual drain-source breakdown voltage.

The breakdown mechanism itself is not destructive for a PN junction. However, overheating caused by the high breakdown current and voltage damages the PN junction unless sufficient heat sinking is provided.

Looking at the MOSFET structure, one can see that the PN junction is not a simple or perfect diode. The MOSFET diode is the collector-base junction of a Bipolar Junction Transistor (BJT), also called the parasitic transistor, made by the N^+ region of source, P/P+ region of the body, and N^+ region of the drain, with the base shorted to the emitter by the front metal.

The capability of a MOSFET to withstand the avalanche condition takes into account these concerns. In fact, two kinds of failure arise: one is related to current, and the other to power dissipation. In the former, failure is caused by the latching of the parasitic bipolar due to the current that flows through its base resistance, multiplied by the gain. The second is reached when the temperature of the junction rises to a critical value that provokes the formation of hot spots caused by regenerative thermal runaway, with average temperatures of about 650°C, that peak at approximately 1000°C, which then triggers extremely rapid device destruction.

Figure 1. MOSFET vertical structure and parasitic elements



1.1 Failure modes descriptions

The integral diode of a MOSFET is the collector-base junction of the parasitic transistor. If the current flows laterally through region P, the increase in the voltage drop across the emitter base resistance causes the BJT to turn ON.

The initial avalanche current is concentrated mainly in the diode localized in the deep zone of P+; as soon as the current grows, it begins to interest the more lightly doped P regions. Since, by design, the lateral resistance RP value is higher than that of the heavy doped P^+ region vertical resistance, and the current is concentrated in the region P^+, the BJT should not turn ON.

As soon as the current begins to stimulate the P region, causing a sufficient drop of voltage to equal the BJT base-emitter voltage (V_{BE}), the base current (I_B), in conjunction with the transistor β will cause the BJT to turn ON. The V_{BE} has a negative temperature coefficient, consequently leading to thermal runaway and finally, the destruction of the device due to the secondary breakdown of the parasitic BJT. The adoption of a heavily doped P^+ region, thereby determining the reduction of the transistor gain and base resistance has been the first step for MOSFET improvement, followed by other, more subtle optimizations.

The power that is dissipated in the MOSFET causes an increase in junction temperature. If the temperature increases to a critical value set by the siliconfs property, the failure, without the contribution of the parasitic bipolar, occurs because of the creation of thermally generated carriers in the epitaxial/bulk region, which in turn, create the hot spots. The critical temperature to have phenomenon is beyond the maximum junction temperature of the devices, and is related to the intrinsic temperature of doped silicon, to which the concentration of the bulk is equal to that of the thermally generated carriers.

The temperature increase that occurs during avalanche phenomena, due to the silicon thermal capacitance, is not instantaneous. Therefore, this type of failure should be distinguished from that caused by current as the device holds the breakdown voltage for a finite time before its destruction.

2 Testing avalanche ruggedness

The avalanche capability of the device is usually evaluated by using a circuit that performs an Unclamped Inductive Switching (UIS) operation like the one shown in *Figure 2.* The operation is as follows:

1. At zero time, the device switches ON, closing the circuit.
2. The current increases following an exponential law as a function of the L/R characteristics of the circuit, which are caused by the presence of an inductance, given some resistance due to the layout and the MOSFET ON resistance ($R_{DS(ON)}$).
3. As soon as the device is switched OFF, the dI/dt causes an overvoltage on the drain of the device because the magnetic field in the inductance cannot instantaneously go to zero (see *Figure 3.*).

Figure 2. UIS reference diagram

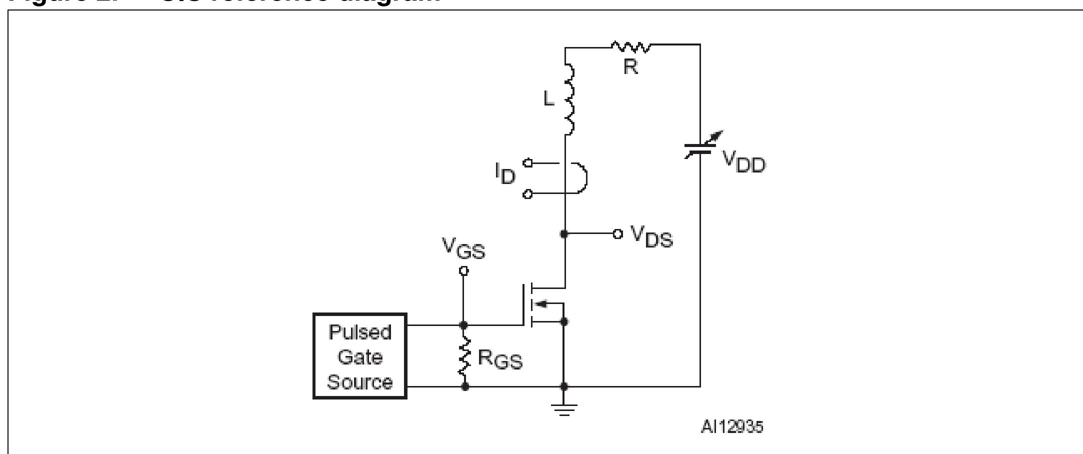
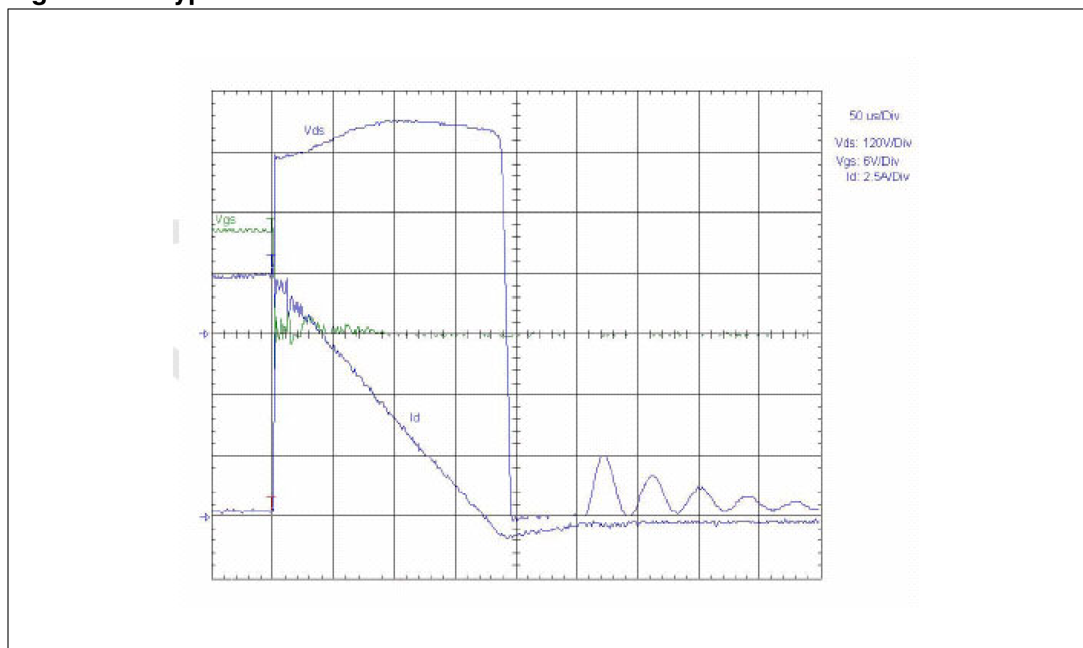


Figure 3. Typical UIS waveforms



The device is essentially an open circuit up to its own blocking voltage, therefore the extra voltage is limited by the BV_{DSS} of the device under test (DUT). During the Avalanche, the current flows through the DUT, dissipating the accumulated energy that was stored in the coil during the charging operation. *Table 1.*: UIS circuit equations on page 8 explains several relations for the t_{AV}, E_{AV}, and the P_{AVG} with several circuit configurations. A device is commonly defined rugged, or avalanche-rated, if during some stated coil and conducted current conditions, the device survives this test.

In the past, circuits like the one in *Figure 4.* were recommended to test for this capability. The current is maintained constant for a set time, eliminating the requirement for the coil. However, the only recognized method is to use the circuit described in *Figure 2.* (per JEDEC standard No. 24-5, MIL-STD750D method 3040.2).

A circuit commonly used to test the avalanche ruggedness of the MOSFET is shown in *Figure 5.* Its special feature is a power switch in series to the V_{DD} that connects the voltage source to the circuit only during the coil charging, disconnecting it a few microseconds before the switch-off and the avalanche operation. This technique allows the user to increase the V_{DD} beyond DUT's maximum rated V_{DS}, which speeds up the charging of the coil during turn-on, and consequently decreases the turn-on state time. Also, the energy dissipated is different (see *Table 1.*).

Figure 4. Constant current avalanche fixture

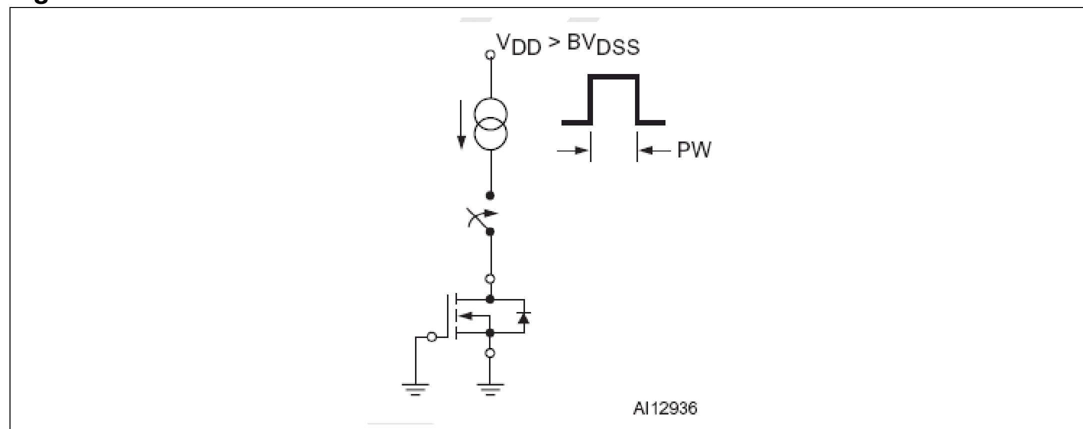


Figure 5. Disconnected supply UIS fixture

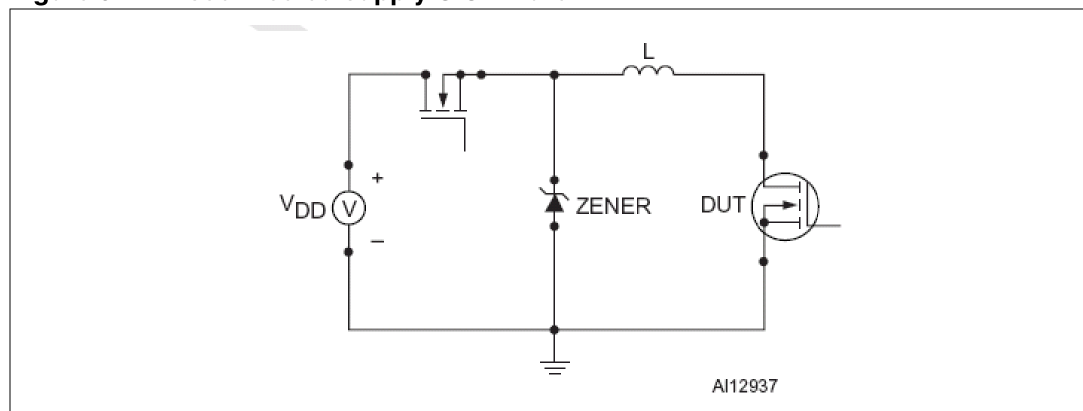


Table 1. UIS circuit equations

Circuit condition during avalanche		t_{av}(s) Time in avalanche	Avalanche energy (J)	Avalanche power (W)
R	V_{DD}			
0	V_{DD}	$L\ I_O/(V_{DS}-V_{DD})$	$0.5\ L\ I_O^2\ V_{DS}/(V_{DS} - V_{DD})$	$0.5\ I_O\ V_{DS}$
0	0	$L\ I_O/V_{DS}$	$0.5\ L\ I_O^2$	$0.5\ I_O\ V_{DS}$
R	V_{DD}	$(L/R)\ln[1/\ln(1+1/\Psi)-\Psi]$	$(L\ I_O\ V_{DS}/R)[1-\Psi\ln(1+1/\Psi)]$	$I_O\ V_{DS}\ [1/\ln(1+1/\Psi)-\Psi]$

Legend:

V_{DS} Device breakdown voltage constant during avalanche

I_O Peak current during avalanche

L Inductance

R Coil series resistance

V_{DD} Circuit supply voltage

Ψ The ratio of the inductor plus the resistor voltage to the resistor voltage drop: $(V_{DS} - V_{DD})/(R \bullet I_O)$

3 Datasheet avalanche ratings

When the device is classified as gAvalanche Ratedh, the datasheet provides the end-user some useful parameters which define the ratings of the device during avalanche:

- Avalanche operation maximum current (I_{AR})
- Energy during Avalanche for Single pulse (EAS)

3.1 Avalanche operation maximum current (I_{AR})

This is the maximum current that can flow through the device during avalanche operations without the BJT latching. This Maximum limit must be considered as an absolute maximum rating. Even if the critical current to bring the device to failure is higher than the I_{AR}, the producer guarantees the operation of the device below this limit. This test is usually conducted for several microseconds. All of ST's High Voltage Power MOSFETs are tested according to the I_{AR}.

All the avalanche operations (single event or repetitive) below this current value can be considered safe unless there are power dissipation issues.

Note: For MOSFETs connected in parallel, the current that is switched during the avalanche phenomenon is not shared, which is different than operations in the conduction state. In fact, at turn-off, only the device with the lower breakdown and/or with the faster switch will go into avalanche, withstanding the total current that is shared with the other MOSFETs in parallel during the ON state.

If such current is more than the I_{AR}, the device can fail. Even if the energy associated with that event is very low, failure would be due to the activation of the MOSFET's parasitic bipolar.

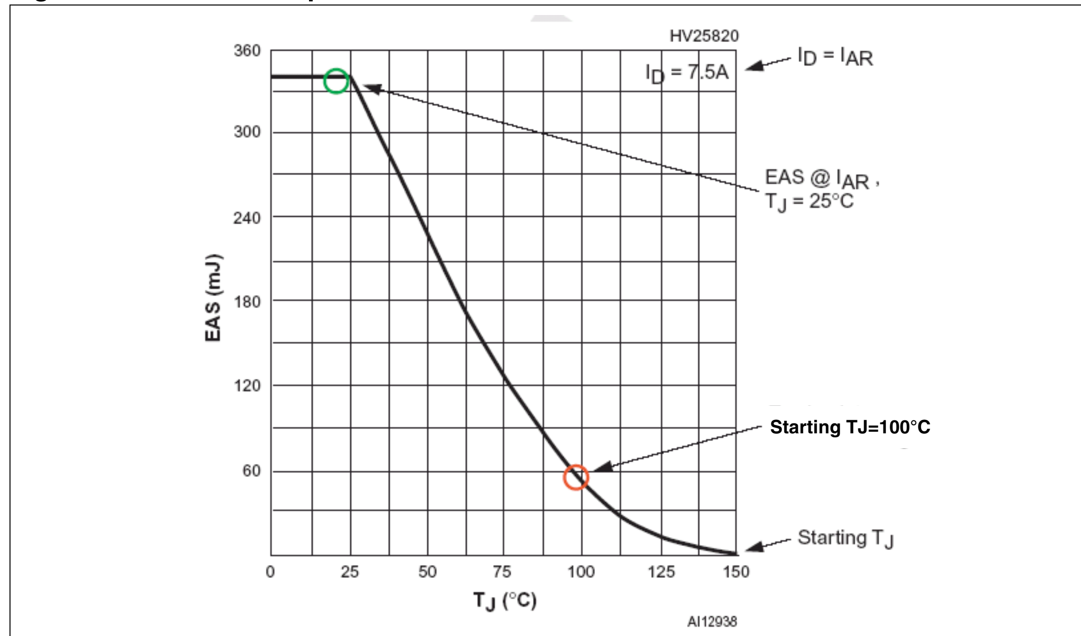
3.2 Energy during avalanche for single pulse (EAS)

This is the maximum energy that can be dissipated by the device during a single pulse avalanche operation (at the same circuit conditions described in testing avalanche ruggedness. From the I_{AR} and starting junction temperature of 25°C, the junction temperature is brought up to the maximum that is stated in the absolute maximum ratings.

The EAS value decreases as the starting junction temperature increases. In most datasheets, this energy derating curve (see *Figure 6.*) is referred to as “Avalanche Energy vs. Starting T_J”.

In the case of *Figure 6.*, all of the single event avalanche operations below the EAS value are considered safe for the device, if the junction starting temperature is 25°C, then the drain current is switched to less than or equal to I_{AR}. If TJ > 25°C, the user can refer to this curve to obtain the correct energy dissipation derating.

Figure 6. EAS vs temperature STP9NK80Z



3.3 Avalanche rating example

In this example, a user wants to use an STP9NK80Z as a DC/DC converter main switch. The datasheet ratings of this particular device are:

- EAS = 350mJ,
- I_{AR} = 7.5A, and
- $T_{J(max)}$ = 150°C.

According to the board analysis, the device used for such power supply condition can experience a single pulse avalanche operation. The measurements have shown that the average junction temperature is 100°C, the peak drain current switched during the avalanche is 4A, and the energy that is dissipated during that single avalanche operation is 0.24mJ.

To understand if the device is working within the datasheet ratings, the switched current needs to be checked by comparing it to the I_{AR}; because the I_D peak value is 4A and below the I_{AR}, this rating is satisfied.

To confirm that T_J is below $T_{J(max)}$, it is assumed that T_J before the avalanche is average (100°C). *Figure 6.* shows that the energy it takes to bring T_J to the maximum rating (starting from 100°C) is approximately 50mJ. Since the energy measured is below 50mJ, the T_J reached during the avalanche will be less than $T_{J(max)}$. Considering that both of the bonds, the current below I_{AR} and the T_J value below the $T_{J(max)}$ are well satisfied, one can safely state that the device (under that single avalanche event) is working within the datasheet ratings.

Each MOSFET manufacturer (including ST) presents their own approaches to measuring EAS values, as well as their findings. These values are not simple to state because it is very difficult to look at T_J during an avalanche operation. In order to provide as clear an explanation as possible, some manufacturers set this value by using the thermal impedance stated in the datasheet. This could be an interesting approach, but some concerns would

have to be taken into consideration. These are mainly systemic in nature because the datasheet thermal impedance is the response of the userfs system to a rectangular power pulse, while maintaining the package case temperature at 25°C. This response can be expressed as follows:

Equation 1

$$\Delta T_{jc} = Zth_{jc}(t)P$$

where,

ΔT_{JC}= Change in junction-case temperature

Zth_{JC}= Rectangular pulse derived from triangular pulse

t= Triangular and Rectangular response time, and

P= Power dissipated

The application of *Equation 1*, without any modification cannot give precise information. In fact, a comparison between a rectangular and a triangular power pulse (both with the same peak), indicates that the peak temperature between them is quite different (see *Figure 7.*). To use the Zth, the triangular pulse can be approximated as rectangular pulse, with scaled amplitude and width.

Another important concern about the use of thermal impedance is that usually it is experimentally and theoretically calculated according to the ON state of the device, so the normal power distribution within the device may be different from the one that occurs during the avalanche state.

ST's approach to an EAS statement starts from a theoretical thermal model of the die with some experimental verifications. The $T_{J(max)}$ during an avalanche may be sterting from:

Equation 2

$$T_j = \frac{P_0}{AK}\sqrt{t_{av}} + T_{starting}$$

where:

t_{AV} = Avalanche time (s),

A = die area (m^2),

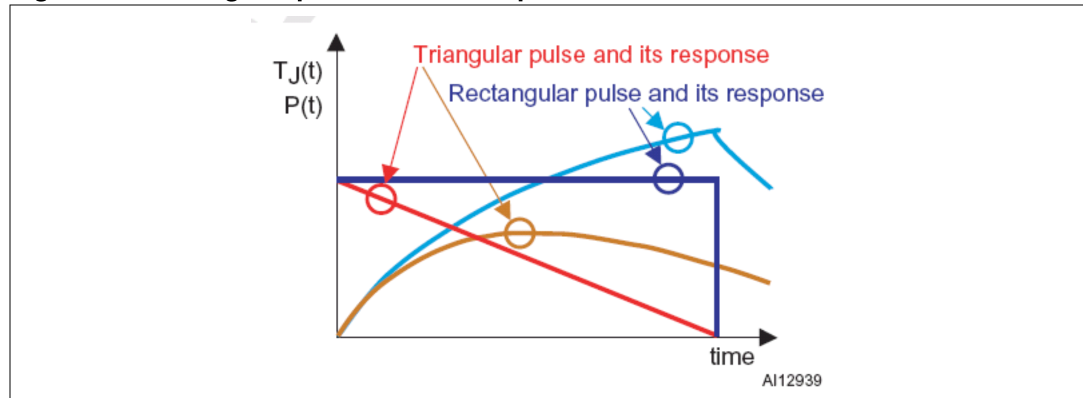
P_0 = peak power (W), and

K= the silicon‘s thermal constant ($Wm^{-2}\ s^{1/2}\ K^{-1}$)

This solution is derived from the general heat transmission equation (Fourier equation) for the special case where an infinite media (mono-dimensional case) is subordinated to a short rectangular power source pulse and uniformly distributed over a die area.

Equation 2, when it is applied to a triangular power pulse, is a simple and good approximation to use for the temperature increase calculation within the device during the avalanche operation, if the pulse is of short duration.

Figure 7. Triangular pulse thermal response



Starting from this model, the experimental verification is made looking to the V_{DS} shape during the avalanche. In fact the breakdown voltage of the device is not constant when varying the temperature and the current.

The variation of the blocking voltage with the current is nearly linear, and this resistance is specific to the die size per a given set of design rules, the epitaxial layer, and the package.

Figure 8. shows the measured characteristic of BV_{DSS} versus the I_D for a 700V device. The voltage variation with the temperature is positive as well, and the variation depends on the structural characteristics of the silicon die. By taking these items into account, the T_J can be extrapolated from the V_{DS} curve.

Figure 8. BV_{DSS} vs I_D

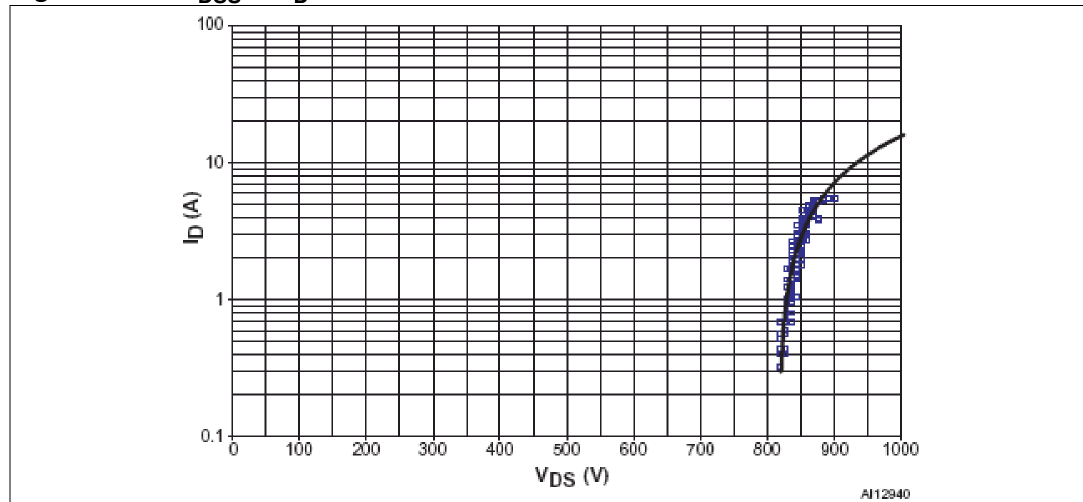
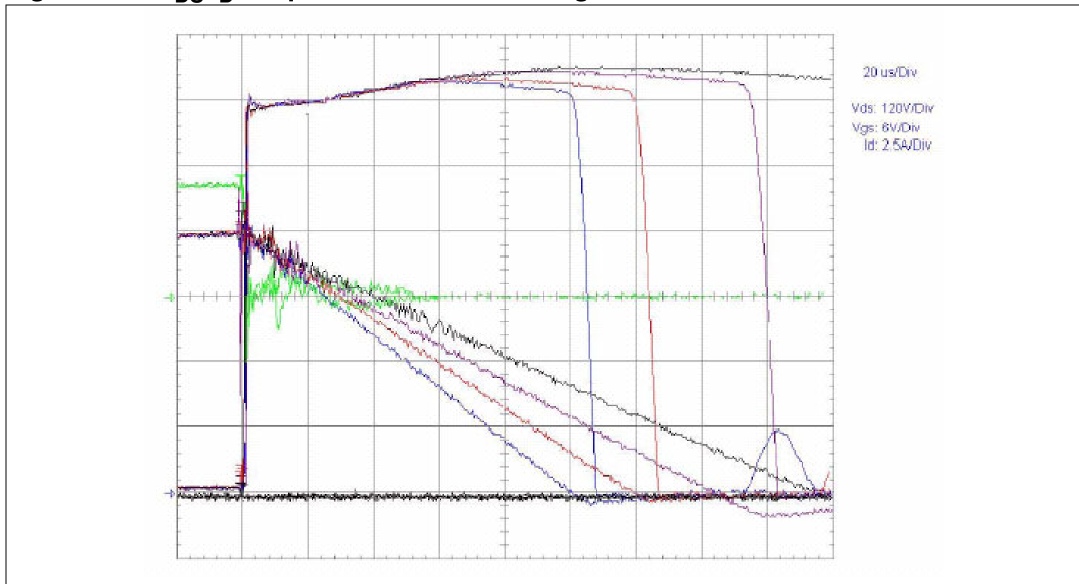


Figure 9. shows the actual V_{DS} curve during an avalanche, where the increase of V_{DS} observed is due to the rise of the silicon temperature. *Figure 9.* also shows the waveforms for the same device as it is subjected to different coils (i.e. different energy levels) at the same peak current.

The different V_{DS} shapes are due to different maximum temperatures reached by the junction. The linear relationship of the V_{DS} with the die temperature becomes clear when comparing the V_{DS} quasi-parabolic shape to the temperature profile for a triangular power pulse (see *Figure 7.*).

Figure 9. V_{DS}/I_D shapes with the Coil during the UIS



3.3.1 EAR (Energy during avalanche for repetitive pulse)

Often stated in the datasheet, this value is defined as the energy at IAR during repetitive operation, and the value is usually calculated with a 10KHz power pulse train with a 50% duty cycle and the nominal power rating of the device (see Equation 3).

Equation 3

$$EAR=power/f$$

For instance, if the available power of the MOSFET (P_D in the datasheet) is 150W, the EAR should be equal to 15mJ. However, this value is redundant and not very useful for the design, as it gives very poor information about the maximum energy to be dissipated and keep T_J below $T_{J(max)}$. A quick way to evaluate the temperature during avalanche is to take into account the extra power dissipation introduced by the repetitive avalanche, and to calculate the heat sink size required to dissipate it. Because of a triangular pulse:

Equation 4

$$E = \frac{1}{2}VI \bullet t_{AV}$$

And the additional average power to be dissipated is expressed as:

Equation 5

$$P_{AV} = E \bullet f= \frac{1}{2}VI \bullet t_{AV} \bullet f$$

where,

f= Frequency (see *Equation 3*),

t_{AV}= Avalanche time,

V= Peak voltage, and

I= Peak current

The total power includes the power conduction (P_{COND}) and switching (P_{SW}) losses:

Equation 6

$$P_{TOT} = P_{COND} + P_{SW} + P_{AV}$$

The STW9NK80Z is used again as an example (see section *3.3*), however, in this case, the avalanche is not a single event, but is repetitive, with a frequency, f=50kHz.

For the single event example, when the current is below I_{AR} and the T_J is below 150°C, the device works in a safe operating mode. When the device is subjected to repetitive avalanche events, it needs to be checked to see if it maintains the T_J below 150°C. Since power dissipation for each avalanche pulse is 0.24mJ, the average avalanche power dissipation is expressed as:

Equation 7

$$P_{AV} = E \bullet f = 0.24mJ \bullet 50kHz = 12W$$

If the device has a junction-to-ambient thermal resistance (R_{thJA}),

Equation 8

$$R_{thJA} = R_{thJC} + R_{thCS} + R_{thSA} = 10°C / W$$

and the average switching and conduction losses equal to 2W,

Equation 9

$$P_{TOT} = P_{COND} + P_{SW} + P_{AV} = 2W + 12W = 14W$$

then the average temperature is calculated as follows:

Equation 10

$$T_J = P_{TOT} \bullet Rth_{JA} + T_A = 140°C + T_A$$

Given that the average temperature and peak temperature during the avalanche should be higher, it is clear that the avalanche phenomenon is generating power so high that the system thermal behavior cannot dissipate in order to maintain the T_J below $T_{J(max)}$.

The only solution is to reduce the thermal resistance of the system by changing the heat sink or redesigning the application to avoid the avalanche failure.

In order to obtain a more accurate computation, the only way to evaluate the maximum temperature during repetitive avalanche is to calculate it by the Zth of the system. Despite all the concerns already discussed about adopting the published Zth for the avalanche (see *Equation 1*), the computation results for repetitive avalanche as given by manufacturers are sufficiently guardbanded for real world applications.

Several methods can be used to find the steady-state maximum temperature during a steady-state or after a finite number of avalanche occurrences.

The most frequently and sufficiently conservative equation used in order to find the maximum temperature for periodic rectangular power pulses at steady-state is:

Equation 11

$$\Delta T_{JC(max)} = P_0\left(\frac{t_p}{T}R_{thJC} + \left(1 - \frac{t_p}{T}\right)Zth_{JC}(t_p)\right)$$

Where,

P_0= Peak power,

T= Period of the pulses train, and

t_p = Power pulse width.

Considering the repetitive avalanche application (but it can be applied to several operative modes) the calculation of the peak temperature must also take into account the conduction and switching losses. *Figure 10.* shows the power profile of a typical switching, while *Figure 11.* illustrates the superimposition application.

Figure 10. Modeling triangular pulses using rectangular pulses example

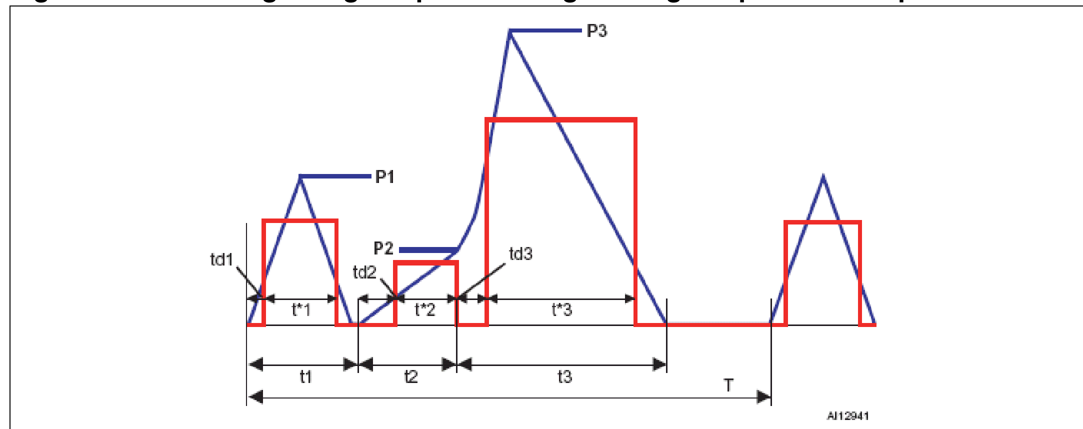
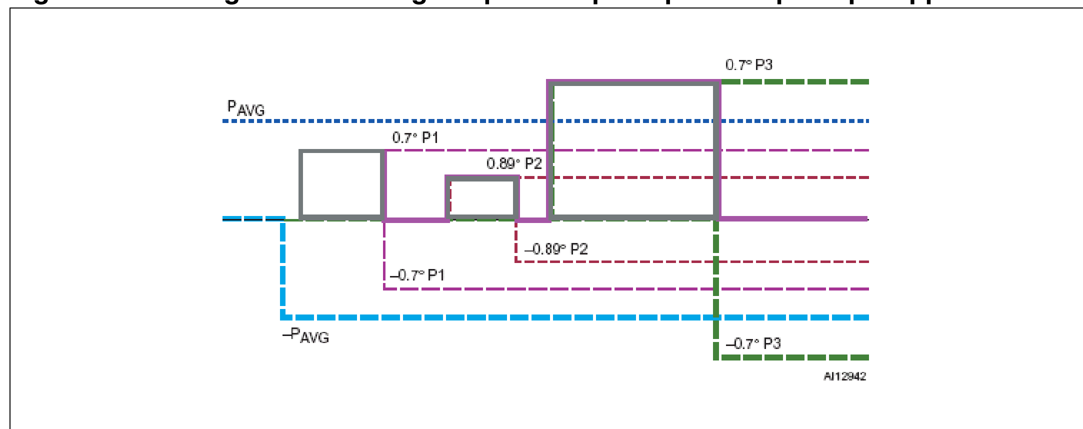


Figure 11. Triangular-to-rectangular pulse superimposition principle application



It is well known that a triangular power pulse can be modeled as a peak power 0.7 amplitude rectangular pulse with a 0.71 actual width. Moreover, a ramp power shape can be modeled as a 0.56 width step pulse with a 0.89 actual amplitude (*Table 2.*). *Figure 12.* shows the triangular power pulse simulated thermal impedance temperature response (blue line), as compared to the rectangular approximation (red line). The average power can be calculated from each peak power result:

Equation 12

$$P_{AVE} = \frac{t_1}{T}0.5 \bullet P_1 + \frac{t_2}{T}0.5 \bullet P_2 + \frac{t_3}{T}0.5 \bullet P_3$$

By superimposition principle and the manipulation of *Equation 11*, the peak temperature results from every single power pulse in *Figure 11.* may be expressed:

- First pulse

Equation 13

$$\Delta T_{JC(max1)} = P_{AVE}(R_{thJC} - Zth_{JC}(t_1^* + t_{D1})) + 0.7 \bullet P_1 \bullet Zth_{JC}(t_1^*)$$

- Second pulse

Equation 14

$$\Delta T_{JC(max1)} = P_{AVE}(R_{thJC} - Zth_{JC}(t_1 + t_2)) + 0.89 \bullet P_2 \bullet Zth_{JC}(t_2^*) +$$
$$+0.7 \bullet P_1 \bullet [Zth_{JC}(t_1 - t_{D1} + t_2) - Zth_{JC}(t_{D1} + t_2)]$$

- Third pulse

Equation 15

$$\Delta T_{JCmax1} = P_{AVE}(R_{thJC} - Zth_{JC}(t_1 + t_2 + t_{D3} + t_3^*)) + 0.7 \bullet P_3 \bullet Zth_{jc}(t_3^*) +$$
$$+0.7 \bullet P_1 \bullet [Zth_{JC}(t_1 - t_{D1} + t_2 + t_3^* + t_{D3}) - Zth_{JC}(t_{D1} + t_2 + t_3^* + t_{D3})] +$$
$$+0.89 \bullet P_2 \bullet Zth_{JC}(t_2^* + t_3^* + t_{D3}) - Zth_{JC}(t_3^* + t_{D3})$$

Figure 12. Thermal response comparison

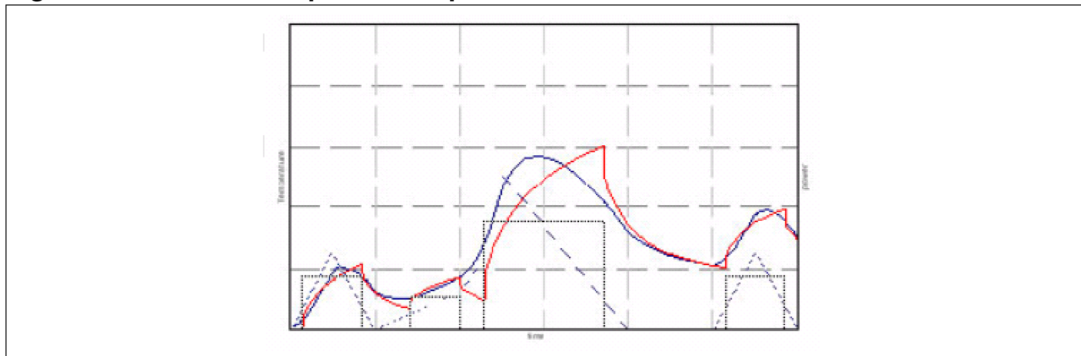


Table 2. Rectangular approximation of special power curves

Curve	P(t) see *Appendix A on page 24*	Energy	t	P'
Ramp	$P\ t/t_P$	$0.5^*\ P_{PEAK}{}^*t_P$	$0.56\ t_P$	$0.89\ P_{Peak}$
Triangular	*Figure 21.*	$0.5^*\ P_{PEAK}{}^*t_P$	$0.71\ t_P$	$0.70\ P_{Peak}$
Parabolic	$P\ t^2/t_P^2$	$0.33^*\ P_{PEAK}{}^*t_P$	$0.39\ t_P$	$0.85\ P_{Peak}$

Using ST's MDMesh STP11NM60FP as an actual example, *Figure 13.* shows the switching waveforms of the device as it is applied as a main switch in an AC adapter. They are also waveforms detailing the avalanche phenomenon.

To confirm that the device is working within the specification we have to check the datasheet ratings (see *Figure 14.* and *Figure 15.*). The data is as follows:

- T= 12µs
- T_{CASE}=70°C
- T_{ON}=40ns;
  $$P_{PEAK(ON)} = 160V \bullet 1.6A = 256W$$
- T_{OFF}=60ns
  $$P_{PEAK(OFF)} = 280V \bullet 2.4A = 672W$$
- t_{COND}=2.4µs
  $$P_{PEAK(COND)} = (4A)^2 \bullet 0.45 \bullet 2.4 = 17.3W$$
- t_{AV}=86ns
  $$P_{PEAK(AV)} = 680V \bullet 3.6A = 2448W$$

For the peak power calculation over the conduction state, it is assumed that the worst case $R_{DS(ON)}$ is:

$$T_J = 150°C$$

and,

$$R_{DS(ON)}(150°C) = R_{DS(ON)}(25°C) \bullet 2.4$$

where,

2.4 is the derating factor found in the STP11NM60FP datasheet, in the plot showing the “normalized $R_{DS(ON)}$ vs. temperature".

Figure 13. Steady-state STP11NM60FP switching

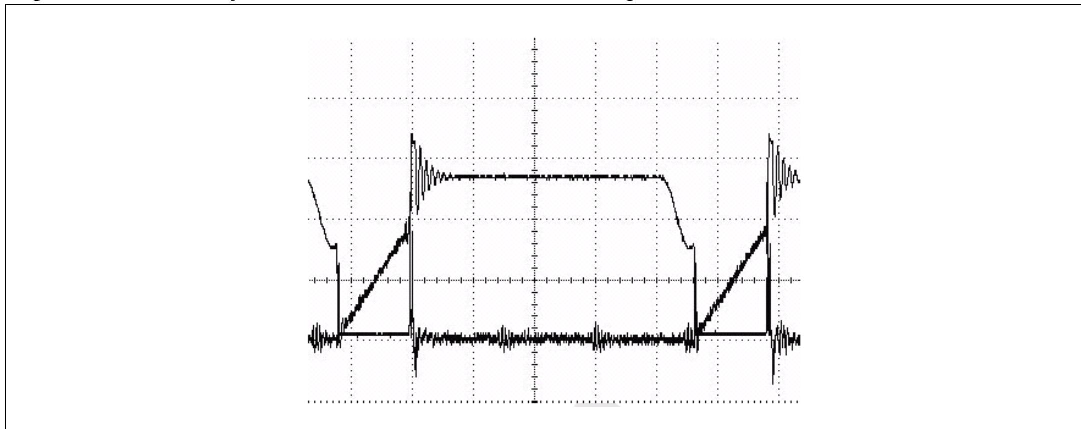


Figure 14. STP11NM60FP switch-OFF details

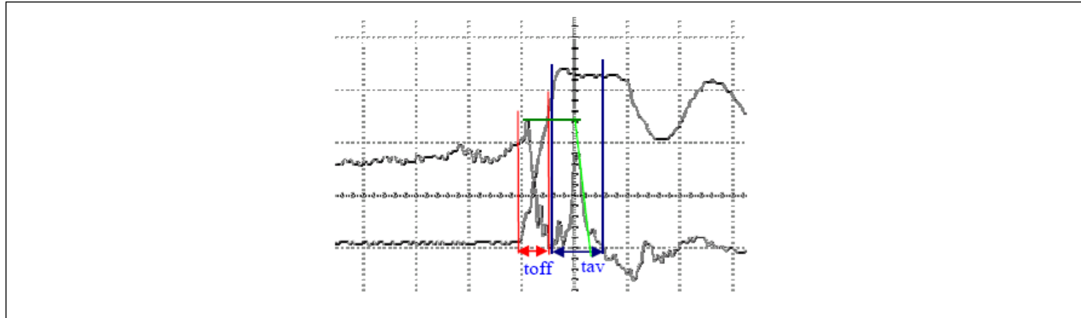
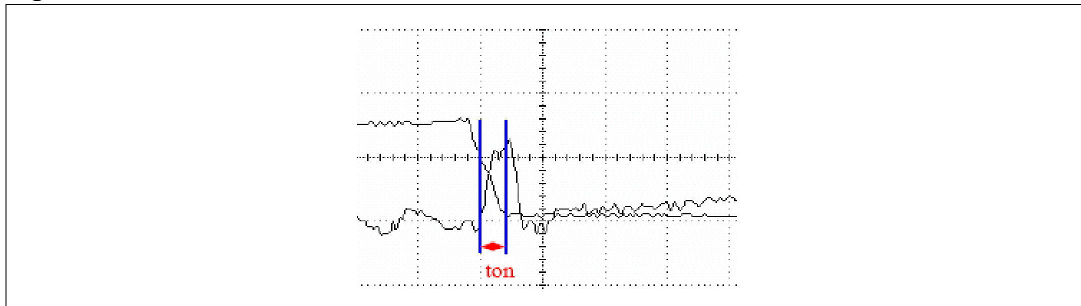


Figure 15. STP11NM60FP switch-ON details



The datasheet indicates that the I_{AR} is 5.5A. Since the peak current during the avalanche is 3.6A (below the datasheet ratings), the I_{AR} constraint is satisfied.

Note: That the peak current before the turn OFF, that in this case is 4.8A, should be taken into account as very worst case for avalanche in case of a higher dV/dt, but also in this last case, the specification is satisfied.

Average power is calculated as follows:

Equation 16

$$P_{AVE} = \frac{t_{AV}}{T}0.5 \bullet P_{PEAK(AV)} + \frac{t_{COND}}{T}0.5 \bullet P_{PEAK(COND)} + \frac{t_{ON}}{T}0.5 \bullet P_{PEAK(ON)} +$$

$$+ \frac{t_{OFF}}{T}0.5 \bullet P_{PEAK(OFF)}$$

Equation 17

$$P_{AVE} = 8.77 + 1.73 + 0.43 + 1.68 = 12.61W$$

Note: For the conduction losses, the worst case of a triangular power shape is considered, even if the right one should not be.

T_{CASE}=70°C, and the R_{thjc} is 3.57 K/W, so the average T_J may be calculated as follows:

Equation 18

$$T_J = P_{AVE}R_{thJC} + T_{CASE} = 45°C + 70°C = 115°C$$

A quick way to calculate the maximum temperature during the avalanche is to add the peak temperature due to the avalanche pulse to the average temperature:

Equation 19

$$Tj = P_{AVE}R_{thJC} + 0.7P_{PEAK(AV)}Zth_{JC}(0.71t_{AV}) + T_{CASE}$$

For the purposes of this example, extrapolating from *Figure 16.*, the Z_{thJC} at 61ns is expressed as:

Equation 20

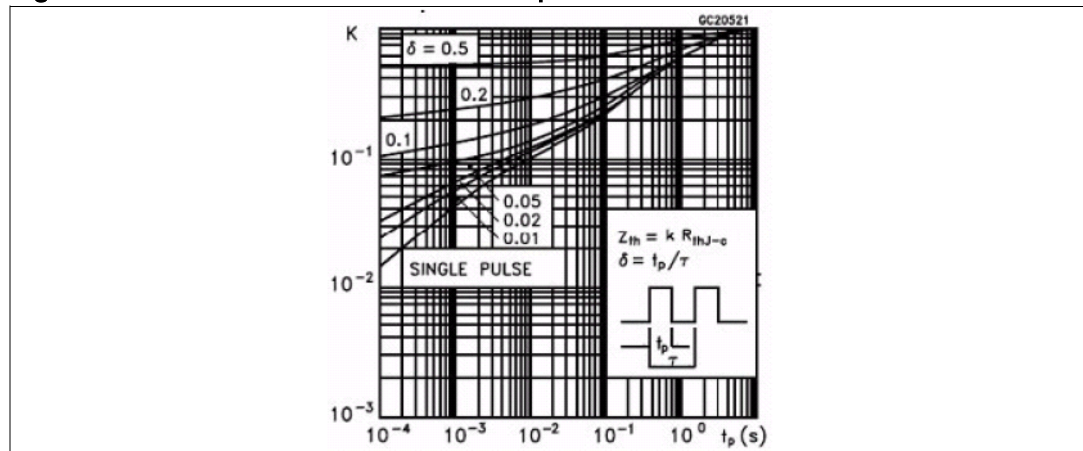
$$Zth_{JC}(61ns) \approx 3.57 \bullet K(61ns) = 0.00125°C/W$$

thus,

Equation 21

$$T_{J(max)} = 45 + 2448 \bullet 0.7 \bullet 0.00125 + 70 \approx 117°C$$

Figure 16. Normalized STP11NM60FP impedante



By using *Equation 15*, a more accurate TJ value at avalanche onset can be calculated. Modeling each power contribution as a rectangular pulse (see *Figure 17.*):

- Pulse 1 (turn ON)

Equation 22

$$t_1^* = 40ns \bullet 0.71 = 28.4ns \qquad td1 = 5.8ns \qquad P_1^* = 0.7 \bullet 256W = 179W$$

- Pulse 2 (conduction)

Equation 23

$$t_2^* = 2.4\mu s \bullet 0.56 = 1.34\mu s \qquad td2 = 1.06\mu s \qquad P_2^* = 0.89 \bullet 17.3W = 15.4W$$

- Pulse 3 (turn OFF)

Equation 24

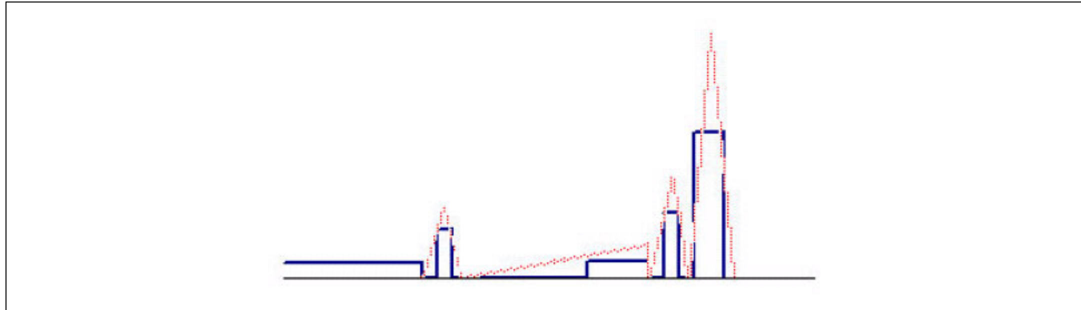
$$t_3^* = 60ns \bullet 0.71 = 43ns \qquad td3 = 58ns \qquad P_3^* = 0.7 \bullet 672W = 470W$$

- Pulse 4 (avalanche)

Equation 25

$$t_4^* = 86ns \bullet 0.71 = 61ns \qquad td4 = 12.5ns \qquad P_4^* = 0.7 \bullet 2448W = 1714W$$

Figure 17. STP11NM60FP rectangular pulse switching approximation



By using the superimposition principle (see *Figure 18.*) the maximum temperature at avalanche onset is expressed as:

Equation 26

$$\Delta T_{jc}max_{av} = P_4^* \bullet Zth_{jc}(t_4^*) + P_{AVE}(Rth_{jc} - Zth_{jc}(t_1 + t_2 + t_3 + t_4^* + t_{D4}))+$$
$$+ P_3^* \bullet [Zth_{jc}(t_3^* + t_{D3} + t_{D4} + t_4^*) - Zth_{jc}(t_{D3} + t_{D4} + t_4^*)] +$$
$$+ P_2^* \bullet [Zth_{jc}(t_2^* + t_3 + t_{D4} + t_4^*) - Zth_{jc}(t_3 + t_{D4} + t_4^*)] +$$
$$P_1^* \bullet [Zth_{jc}(t_1^* + t_{D1} + t_2 + t_3 + t_{D4} + t_4^*) - Zth_{jc}(t_{D1} + t_2 + t_3 + t_{D4} + t_4^*)]$$

then,

Equation 27

$$\Delta T_{jc}max_{av} = P_4^* \bullet Zth_{jc}(61ns) + P_{AVE}(Rth_{jc} - Zth_{jc}(2.57us)) + P_3^* \bullet [Zth_{jc}(125ns) - Zth_{jc}(82ns)]+$$
$$+P_2^* \bullet [Zth_{jc}(1.48us) - Zth_{jc}(133ns)]+$$
$$+P_1^* \bullet [Zth_{jc}(2.57us) - Zth_{jc}(2.54us)] = 47.28° C$$

thus,

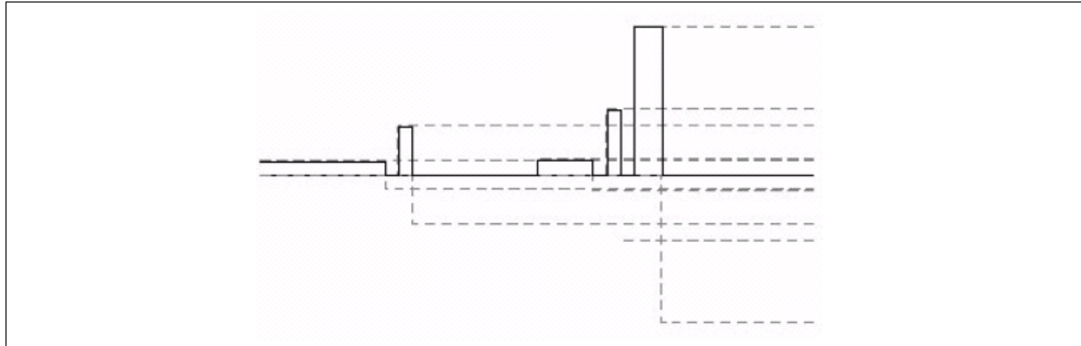
Equation 28

$$T_j = 47.28° C + 70° C \approx 117° C$$

The result, in this case, confirms the application of the simplified equation (see *Equation 18*).

The STP11NM60FP working within the datasheet ratings, I_{AR} and $T_{J(max)}$. Different ambient temperatures or some heat sinking faults or, even some variation of other components in the board can bring the STP11NM60FP to operating points (I_{AR} and $T_{J(max)}$) beyond the absolute maximum ratings and consequently risk the Power MOSFET's failure.

Figure 18. STP11NM60FP rectangular pulse superimposition principle graph



The temperature increase due to a finite number of repetitive avalanche phenomena may be calculated by substituting the R_{th} of *Equation 11* with the Zth calculated at the train pulse duration τ:

Equation 29

$$\Delta T_{JC(max)} = P_0\left(\frac{t_{AV}}{T}Zth_{JC}(\tau) + \left(1 - \frac{t_{AV}}{T}\right)Zth_{JC}(t_{AV})\right)$$

Other methods may be used. For example, using ‘ti’ as the rise and fall times for each rectangular power pulse (see *Figure 13.*), the T_J may be calculated with the superimposition principle for each pulse contribution. This method can be used for trains of few pulses. At the end of the Nth pulse,

Equation 30

$$\Delta T_{JC}(n) = P_0 \sum_{i=1}^{n}(Zth_{JC}((n-i)T + t_{AV}) - Zth_{JC}(n-i)T))$$

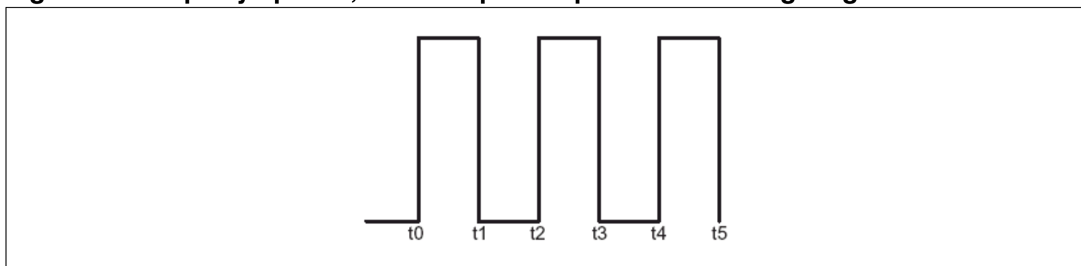
However, for a considerably high number of pulses, this equivalent method should be used to calculate T_J at the Nth avalanche pulse:

Equation 31

$$\Delta T_{JC}(n) = P_0\left(\frac{t_{AV}}{T}Zth((n-2)T + t_{AV}) + \left(1 - \frac{t_{AV}}{T}\right)Zth_{JC}(T + t_{AV}) - Zth_{JC}(T) + Zth_{JC}(t_{AV})\right)$$

This result is to be added (by the superimposition principle) to the temperature increase due to the conduction and switching losses.

Figure 19. Equally spaced, same amplitude pulse train timing diagram



4 Conclusion

Here are a few reminders:

- The required verifications for single and repetitive avalanche is that $T_{J(max)}$ and I_{AR} must always be below the absolute maximum ratings in the DUT datasheet.
- Any high frequency repetitive avalanche may result in device failures, depending on the actual consistency of the heat sink used.
- All manufacturers' production testing is performed only for some milliseconds and that a “pass” is simply defined as a device that has survived without destructive damage.
- Stresses of highly localized peak temperatures and currents at the “microscopic” levels on the MOSFET are impossible to identify. All manufacturing processes are intended to produce uniform and consistent test results (e.g. Rb and Beta). but this does not mean that any single device amongst these, up to several thousands from a single wafer are perfect, even if it survives the short production test.
- The reliance on data sheet avalanche ratings, even if the in-circuit stresses are not carefully calculated or characterized, is motivated by a potentially significant circuit cost saving. The apparent respect of the ratings at certain standard “in lab” conditions cannot be easily and safely generalized to all normal or abnormal events that can happen in the real world application environment. Accepting and tolerating - at least as worst case - the use of the avalanche characteristics of the Power MOSFET in applications where such behavior is not strictly required, must take into account the risk of a reduced guard-band for withstanding events and any other variations that can be correlated with the application failure.

Appendix A Rectangular approximation of special power curves

Figure 20. Rectangular approximation of ramp curve

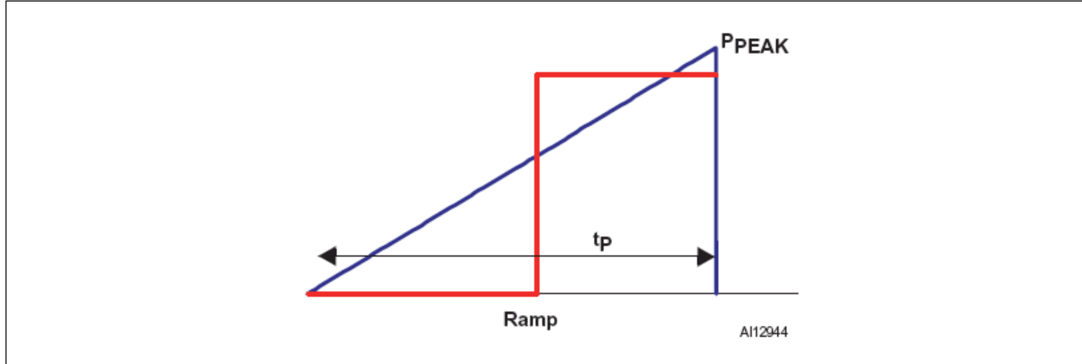


Figure 21. Rectangular approximation of triangular curve

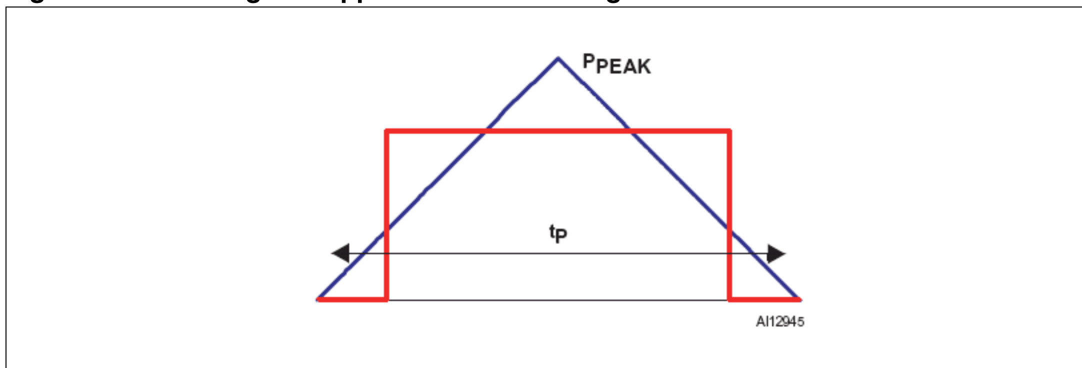
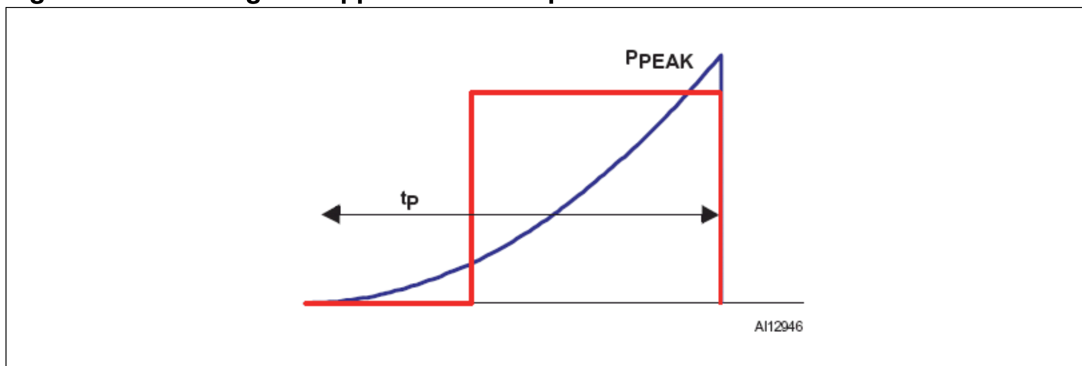


Figure 22. Rectangular approximation of parabolic curve



Appendix B References

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5 Revision history

Table 3. Revision history

Date	Revision	Changes
02-Aug-2006	1	Initial release.

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