Introduction

This document describes a two output buck with the VIPer16LD, a new offline high voltage converter by ST, specifically developed for non-isolated SMPS. In fact the output regulation is easily obtained by a voltage divider connected to the feedback FB pin. Moreover, the VIPer16LD can be externally biased or self-biased. The former reaches very low standby-consumption (< 60 mW at 230 V_{AC}), the latter saves costs and complication of the IC supplying network. The other device’s features are:

- 800 V avalanche rugged power section,
- PWM operation at 60 kHz with frequency jittering for lower EMI
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition

The available protection includes: thermal shutdown with hysteresis, delayed overload protection and open loop failure protection. Protection is in auto-restart mode.

Figure 1. Product evaluation board picture
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1 Adapter features

Electrical specifications of the product evaluation board are listed in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>$V_{IN}$</td>
<td>[90 V&lt;sub&gt;AC&lt;/sub&gt;; 265 V&lt;sub&gt;AC&lt;/sub&gt;]</td>
</tr>
<tr>
<td>Output voltage 1</td>
<td>$V_{OUT1}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Max. output current 1</td>
<td>$I_{OUT1}$</td>
<td>0.1 A</td>
</tr>
<tr>
<td>Output voltage 2</td>
<td>$V_{OUT2}$</td>
<td>5 V (through LDO)</td>
</tr>
<tr>
<td>Max. output current 2</td>
<td>$I_{OUT2}$</td>
<td>0.05 A</td>
</tr>
<tr>
<td>Precision of output regulation</td>
<td>$\Delta V_{OUT_LF}$</td>
<td>±5%</td>
</tr>
<tr>
<td>High frequency output voltage ripple</td>
<td>$\Delta V_{OUT_HF}$</td>
<td>50 mV</td>
</tr>
<tr>
<td>Max. ambient operating temperature</td>
<td>$T_{AMB}$</td>
<td>60 ºC</td>
</tr>
</tbody>
</table>
2 Circuit description

The converter schematic is given in Figure 4. The input section includes a resistor R1 for inrush current limiting, diodes D1 and D2 and a Pi filter (C1, L1, C2) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier and its reference voltage is $V_{FB \_ REF} = 3.3 \text{ V}$. The output voltage $V_{OUT1}$ is regulated by the voltage divider, which is composed of R4 and R5, according to the following formula:

\[
V_{OUT1} = \left(1 + \frac{R5}{R4}\right) \cdot V_{FB \_ REF}
\]

where R5 is split into R5A and R5B to allow a better tuning of the output voltage.

$V_{OUT2}$ comes from $V_{OUT1}$ through a linear voltage regulator, the compensation is performed by the R-C-C network connected between COMP and GND pins.

At power-up, the DRAIN pin supplies the internal HV start-up current generator, which charges the C3 capacitor up to $V_{DDON}$ (13 V). At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C3.

If the jumper J1 is not selected, the VIPer16LD is self-biased: the C3 capacitor voltage, due to the system consumption, falls down and when it reaches $V_{DDCS \_ ON}$ (10.5 V typ.), the internal HV current generator is turned on, recharging C3 up to $V_{DDON}$, after that the HV generator is switched off again. The VIPer16LD is internally supplied without any external network, which minimizes the number of external components. Moreover this function allows the designer to generate output voltages below the voltage lockout (5 V for example) with a simple inductor.

If the jumper J1 is selected, the HV start-up generator is activated at power on only: when $V_{OUT1}$ has reached its steady-state value, IC is biased from the output through the diode D6, allowing the system to reach very low standby-consumption values. This is referred to “external biasing” and can be obtained only if $V_{OUT1}$ is high enough to keep the C3 voltage always above the $V_{DDCS \_ ON}$ threshold.

The shape of the $V_{DD}$ voltage is depicted in Figure 5 and 6 for self-biasing and external biasing respectively.

The R6 resistor, if connected, reduces the default current limitation of the device $I_{DLIM}$ by a certain percentage depending on the resistor value, as reported in the curve $I_{LIM}$ vs. $R_{LIM}$ of the datasheet. This optimizes the design of the magnetic and power elements.
### 3 Bill of material, layout and schematic

Table 2. Bill of material

<table>
<thead>
<tr>
<th>Reference</th>
<th>Part</th>
<th>Description</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cin</td>
<td>100 nF, X2</td>
<td>Series B32922</td>
<td>Epcos</td>
</tr>
<tr>
<td>C1, C2</td>
<td>3.3 µF, 450 V</td>
<td>Electrolytic capacitor</td>
<td>Series M Panasonic</td>
</tr>
<tr>
<td>C3</td>
<td>1 µF, 35 V</td>
<td>Electrolytic capacitor</td>
<td>Series NHG Panasonic</td>
</tr>
<tr>
<td>C4</td>
<td>100 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>Not mounted</td>
<td>Ceramic capacitor</td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>Not mounted</td>
<td>Ceramic capacitor</td>
<td></td>
</tr>
<tr>
<td>C7</td>
<td>1.5 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td></td>
</tr>
<tr>
<td>C8</td>
<td>100 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td></td>
</tr>
<tr>
<td>C9</td>
<td>330 µF, 16 V</td>
<td>Electrolytic capacitor ultra-low ESR</td>
<td>Rubycon</td>
</tr>
<tr>
<td>C10</td>
<td>100 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td>Epcos</td>
</tr>
<tr>
<td>R1</td>
<td>10 Ω</td>
<td>1/2 W resistor</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>Not mounted</td>
<td>1/4 W resistor</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>1 kΩ</td>
<td>1/4 W resistor</td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>12 kΩ</td>
<td>1/4 W resistor</td>
<td></td>
</tr>
<tr>
<td>R5A</td>
<td>33 kΩ</td>
<td>1/4 W resistor</td>
<td></td>
</tr>
<tr>
<td>R5B</td>
<td>0</td>
<td>1/4 W resistor</td>
<td></td>
</tr>
<tr>
<td>R6</td>
<td>Not mounted</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1, D2</td>
<td>GL1M</td>
<td>1000 V/ 1 A diode</td>
<td>Semikron</td>
</tr>
<tr>
<td>D3, D4</td>
<td>STTH1L06</td>
<td>Ultra-fast 600 V diode</td>
<td>ST</td>
</tr>
<tr>
<td>D5</td>
<td>Not mounted</td>
<td>Zener diode</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>LL4148</td>
<td>Diode</td>
<td>Vishay</td>
</tr>
<tr>
<td>L1</td>
<td>1 mH</td>
<td>Axial inductor</td>
<td>Epcos</td>
</tr>
<tr>
<td>L2</td>
<td>1.5 mH</td>
<td>Power inductor</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>IC1</td>
<td>VIPer16LD</td>
<td>Controlled switch</td>
<td>ST</td>
</tr>
<tr>
<td>IC2</td>
<td>L78L05</td>
<td>Voltage regulator</td>
<td>ST</td>
</tr>
</tbody>
</table>
Figure 4. Schematic
Figure 5. $V_{DD}$ waveform, self-biasing (J1 not selected)

Figure 6. $V_{DD}$ waveform, external biasing (J1 selected)
4 Board testing

4.1 Typical waveforms

Source voltage and current waveforms in full load conditions are reported for two nominal input voltages in Figure 7 and 8, and for minimum and maximum input voltage in Figure 9 and 10 respectively.

Figure 7. Source current and voltage at max. load 115 VAC

Figure 8. Source current and voltage at max. load 230 VAC

Figure 9. Source current and voltage at max. load 90 VAC

Figure 10. Source current and voltage at max. load 265 VAC
4.2 Precision of the regulation and output voltage ripple

The output voltage $V_{OUT1}$ of the board has been measured according to different lines and load conditions, both when 5 V output (obtained through linear regulator) is open loaded and full loaded. Results are reported on Table 3. The output voltage is not affected by the line condition and by the IC biasing (external or self-biasing).

<table>
<thead>
<tr>
<th>$V_{IN}$ (VAC)</th>
<th>No load</th>
<th>25% load</th>
<th>50% load</th>
<th>75% load</th>
<th>100% load</th>
</tr>
</thead>
<tbody>
<tr>
<td>115</td>
<td>12.73</td>
<td>12.61</td>
<td>12.14</td>
<td>12.04</td>
<td>12.08</td>
</tr>
<tr>
<td>150</td>
<td>12.76</td>
<td>12.65</td>
<td>12.14</td>
<td>12.04</td>
<td>12.08</td>
</tr>
<tr>
<td>180</td>
<td>12.79</td>
<td>12.68</td>
<td>12.15</td>
<td>12.05</td>
<td>12.08</td>
</tr>
<tr>
<td>230</td>
<td>12.86</td>
<td>12.76</td>
<td>12.16</td>
<td>12.06</td>
<td>12.08</td>
</tr>
<tr>
<td>265</td>
<td>12.87</td>
<td>12.78</td>
<td>12.17</td>
<td>12.08</td>
<td>12.08</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$V_{IN}$ (VAC)</th>
<th>No load</th>
<th>25% load</th>
<th>50% load</th>
<th>75% load</th>
<th>100% load</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>12.01</td>
<td>12.11</td>
<td>12.06</td>
<td>11.98</td>
<td>11.97</td>
</tr>
<tr>
<td>115</td>
<td>12.00</td>
<td>12.09</td>
<td>12.05</td>
<td>11.98</td>
<td>11.97</td>
</tr>
<tr>
<td>150</td>
<td>12.00</td>
<td>12.08</td>
<td>12.04</td>
<td>11.97</td>
<td>11.97</td>
</tr>
<tr>
<td>180</td>
<td>12.00</td>
<td>12.08</td>
<td>12.04</td>
<td>11.97</td>
<td>11.96</td>
</tr>
<tr>
<td>230</td>
<td>12.00</td>
<td>12.08</td>
<td>12.04</td>
<td>11.98</td>
<td>11.96</td>
</tr>
<tr>
<td>265</td>
<td>12.00</td>
<td>12.08</td>
<td>12.04</td>
<td>11.98</td>
<td>11.96</td>
</tr>
</tbody>
</table>
The ripple at the switching frequency, superimposed to the output voltage $V_{OUT1}$, has also been measured and it is shown in figures below at maximum load and nominal input voltages.

Figure 11. Line regulation (external biasing, $I_{out2} = 0$ mA)  
Figure 12. Line regulation (external biasing, $I_{out2} = 50$ mA)  

Figure 13. Load regulation (external biasing, $I_{out2} = 0$ mA)  
Figure 14. Load regulation (external biasing, $I_{out2} = 50$ mA)  

Figure 15. Output voltage ripple at max. load 90 $V_{AC}$  
Figure 16. Output voltage ripple at max. load 265 $V_{AC}$
4.3 Standby performance

As explained in Section 2, two different settings of the IC biasing are possible in the present product evaluation board.

If low standby power loss is a priority, J1 should be selected; it connects diode D6 and disables the HV current generator during steady-state operation. If standby loss is not the main focus, the IC can be self-biased (by deselecting J1), saving the cost of the D6 diode.

The standby performance is shown in the figure below for both cases, with linear regulator disconnected and a 15 V Zener diode across the 12 V output to avoid overvoltage in no load conditions.

The highest line represents the consumption of the converter in those cases where diode D6 is not assembled (IC self-biased), the lower line is the consumption of the converter with diode D6 (IC externally biased).

Figure 17. No load consumption

4.4 Efficiency

The active mode efficiency is defined as the average of efficiency measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages ($V_{IN} = 115 \ V_{AC}$ and $V_{IN} = 230 \ V_{AC}$).

External power supplies (those contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 5 active mode efficiency criterion, which, for a power throughput of 1.5 W, states the active mode efficiency is higher than 67.4% (CoC5 Tier 1, entered into force in January 2014); this limit should increase to 70% starting from January 2016 (CoC5 Tier 2).

DOE (department of energy) recommendation is another standard, whose active mode efficiency requirement for the same power throughput is 69.9%.

The above requirements refer to single output converters and they do not apply to the presented evaluation board, which has two outputs. However, due to the following setting, this board can be evaluated as a single output converter:

- OUT1 loaded with a nominal load: $I_{OUT1} = 130 \ mA$ (corresponding to the nominal power throughput of the board when loaded on both outputs)
- The L7805 connected but no loaded ($I_{OUT2} = 0$)
In this manner, the board is compliant with the above mentioned standards, see *Figure 18*, where the average efficiency measurements at 115 VAC (76.3%) and at 230 VAC (72.3%) are plotted with dotted lines. In the same figure the efficiency at 25%, 50%, 75% and 100% of load for both input voltages is also shown.

![Figure 18. Active mode efficiency and comparison with CoC5 and DOE standards](image)

CoC5 standard has also some requirements on the active mode efficiency when the output load is 10% of the nominal output power. The comparison between the requirement for an external power supply with a power throughput of 1.5 W and the performance of the evaluation board is shown in *Table 5*, where the STEVAL-ISA119V1 is Tier 1 and Tier 2 compliant.

<table>
<thead>
<tr>
<th>CoC5 minimum efficiency requirement in active mode at 10% of full load (P&lt;sub&gt;OUT&lt;/sub&gt; = 1.5 W)</th>
<th>Board performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 1</td>
<td>Tier 2</td>
</tr>
<tr>
<td>57.4%</td>
<td>60%</td>
</tr>
</tbody>
</table>

### 4.5 Light load performance

In the version 5 of the Code of Conduct, the power consumption of the power supply is considered even if it is not loaded. Concerning standards, *Table 6* gives some indications:

<table>
<thead>
<tr>
<th>Nameplate output power (P&lt;sub&gt;no&lt;/sub&gt;)</th>
<th>Maximum power in no load for AC-DC EPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 1</td>
<td>Tier 2</td>
</tr>
<tr>
<td>0.3 W &lt; P&lt;sub&gt;no&lt;/sub&gt; ≤ 49 W</td>
<td>0.15 W</td>
</tr>
<tr>
<td>50 W &lt; P&lt;sub&gt;no&lt;/sub&gt; &lt; 250 W</td>
<td>0.25 W</td>
</tr>
</tbody>
</table>

In no load condition and with different input voltages, the input power of the converter has been measured and results are reported in *Table 7*. 

![Table 5. CoC5 requirement and performance at 10% output load](image)

![Table 6. Energy consumption criteria for no load](image)
The board is compliant with both Tier 1 and Tier 2 requirements. In the same table the consumption of the board in some other light load cases \((P_{\text{OUT}} = 25 \text{ mW}, P_{\text{OUT}} = 50 \text{ mW} \text{ and } P_{\text{OUT}} = 250 \text{ mW})\) is also shown.

The load profile is: load applied on OUT1 only; the L7805 connected but \(I_{\text{OUT2}} = 0\) (see Section 4.4).

### Table 7. Light load consumption

<table>
<thead>
<tr>
<th>(V_{\text{IN}} [\text{VAC}])</th>
<th>(P_{\text{IN}} [\text{mW}])</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>@ (P_{\text{OUT}} = 0)</td>
</tr>
<tr>
<td>115</td>
<td>56</td>
</tr>
<tr>
<td>230</td>
<td>67</td>
</tr>
</tbody>
</table>

According to the equipment supplied, there are several criteria to measure the performance of a converter. For instance, the ErP lot 6 criterion for light load performance, states that the input power in the standby condition should be less than 500 mW. A typical market requirement would be to achieve the same with a 250 mW load. The evaluation board can meet this requirement, as shown in Table 7.

Another criterion for light load evaluation is the measurement of the output power (or the efficiency) when the input power is equal to one watt. This and some other measurements under light load conditions are shown in Table 7 and Table 8.

### Table 8. Light load efficiency

<table>
<thead>
<tr>
<th>(V_{\text{IN}} [\text{VAC}])</th>
<th>Efficiency [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>@ (P_{\text{IN}} = 250 \text{ mW})</td>
</tr>
<tr>
<td>115</td>
<td>64.2</td>
</tr>
<tr>
<td>230</td>
<td>58.3</td>
</tr>
</tbody>
</table>
5 Functional check

5.1 Startup

The start-up phase at maximum load is shown in *Figure 19, 20, 21 and 22* at both nominal input voltages (115 V\textsubscript{AC} and 230 V\textsubscript{AC}).
5.2 Overload protection

In case of overload or short-circuit (see Figure 23), the current across the inductor L2 reaches the $I_{\text{DLIM}}$ value. In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for $t_{\text{OVL}}$ time (50 msec typical, internally set) the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{\text{RESTART}}$ time (1 sec typical). When this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (see Figure 24). This ensures restart attempts of the converter with low repetition rate, so that it can work safely with extremely low power throughput and avoid the IC overheating in case of repeated overload events.

After the short removal, the IC resumes working normally. If the short is removed during $t_{\text{SS}}$ or $t_{\text{RESTART}}$, i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{\text{RESTART}}$, the IC must wait for the $t_{\text{RESTART}}$ period to elapse before switching is resumed (see Figure 26).
5.3 Feedback loop failure protection

This protection is available any time IC is externally biased. As the loop is broken (R4 shorted or R5 open), $V_{OUT1}$ increases and the VIPER16LD runs to its maximum current limitation. If J1 is selected, $V_{DD}$ pin voltage increases as well, because it is linked to $V_{OUT1}$ through diode D6.

If $V_{DD}$ voltage reaches $V_{DDclamp}$ threshold (23.5 V min.) in less than 50 msec, IC is shut down by open loop failure protection (see Figure 27 and 28), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low-side resistor of the output voltage divider, R4. The same behavior can be induced opening the high-side resistor, $R5 = R5A + R5B$.

The protection acts in auto restart mode with $t_{RESTART} = 1$ sec (see Figure 28). As the fault is removed, normal operation is restored after last $t_{RESTART}$ interval has been completed (see Figure 30).
**Figure 27. Feedback loop failure protection: tripping**

Fault is applied here

**Figure 28. Feedback loop failure protection: steady-state**

**Figure 29. Feedback loop failure protection: steady-state (zoom)**

Fault is removed here

**Figure 30. Feedback loop failure protection: converter restart**
6 Thermal measurements

A thermal analysis of the product evaluation board in full load conditions at $T_{\text{AMB}} = 25 \, ^{\circ}\text{C}$ has been performed using an IR camera. Results are shown in the following figures, where the check points A, B, C and D indicate respectively: IC2, VIPer16LD, D4 and room temperature.

Figure 31. Thermal measurement at $V_{\text{IN}} = 90 \, V_{\text{AC}}$, full load  
($I_{\text{OUT1}} = 100 \, mA$, $I_{\text{OUT2}} = 50 \, mA$)

Figure 32. Thermal measurement at $V_{\text{IN}} = 115 \, V_{\text{AC}}$, full load  
($I_{\text{OUT1}} = 100 \, mA$, $I_{\text{OUT2}} = 50 \, mA$)
Figure 33. Thermal measurement at $V_{IN} = 230\ V_{AC}$, full load
($I_{OUT1} = 100\ mA$, $I_{OUT2} = 50\ mA$)

Figure 34. Thermal measurement at $V_{IN} = 265\ V_{AC}$, full load
($I_{OUT1} = 100\ mA$, $I_{OUT2} = 50\ mA$)
7 EMI measurements

A pre-compliance test to EN55022 (Class B) European normative has been performed using an EMC analyzer and an LISN. The average EMC measurements at 115 VAC/full load and 230 VAC/full load have been performed and the results are shown in Figure 35 and 36.

**Figure 35. Average measurement at \( V_{\text{IN}} = 115 \text{ VAC} \), full load**

\( I_{\text{OUT1}} = 100 \text{ mA, } I_{\text{OUT2}} = 50 \text{ mA} \)

**Figure 36. Average measurement at \( V_{\text{IN}} = 230 \text{ VAC} \), full load**

\( I_{\text{OUT1}} = 100 \text{ mA, } I_{\text{OUT2}} = 50 \text{ mA} \)
Appendix A  Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. Digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

*Figure 37* shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

*Figure 37. Connections of the UUT to the wattmeter for power measurements*

An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter’s efficiency, which has been measured in different input/output conditions.

### A.1 Measuring input power

With reference to *Figure 37*, the UUT input current causes a voltage drop across the ammeter’s internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch of *Figure 37* is in position 1 (see also the simplified scheme of *Figure 38*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in light load conditions).
In case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in Figure 37 can be changed to position 2 (see simplified scheme of Figure 39) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

On the other hand, the position of Figure 39 may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is better to use the setting of Figure 38 for light load measurements and Figure 39 for heavy load measurements.
If it is not clear which measurement scheme has the lesser effect on the result, both of them should be tested and then, the lower input power value should be registered.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and measurements can be recorded at the end of the 5-minute’s period. If AC input power is not stable over a 5-minute’s period, the average power or accumulated energy is measured overtime for both AC input and DC output.

Some wattmeter models allow integration of the measured input power in a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is calculated dividing by the integration time itself.
8 References

[1] Code of Conduct on energy efficiency of external power supplies, version 4
[2] VIPER16 datasheet
9_revision_history

Table 9. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tr>
<td>09-Dec-2014</td>
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<td>Initial release.</td>
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