1 Introduction

The electronic ballast market has undergone dramatic changes over the last few years. It has moved from full analog, very differentiated applications made by a collection of drivers and controllers, where use of custom ASICs was widespread, to a couple of standard platforms.

The basic building blocks are still the same. They include a power factor corrector stage and an inverting high voltage stage (Figure 1). On the one hand, analog platforms are targeting the low cost/basic performance applications. Their main drivers and controllers are widely used and well known ICs such as Power Factor Correctors (L6561/2/3) and High Voltage Ballast Controllers (L6569x/ L6571x/ L6574). On the other hand, a new digital platform concept has gained more interest and acceptance. A microcontroller with a simple Half Bridge Driver (L638x) has replaced the ballast controller. The Half Bridge Driver is used mainly for high-end applications, especially where the microcontroller has to deal with communication tasks (e.g. using the Dali protocol).

STMicroelectronics' digital ballast reference design STEVAL-ILB002V1 introduces a safe operating Power Factor Controller (PFC) and Ballast Controller. Even with relatively simple microcontroller firmware routines, the results for power control and ballast protection are in line with advanced analog controlled ballasts, while adding flexibility, for example, the possibility to drive a wide variety of lamps, or to easily introduce different protection schemes.

This application note deals in detail with the first block of the digital ballast, which provides stable DC bus voltage for the halfbridge in all load conditions, as well as controlling the input current shape which fulfills IEC standards (6.: IEC 61000-3-2 "Electromagnetic compatibility").

The final description of the digital ballast - the lamp control block - will be described in detail in a separate application note.
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2 Power Factor Correction (PFC)

Theoretically, any switching topology can be used to achieve a high power factor but, in practice, the boost topology has become the most popular because of the advantages it offers. These include:

- Circuit requires the least external parts, thus it is the cheapest available.
- Boost inductor, located between the bridge and the switch, lowers the input di/dt, thus minimizing noise generated at the input and consequently reducing the EMI filter input requirements.
- Switch is source-grounded and therefore easy to drive.

Three methods of controlling the PFC preregulator are currently widely used. They are:

- The Fixed Frequency Average Current Mode PWM.
- The Transition Mode (TM) PWM (fixed on-time, variable frequency).
- The peak current mode with fixed off-time.

Control of the first method is complicated and requires a sophisticated IC controller (e.g. either ST’s L4981A or ST’s L4981B which offers frequency modulation) and a considerable component count.

Control of the second method is simpler (e.g. ST’s L6561/2/3 family) and requires fewer external parts. It is therefore much less expensive.

With the Fixed Frequency Average Current Mode method, the boost inductor operates in continuous conduction mode, while the TM method causes the inductor to work on the boundary between continuous and discontinuous modes. Thus, for a given throughput power, TM operation involves higher peak currents, suggesting it is more efficient at lower power ranges (typically below 200W). In contrast, the Fixed Frequency Average Current Mode is recommended for higher power levels.

A third method of control, that of applying constant $T_{off}$ control, results in continuous conduction mode. The same simple TM-controllers may be used, as may a small RC network to set the off-time. This method is described in AN1792 (7) It is optimal for an input power of between 200 and 400W.

2.1 Transition Mode operation

As mentioned above, the typical PFC topology used in electronic ballasts is a step-up (boost) regulator (Figure 1) working in transition conduction mode. Figure 2 outlines the Transition Mode principles. When the MOSFET is turned on, the inductor is charged from the input voltage source. When the MOSFET is turned off, the boost inductor discharges its energy into the load until its current falls to zero. When the latter occurs, the boost inductor has no energy and a zero current (ZCD) signal is detected, due to a demagnetization change on the auxiliary winding. This drives the MOSFET on again, whereby another conversion cycle starts. As the drain voltage drops before turn-on, the turn-on switching losses are minimized. Figure 2 indicates the geometric relationship of average and peak currents. Due to the triangular shape of the inductor current, the peak current is twice the average current.
2.2 Digital implementation - Enhanced One Pulse Mode

To provide good switch control, as described in Chapter 2.1 above, a simple 8-bit microcontroller may be used and a special PWM timer mode has been introduced. The timer mode, called “Enhanced One Pulse Mode” of the PWM generator (12-bit autoreload timer) is found inside the ST7FLITE19B microcontroller. It is explained in Figure 3 and in datasheet ST7Lite1xB (4). In principle, when a zero current event occurs the microcontroller will reset the timer and turn-on the PFC MOSFET. If there is no signal from ZCD, the timer will overflow and turn-on the MOSFET anyway (it means a minimum switching frequency is secured). The on-time of the MOSFET is set by a software control routine and is constant during the mains half-cycle (this is detailed below in Chapter 4). The control routine executed by the MCU alters the on-time depending on the input voltage level and the load current.
Figure 3. Principle of the Enhanced One Pulse Mode, inside the ST7Lite1B

- Timer reset caused by ZCD
- Timer reset caused by autoreload value match
- Compare event
- Events ignored because MOSFET is turned on
- No event occurred
3 Power circuits design

3.1 Power components

All components have been calculated following application note AN966 (3). A full description of the design and selection of each component, based on the analog TM PFC controller L6561, is also given in Appendix A. At the moment, input voltage is limited for European mains. Future Software updates will include wide range input capability.

Besides the passive and discrete components of the microcontroller, the most important part is the power management unit, L6382D5, which helps control the power. It provides a stable (±2%) 5V supply for the microcontroller during the whole operation. It also supplies a high voltage start-up. In addition, one of the general purpose gate drivers integrated inside L6382D5 is used to translate TTL PWM signals from the microcontroller to the boost converter gate of the MOSFET.

Figure 4. Input voltage & current with modified EMI filter (compared to STEVAL-ILB002V1) PF = 0.994 THD = 10.3%

Note: Brown = Mains voltage, Blue = Input current.
Reference board design measurements of STEVAL-ILB002V1 (Figure 5) show a THD value of 10.4% and a PF value of 0.991. Between the manufacturing of the STEVAL-ILB002V1 reference design and publication of this application note, design work has continued and some improvements have been made. For example, EMI filter parameters have been changed from C-L-C to C-L filters, which give better results for waveform, power factor, and THD. This optimized version is given in Figure 7 and result in the measured waveforms shown in Figure 4 with THD = 10.3% and PF = 0.994.
3.2 Schematics

Figure 6. Schematics of STEVAL-ILB002V1 reference design
Figure 7. Modified EMI filter (not included in STEVAL-ILB002V1 reference design)
### 3.3 Bill of material (STEVAL-ILB002V1)

#### Table 1. Bill of material - PFC

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4 Signals measurement, processing & control

*Figure 8* shows the general flow diagram of the PFC Software. It is described in a step by step fashion in the following paragraphs.

*Figure 8. General flowchart of PFC software*
4.1 Input voltage

The first signal used by the microcontroller is a voltage connected to the input connector. This voltage is first divided and filtered by the circuitry shown in Figure 9. Then it is measured by an analog to digital converter (ADC) inside the microcontroller. This signal has several uses. The first is to avoid connecting the wrong input voltage at the beginning (i.e. only European mains are allowed) and second to guard input over-voltage during normal operation. The whole operation is stopped if the microcontroller detects any problems. If an application is stopped due to a fail condition, it could be restarted only by re-lamping (insertion of the lamp) or by mains recycling. The third use of the input voltage measurement is to detect this recycling (disconnection and reconnection of the mains).

A fourth use of the input voltage is when it works in conjunction with the main control loop (described in Chapter 4.2) to recognize a zero mains voltage crossing.

Figure 9. Input voltage sensing circuit
Figure 10. Input voltage sensing circuit output

Note: Brown = mains voltage, Green = voltage on ADC pin.
4.2 Output voltage

The DC bus voltage (PFC output voltage) is measured by a high voltage divider with a low-pass filter (Figure 12). It is used by the software as an input for a PID regulator to calculate the MOSFET on-time. Parameters for the regulator are not fixed but change depending on the lamp state. This is because the electronic ballast behaves like a load with strongly changing conditions (preheating / ignition / normal operation). Figure 13 outlines one control cycle, and clearly shows that the regulator changes the MOSFET on-time at the synchronization event with the mains voltage zero crossing.
Figure 12. Output voltage sensing circuit

![Output voltage sensing circuit diagram]

Figure 13. Output voltage control loop flowchart

![Output voltage control loop flowchart diagram]
Figure 14 shows a DC bus voltage waveform during ballast turn-on. The precision of regulation during normal operation (lamp is on) is ±5%. The only moment when this accuracy is breached is at ignition phase, when there is a relative fast load change (lamp voltage and current rise quickly). It is assumed that by improving the regulation parameters, the ballast will also work from wide range mains (without any component change).

Figure 14. Application start-up

Note: Brown = V_{DC BUS}; Yellow = lamp current.

Beside the main control loop, output voltage is also used for protection. The software is continuously supervising the output voltage value and when it reaches the upper or lower threshold an error is detected. Overvoltage above the higher threshold could mean that there is an unexpected fast load reduction. Alternatively, breaking the lower threshold means a fast increase of the load. Both situation are considered dangerous and are recognized as faults.
4.3 Zero Current Detection

Detection of a zero current crossing the PFC inductor is extremely important. As described in Section 2: Power Factor Correction (PFC), a ZCD defines the moment when the switch should be turned on again. A well-known method used in other analog PFC applications has been implemented for the digital ballast. The secondary winding of PFC inductor (1:10 winding ratio) gives a correct signal for the autoreload timer (Chapter 2.2). Typical signals are shown in Figure 16.

Note: Brown = DC bus voltage; Blue = lamp filament current.
Figure 16. Zero current crossing detection

Note: Green = microcontroller's input pin 18, Blue = inductor current.
4.4 MOSFET current measurement

The main reason for measuring a current flowing through the PFC MOSFET is to prevent exceeding the maximum current rating and so saturating the boost inductor which results in damaging components.

The software routines in general are too slow to perform fast reaction. For this reason, only hardware peripherals are used, and the software is excluded from the detection of overcurrent. Two extra features of the ST7LITE19B are important for this protection:

- the analog comparator;
- the break function.

The comparator integrated inside the microcontroller (datasheet ST7Lite1xB, section 11.6) is a general purpose analog comparator with either an external or internal reference. Output can be seen on an external pin (Port PA7 - pin 11), or as it is in this case used only internally as an input for the second peripheral - the Break.

The Break function is an emergency shutdown used to stop all PWM outputs (i.e. MOSFET gate signals). A detailed description of it may be found in the ST7FLITE19B datasheet, section 11.2.3.3.
In order to simulate the PFC MOSFET overcurrent without stressing other components of the digital ballast, an external DC source has to be connected in parallel with the sense resistor R9 (0.5 Ω). Afterwards, the MOSFET’s gate signal is measured, and the protection response time may be obtained, as shown in Figure 19. Such a response time was measured in less than 500ns, which is fast enough to prevent coil saturation and thereby protect the MOSFET from damage.

Figure 18. Maximum MOSFET’s $T_{\text{ON}}$ protection routine
In addition to the aforementioned hardware protections, another safety feature (Maximum $T_{\text{ON}}$ increase protection) is implemented in the software and outlined in Figure 18. During normal operation, the PFC routine counts the number of times the pre-set MOSFET’s on-time maximum ($T_{\text{ONMAX}}$) is reached. If the maximum count ($N_{\text{MAX}}$) is exceeded an error is introduced and the application is stopped. This condition indicates that the boost converter is unable to reach the required output voltage.

**Figure 19. Overcurrent reaction demonstration**

*Note:* Brown = sense resistor voltage, Green = digital signal for driving MOSFET’s gate.
5 Conclusion and outlook

This application note explains the power factor correction (PFC) stage of the new digital ballast reference design. It demonstrates a synergy between the power management unit L6382D5 and the 8-bit microcontroller ST7FLITE19B in a fully digitally controlled application. The reference design STEVAL-ILB002V1 is introduced with all the features and protections required for high performance digital power supplies/ electronic ballasts. Additional flexibility through the use of a digital approach has been highlighted as well.

The document AN1971 (2) could be referred for more information on first implementation of a digital ballast with control based on the ST7Lite09. Other application notes for full digital ballast (reference design STEVAL ILB002V1) are published in two further application notes.
6 References and related materials

6. IEC 61000-3-2 "Electromagnetic compatibility".
Appendix A  Components calculation

This appendix presents guidelines for the calculation of power components. The content is based on the design process defined in AN966 (3).

A.1  Input capacitor

The input high frequency filter capacitor (C<sub>3</sub>) has to attenuate the switching noise due to the high frequency inductor current ripple (twice the average line current, Figure 9). The worst conditions occur on the peak of the minimum rated input voltage. The maximum high frequency voltage ripple is usually imposed between 1% and 10% of the minimum rated input voltage. This is expressed by a coefficient 'r' (typically, r = 0.01 to 0.1):

\[ C_3 = \frac{I_{RMS}}{2\pi \cdot f_{SW} \cdot r \cdot V_{rms (min)}} \]

High values of C<sub>3</sub> alleviate the burden to the EMI filter but cause the power factor and the harmonic contents of the mains current to worsen, especially at high line and light load. On the other hand, low values of C<sub>3</sub> improve power factor and reduce mains current distortion but require heavier EMI filtering and increase power dissipation in the input bridge. It is up to the designer to find the right trade-off in their application.

A.2  Output capacitor

The output bulk capacitor (C<sub>O</sub>) selection depends on:
● the DC output voltage;
● the admitted overvoltage;
● the output power;
● the desired voltage ripple.

A voltage ripple (\(\Delta V_o = 1/2\) ripple peak-to-peak value) of 100 to 120Hz (twice the mains frequency) is a function of the capacitor impedance and the peak capacitor current (\(I_{C(2f)pk} = I_o\)):

\[ \Delta V_O = I_O \cdot \frac{1}{2\pi \cdot 2f \cdot C_O} \sqrt{\frac{1}{(2\pi \cdot 2f \cdot C_O)^2 + ESR^2}} \]

With a low ESR capacitor the capacitive reactance is dominant, therefore:

\[ C_O \geq \frac{I_O}{4\pi \cdot f \cdot \Delta V_O} = \frac{P_O}{4\pi \cdot f \cdot V_O \cdot \Delta V_O} \]
\( \Delta V_o \) is usually selected in the range 1 to 5% of the output voltage. Although ESR usually does not affect the output ripple, it has to be taken into account for power loss calculations. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

\[
I_{Crms} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot I_{rms}^2 \cdot V_{irms}}{9\pi} - I_o^2}
\]

If the application has to guarantee a specified hold-up time, the selection criterion of the capacitance will change: \( C_o \) has to deliver the output power for a certain time (\( t_{Hold} \)) with a specified maximum dropout voltage:

\[
C_o = \frac{2 \cdot P_o \cdot t_{Hold}}{V_{o_{min}}^2 - V_{op_{min}}^2}
\]

where \( V_{o_{min}} \) is the minimum output voltage value (which takes load regulation and output ripple into account) and \( V_{op_{min}} \) is the minimum output operating voltage before the 'power fail' detection from the downstream system supplied by the PFC.

### A.3 Boost inductor

Designing the boost inductor involves several parameters and different approaches can be followed. First, the inductance value must be defined. The inductance (\( L \)) is usually determined so that the minimum switching frequency is greater than the maximum frequency of the internal starter, to ensure a correct TM operation. Assuming unity PF, it is possible to write:

\[
T_{on} = \frac{L \cdot I_{Lpk} \cdot \sin(\theta)}{\sqrt{2} \cdot V_{irms} \cdot \sin(\theta)} = \frac{L \cdot I_{Lpk}}{\sqrt{2} \cdot V_{irms}}
\]

\[
T_{off} = \frac{L \cdot I_{Lpk} \cdot \sin(\theta)}{V_o - \sqrt{2} \cdot V_{irms} \cdot \sin(\theta)}
\]

\( T_{on} \) being the ON-time and \( T_{off} \) the OFF-time of the power MOSFET, \( I_{Lpk} \) the maximum peak inductor current in a line cycle and \( \theta \) the instantaneous line phase (\( \theta \in (0, \pi) \)). Note that the ON-time is constant over a line cycle.

As previously mentioned, \( I_{Lpk} \) is twice the line-frequency peak current, which is related to the input power and the line voltage:

\[
I_{Lpk} = 2 \cdot \sqrt{2} \cdot \frac{P_i}{V_{irms}}
\]
Substituting this relationship in the expressions of $T_{on}$ and $T_{off}$, after some algebra it is possible to find the instantaneous switching frequency along a line cycle:

$$f_{sw}(\theta) = \frac{1}{T_{on} + T_{off}} = \frac{1}{2 \cdot L \cdot P_i} \cdot \frac{V_{rms}^2 \cdot (V_o - \sqrt{2} \cdot \sin(\theta))}{V_o}$$

The switching frequency will be minimum at the top of the sinusoid ($\theta = \pi/2 \Rightarrow \sin(\theta) = 1$), maximum at the zero crossings of the line voltage ($\theta = 0$ or $\pi \Rightarrow \sin(\theta) = 0$) where $T_{off} = 0$.

The absolute minimum frequency $f_{sw(min)}$ can occur at either the maximum or the minimum mains voltage, thus the inductor value is defined by:

$$L = \frac{V_{rms}^2 \cdot (V_o - \sqrt{2} \cdot V_{rms})}{2 \cdot f_{sw(min)} \cdot P_i \cdot V_o}$$

where $V_{rms}$ can be either $V_{rms(min)}$ or $V_{rms(max)}$, whichever gives the lower value for $L$. Once the value of $L$ is defined, the real design of the inductor can start. Standard high frequency ferrite (gapped core-set with bobbin) is the usual choice in PFC applications. Selection of the most suitable one, among the various types offered by manufacturers, will depend on technical and economic considerations.

The next step is to estimate the core size. To calculate an approximate value of the minimum core size, the following practical equation may be used:

$$\text{Volume} \geq 4K \cdot L \cdot I_{rms}^2$$

where Volume is expressed in cm$^3$, $L$ in mH and the specific energy constant $K$ depends on the ratio of the gap length ($l_{gap}$) and the effective magnetic length ($l_e$) of the ferrite core:

$$K \equiv 14 \cdot 10^{-3} \cdot \frac{l_e}{l_{gap}}$$

The ratio $l_e/l_{gap}$ is fixed by the designer.

Next, the winding has to be specified. Quantities to be defined include the turn number and the wire cross-section.

The (maximum) instantaneous energy inside the boost inductor ($1/2 \times L \times I_{Lpk}^2$) can be expressed in terms of energy stored in the magnetic field, given by the maximum energy density times and the effective core volume $V_e$:

$$\frac{1}{2} \cdot L \cdot I_{Lpk}^2 = \frac{1}{2} \cdot \Delta H \cdot \Delta B \cdot V_e = \frac{1}{2} \cdot \Delta H \cdot \Delta B \cdot A_e \cdot I_e$$

where: $A_e$ is the effective area of the core cross-section, $\Delta H$ is the swing of the magnetic field strength and $\Delta B$ is the swing of the magnetic flux density.
An air gap needs to be introduced to prevent the core from saturating because of its high permeability and to allow an adequate $\Delta H$.

Despite the fact that gap length $l_{gap}$ is only a small per cent of $l_e$, the permeability of ferrite is so high (for power ferrites the typical value of $\mu_r$ is 2500) that it is possible to assume, with good approximation ($\Delta H \approx \Delta H_{gap}$), that the whole magnetic field is concentrated in the air gap. For instance, with an $l_{gap}/l_e$ value of 1% (which is the minimum suggested value) the error caused by the above assumption is approximately 4%. The error is smaller if the $l_{gap}/l_e$ ratio is larger. As a result, the fringing flux in the air gap region may be neglected and the energy balance can be re-written as:

$$L \cdot I_{Lpk}^2 \approx \Delta H_{gap} \cdot \Delta B \cdot A_e \cdot l_{gap}$$

The flux density $\Delta B$, is the same throughout the core and the air gap, and is related to the field strength inside the air gap by the well-known relationship:

$$\Delta B = \mu_0 \cdot \Delta H_{gap}$$

Then, taking Ampere's law into account (but applying it only to the air gap region):

$$l_{gap} \cdot \Delta H_{gap} \approx N \cdot I_{Lpk}$$

it is possible to obtain the following equation from the energy balance equation:

$$L = \mu_0 \cdot \frac{N^2 \cdot A_e}{I_{gap}} \Rightarrow N = \sqrt{\frac{L \cdot l_{gap}}{\mu_0 \cdot A_e}}$$

where $N$ is the turn number of the winding.

Because $N$ is defined, it is recommended to check the core saturation. If the core saturation result is too close to the rated limit, it will be necessary to increase the value of $l_{gap}$ and make a new calculation.

The wire gauge selection is based on limiting the copper losses to an acceptable value:

$$P_{CU} = \frac{4}{3} \cdot I_{rms}^2 \cdot R_{CU}$$

Due to the high ripple frequency, the effective wire resistance $R_{CU}$ increases by skin and proximity effects. For this reason litz wire or multi-wire solutions are recommended. Finally, the space occupied by the winding needs to be evaluated. If it does not fit the winding area of the bobbin, a bigger core set needs to be considered and the winding calculation repeated. It is also necessary to add an auxiliary winding to the inductor, in order for the ZCD pin to recognize at what point the current flowing through the inductor has fallen to zero. The winding is a low cost thin wire and the turn number is the only parameter to be defined.
A.4 Power MOSFET

The choice of MOSFET mainly concerns the $R_{DSon}$, which depends on the output power. The breakdown voltage is fixed by sum of the output voltage, the overvoltage and a safety margin.

The MOSFET’s power dissipation depends on conduction and switching losses.

The conduction losses are given by:

$$P_{ON} = I_{Qrms}^2 \cdot R_{DSon}$$

where:

$$I_{Qrms} = 2 \cdot \sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{1}{6} - \frac{4 \sqrt{2}}{9\pi} \cdot \frac{V_{rms}}{V_o}}$$

Switching losses due to current-voltage cross occur only at turn-off because of the TM operation:

$$P_{CROSS} = V_o \cdot I_{rms} \cdot t_{fall} \cdot f_{sw}$$

where $t_{fall}$ is the crossover time at turn-off. At turn-on, loss is due to the discharge of the total drain capacitance inside the MOSFET itself. In general, these losses are given by:

$$P_{CAP} = \left( 3.3 \cdot C_{OSS} \cdot V_{DRAIN}^{1.5} + \frac{1}{2} \cdot C_d \cdot V_{DRAIN}^2 \right) \cdot f_{sw}$$

where $C_{OSS}$ is the internal drain capacitance of the MOSFET (at $V_{DS} = 25V$), $C_d$ is the total external drain parasitic capacitance and $V_{DRAIN}$ is the drain voltage at MOSFET turn-on. In practice, it is possible to give only a rough estimate of the total switching losses because both $f_{sw}$ and $V_{DRAIN}$ change along a given line half-cycle. $V_{DRAIN}$ in particular, is affected not only by the sinusoidal change of the input voltage but also by the drop due to the resonance of the boost inductor with the total drain capacitance. At low mains voltage, this causes $V_{DRAIN}$ to be zero during a significant portion of each line half-cycle. It is possible to show that "Zero-Voltage-Switching" occurs as long as the instantaneous line voltage is less than half the output voltage.
A.5 Boost Diode

The boost freewheeling diode is a fast recovery one. Its respective DC and RMS current values, which are useful for loss computations, are given below:

\[ I_{D0} = I_0 \]

\[ I_{Drms} = 2 \cdot \sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{V_{irms}}{V_o}} \]

The conduction losses can be estimated as follows:

\[ P_{DON} = V_{to} \cdot I_{DO} + R_d \cdot I_{Drms}^2 \]

where \( V_{to} \) (threshold voltage) and \( R_d \) (differential resistance) are parameters of the diode. The breakdown voltage is fixed with the same criterion as the MOSFET.
7 Revision history

Table 4. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
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<tbody>
<tr>
<td>17-Jan-2007</td>
<td>1</td>
<td>Initial release.</td>
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</table>
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