Introduction

The standard application of the HVLED8xxPF (HVLED807PF, HVLED815PF) is a constant current (CC) LED driver. The average output current $I_{OUT}$, as described in the HVLED815PF datasheet (section 4.5 Constant current operation), does not depend on the value or the waveform of the input voltage $V_{IN}$, then can be used in standard or high power factor implementation.

Two methods of implementing the high power factor (HPF) based on the HVLED8xxPF family are current in use: the current sense modulation and ILED modulation. In either case the input voltage after rectification is not smoothed and the waveform on the bulk capacitor is a semi-sinusoidal waveform. The voltage on the bulk capacitor, $V_{RECT}$, contains information about the phase and waveform of $V_{IN}$.

With the first method, the additional circuitry in Figure 1 applies a DC offset and a modulation, both proportional to the $V_{RECT}$, to the CS pin and permits to obtain an HPF. This solution is described in detail in 1. of Section 3.

The second one, shown in Figure 2, applies a modulation of the ILED pin proportional to the $V_{RECT}$ and features HPF in a single range application (refer to the AN4129 for further details). This application note describes how to modify the basic circuit to support wide input range applications.

![Figure 1. CS HPF; additional components](image1)

![Figure 2. ILED HPF; additional component](image2)
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1 ILED pin

The ILED pin voltage ($V_{ILED}$) is the constant current (CC) loop reference. This voltage divided by two is used as the reference for the MOSFET’s peak drain current during the CC regulation. An external capacitor is used for filtering the ILED pin current with an appropriate time constants ($\tau_{ILED} >> 1 / 2 \cdot \pi \cdot f_{IN}$).

In this configuration the peak of the drain current remains constant during the semi-period but the $t_{ON}$ of the primary MOSFET increases when the instantaneous input voltage decreases and with the mains near the zero-crossing the MOSFET remains in the ON state until the mains voltage becomes enough to source the peak drain current.

Then near the zero-crossing the mains current has a peak as in Figure 3 A.

![Figure 3. ILED voltage and input current waveform](image)

1.1 DC analysis

With a DC input voltage ($V_{IN}$) and the device working in the transition mode (TM), the voltage on the ILED, $V_{ILED}$, is:

**Equation 1**

$$V_{ILED} = 2 \cdot V_{LED} \left( 1 + \frac{V_{C}}{\eta \cdot V_{IN}} \right)$$

This voltage changes in function of mains voltage to maintain constant the output current and $V_{ILED}$ reaches the maximum value at the minimum mains voltage.
In case of sinusoidal mains voltage, if the input current is in phase and with the same waveform of the input voltage (i.e.: HPF and THD > 30%), the Equation 1 becomes:

**Equation 2**

\[
V_{\text{ILEDavg}} = 2 \times V_{\text{CLED}} \left(1 + \frac{V_r}{\eta \times V_{\text{INrms}}}\right)
\]

Where \( V_{\text{ILEDavg}} \) is the average voltage on the ILED pin, obtained by integration \( (\tau_{\text{ILED}} >> 1 / 2 \times \pi \times f_{\text{IN}}) \) of the ILED current in an external capacitor.

*Figure 4* shows the calculated and measured values of the voltage \( V_{\text{ILED}} \) vs. \( V_{\text{IN}} \) with \( V_R = 102 \text{ V} \); the measurements are made on the board EVLHVLED815W10F at \( V_{\text{OUT}} \) nominal (22 V, \( V_R = 102 \text{ V} \)). The difference between the curves, when the \( V_{\text{IN}} \) increases, is due to increasing of switching frequency and then greater power transferred in valley skipping (not TM). *Figure 5* shows the calculated and measured values of the voltage \( V_{\text{ILED}} \) vs. \( V_{\text{IN}} \) with \( V_R = 70 \text{ V} \) and \( V_R = 122 \text{ V} \); the measurements are made on the same board EVLHVLED815W10F changing the number of the LED and then \( V_{\text{OUT}} \) and \( V_R \).
1.2 High power factor modulation analysis

A solution to obtain the high power factor and low THD, as shown in Figure 2 on page 1, is the AC coupling of the ILED pin with the rectified voltage. In this way the average of the voltage \( V_{\text{ILEDavg}} \) is generated by the internal loop, which regulates the average output current, while the waveform is modulated through the voltage divider by \( V_{\text{RECT}} \) (see Figure 3 B).

The average output voltage of an ideal single-phase full wave rectifier is:

**Equation 3**

\[
V_{\text{avg}} = \frac{2}{\pi} * V_{\text{peak}}
\]

Then the AC modulation is optimal when:

**Equation 4**

\[
V_{\text{ILEDavg}} = \frac{2}{\pi} * V_{\text{ILEDpeak}}
\]

To ensure accurate regulation, the peak voltage on the ILED pin \( V_{\text{ILEDpeak}} \) must be smaller than its maximum headroom voltage \( V_{\text{ILEDx}} \) (1.5 V). From **Equation 2** and **Equation 4** can be estimated the maximum reflected voltage:

**Equation 5**

\[
V_{\text{Rmax}} = \eta_{\text{VINmin}} * V_{\text{INmin}} * \left( \frac{V_{\text{ILEDx}}}{\pi * V_{\text{CLED}}} - 1 \right)
\]

The effect of a reflected voltage greater of \( V_{\text{Rmax}} \) is the reduction of the output current when \( V_{\text{IN}} \) is lower than:

**Equation 6**

\[
V_{\text{IN}} = \frac{V_{\text{R}}}{\eta_{\text{VINIn}} * \left( \frac{V_{\text{ILEDx}}}{\pi * V_{\text{CLED}}} - 1 \right)}
\]

The equivalent input resistance of the ILED pin \( (R_{\text{inILED}}) \) is 50 KΩ when \( V_{\text{ILEDavg}} = 1 \) V and the voltage divider must drive the ILED pin with equivalent resistance \( R_{\text{AC}} << R_{\text{inILED}} \). The phase rotation, at the input frequency, introduced from the capacitor \( C_{\text{AC}} \) impacts on the power factor, then the value of the capacitor must be:

**Equation 7**

\[
C_{\text{AC}} \geq 10 * \frac{1}{2 * \pi * f_{\text{IN}} * R_{\text{AC}}}
\]
The selected value of $V_R$ and $V_{I\text{Nmin}}$ imposes the maximum value of:

**Equation 8**

$$V_{\text{ILED}_{\text{avg}}} = 2 \cdot V_{\text{CLED}} \left( 1 + \frac{V_R}{\eta \cdot V_{\text{INmin}}} \right)$$

Where $V_{\text{INmin}}$ is the minimum RMS input voltage and $\eta$ is the efficiency at the $V_{\text{IN}}$ used in the equation.

The correct AC modulation is obtained setting the voltage divider ratio ($K_{\text{AC}}$) equal to:

**Equation 9**

$$K_{\text{AC}} = \frac{V_{\text{RECT}}}{V_{\text{ILED}_{\text{pk}}}} = \frac{\sqrt{2} \cdot V_{\text{INmin}} - V_{\text{drop}}}{\frac{\pi}{2} \cdot V_{\text{ILED}_{\text{avg}}}} = \frac{\sqrt{2} \cdot V_{\text{INmin}} - V_{\text{drop}}}{\pi \cdot V_{\text{CLED}} \left( 1 + \frac{V_R}{\eta \cdot V_{\text{INmin}}} \right)}$$

Where $V_{\text{drop}}$ is the input drop voltage between $V_{\text{IN}}$ and $V_{\text{RECT}}$ (input bridge, input filter, fuse, etc.).

Referring Figure 2 on page 1, because $K_{\text{AC}}$ is $>>$ 1, then $R_p3$ can be set equal to $R_{\text{AC}}$:

**Equation 10**

$$R_p1 + R_p2 = R_p3 \cdot (K_{\text{AC}} - 1)$$

### 1.3 High power factor implementation in wide input range application

With the value of the components chosen in the previous paragraph, the AC modulation is optimized at the minimum input voltage. When the voltage increases, the ILED pin average voltage decreases, but the AC modulation increases and forces to zero the primary current for longer time near the zero crossing (see Figure 3 B). The effect is the generation on the input current a zero crossing distortion, that initially, reduces the harmonics (and THD) of the flyback configuration, but when the input voltage reaches a value around $1.25 \cdot V_{\text{INmin}}$, the distortion begins again to increase. If is desired a THD under 20 - 25%, the ratio between the maximum and minimum of $V_{\text{IN}}$ must be lower than 1.5.

In Figure 6 is presented a solution that permit to cover wide-range application with THD under 20 - 25% and high PF. The circuitry uses in the low range (USA and Japan) a different voltage divider ratio ($K_{\text{ACL}}$), than in the high range (European). The transistor $Q_r$ is used to change the voltage divider ratio between the value $K_{\text{ACL}}$ in the US and Japanese and $K_{\text{ACH}}$ in the European range.
In the low range (88 V - 132 V) the transistor Qr is open and the circuit in Figure 6 becomes as that in Figure 7. The value of $K_{ACL}$ is obtained from Equation 9.

Equation 11

$$K_{ACL} = \frac{V_{p}}{\pi V_{LED} (1 + \frac{V_{R}}{V_{IN_{min}}})}$$

The sum $R_{p1} + R_{p2} + R_{ps}$ can be calculated by Equation 10 that becomes:

Equation 12

$$R_{p1} + R_{p2} + R_{ps} = R_{p3} \times (K_{ACL} - 1)$$

Where $R_{p3} = R_{AC}$ and $R_{ph} = R_{p1} + R_{p2}$.

Rph resistor is splitted into $R_{p1}$ and $R_{p2}$ to satisfy the maximum voltage rating of the case, then $R_{p1} = R_{p2}$, and choosing $R_{ps} = R_{p1} / 3$ permits to use a high value of $R_{pe}$.

Equation 13

$$R_{p1} = R_{p2} = \frac{3}{7} \times R_{p3} \times (K_{ACL} - 1); \quad R_{ps} = \frac{1}{7} \times R_{p3} \times (K_{ACL} - 1)$$
In the high range (185 V - 265 V) the transistor Qr is saturated and the circuit in Figure 6 becomes as that in Figure 8. The value of $K_{ACH}$ is from Equation 9:

**Equation 14**

$$K_{ACH} = \frac{\sqrt{2} \cdot V_{IN\text{minH}} - V_{dRP}}{\eta \cdot V_{\text{CLED}} \left(1 + \frac{V_{S}}{V_{IN\text{minH}}}ight)}$$

Where $V_{IN\text{minH}}$ is the high range minimum RMS input voltage and the value used for $\eta$ and $V_{dRP}$ are the values at the $V_{IN\text{minH}}$.

The value of $R_{pc} + R_{pe}$ to obtain the selected value of $K_{ACH}$ the will be:

**Equation 15**

$$R_{pc} + R_{pe} = \frac{(R_{p1} + R_{p2}) \cdot (R_{ps} + R_{p3})}{R_{p3} \cdot (K_{ACH} - 1) - R_{p1} - R_{p2} - R_{ps}}$$

The resistors $R_{r1}$, $R_{r2}$ and $R_{r3}$ implement a voltage divider. In parallel to the $R_{r3}$ is placed a capacitor $C_{r3}$ that filters the voltage ripple. When this voltage is greater than the sum of Dr Zener voltage ($V_{Z_{Dr}}$) and the base - emitter voltage of Qr ($V_{BE_{Qr}}$), the transistor Qr starts to switch on. The emitter resistor reduces the gain of Qr and permits a linear transition between the low and the high range, that allows to work without hysteresis and reduces the THD in the transition range (132 V -175 V).
Equation 16

\[ R_{r1} + R_{r2} = \frac{2 \cdot \sqrt{2} \cdot V_{\text{InthL}} \cdot R_{r3}}{(V_{\text{Z,Dr}} + V_{\text{BE,Qr}})} \]

Where \( V_{\text{InthL}} \) is the lower transition voltage and \( R_{r3} \ll (1 + h_{\text{FE,Qr}}) \cdot R_{\text{pe}} \).

Figure 8. Equivalent pin ILED modulation circuitry in high input voltage range

The higher transition voltage \( (V_{\text{INHL}}) \) is determined by \( R_{\text{pe}} \) but the base of \( Q_r \) is always biased while the collector voltage drops near to zero and modelling is not simple.

Starting from the below estimated values and the recommended value in Section 2.10 on page 16 further fine tuning of the final application can be done assuming that:

- Decreasing/increasing the Dz Zener voltage the lower transition voltage decreases/increases
- Decreasing/increasing the \( R_{r3} \) resistor value the lower and the higher transition voltage increase/decrease
- Decreasing/increasing the \( R_{r1}, R_{r2} \) resistor value the lower and the higher transition voltage decrease/increase
- Decreasing/increasing the \( R_{\text{pe}} \) resistor value the spread between the lower and the higher transition voltage decreases/increases.
Designing a high PF wide range LED driver with the HVLED815PF

2 Main characteristics and circuit description

The main characteristics of the LED driver are listed here:

- Universal input mains range: 88 ÷ 265 VAC
- Output power 10 W continuous operation
- Output current: 460 mA at 22 V continuous operation
- Overall efficiency up to 85%
- Power factor higher than 0.95

2.1 Input specification

The following is a possible design procedure for a high power factor LED driver using the HVLED815PF device. This design is referred to the schematics of Figure 9. First step is to define the design specification.

Minimum mains voltage [VAC rms]:

Equation 17

\[ V_{\text{IN min}} = 88 \text{ V} \]

Maximum mains voltage [VAC rms]:

Equation 18

\[ V_{\text{IN max}} = 265 \text{ V} \]

Range (wide, US or European) = WIDE; in the European range maximum output power is 15 W, in an other case must be limited to 9 - 10 W. If the mains voltage range is a single range, the switch range network can be omitted (R13, D4, D7, Q2, R21, R20, R4). In a wide mains voltage range the network switches smoothly between the US range and European range.

Minimum mains frequency [Hz]:

Equation 19

\[ F_{\text{IN min}} = 47 \text{ Hz} \]

Mean output current [mA]:

Equation 20

\[ I_{\text{OUT}} = 460 \text{ mA} \]

Output current ripple [%]:

Equation 21

\[ \Delta I_{\text{OUT}} = 140 \% \]
Mean output voltage [V]:

**Equation 22**

\[ V_{\text{OUT}} = 21.7 \text{ V} \]

The mean voltage LED string drop is the output voltage.

Overvoltage protection [V]:

**Equation 23**

\[ V_{\text{OVP}} = 29 \text{ V} \]

The output voltage \( V_{\text{OUT}} \) has a ripple at twice the line frequency and whose amplitude is proportional to the output current and reverse proportional to output capacitance. This application has a high ripple voltage (due to the high power factor and small bulk capacitor).

With a mean output voltage of 22 V the peak is at 25 V.

For reliability the output capacitor has a rated voltage of 35 V.

The selected OVP threshold of 29 V is set between these two limits (the peak output voltage and output capacitor rated voltage).

Supply voltage of the device [V]:

**Equation 24**

\[ V_{\text{CC}} = 12 \text{ V} \]

In this design the supply voltage \( V_{\text{CC}} \) is low. That value is selected, because in this design the output voltage is fixed to 22 V. A higher value of \( V_{\text{CC}} \) is recommended (until 18 - 21 V) in case of application with variable output voltage (example: \( I_{\text{out}} = 460 \text{ mA}, V_{\text{out}} = 14 \text{ V} \sim 22 \text{ V} \)).

The efficiency is better if the supply current is sourced from the auxiliary winding rather than from the high voltage startup.
2.2 Operating conditions

The first step is to verify:

Maximum power output [W]:

Equation 25

\[ P_{\text{OUT}} = I_{\text{OUT}} \cdot V_{\text{OUT}} \leq P_{\text{OUT\_MAX}} \]

In the European range (\( V_{\text{IN\_min}} > 175 \text{ V} \)) \( \rightarrow P_{\text{OUT\_max}} < 15 \text{ W} \)
In the US and Japanese range (\( V_{\text{IN\_min}} < 175 \text{ V} \)) \( \rightarrow P_{\text{OUT\_max}} < 10 \text{ W} \).

2.3 Transformer design

The voltage at the ILED pin must be limited at 1.5 V.

Then for the best performance the optimal reflected voltage \( V_{\text{Ropt}} \) must be set for using all the dynamics of the ILED pin at minimum mains.

Equation 26

\[ V_{\text{Ropt}} = \eta_{\text{VIN\_min}} \cdot V_{\text{IN\_min}} \cdot \left( \frac{V_{\text{ILED}}}{\eta \cdot V_{\text{ILED}} + 1} \right) = 98 \text{ V} \]

Where:
\( \eta_{\text{VIN\_min}} = 80\% \rightarrow \text{efficiency at minimum input voltage} \)
\( V_{\text{ILED}} = 1.5 \text{ V} \rightarrow \text{pin ILED maximum voltage} \)

2.4 Drain source breakdown

Reflected voltage can be limited by drain-source breakdown voltage.

Equation 27

\[ V_{\text{Rbrk}} = V_{(BR)\text{DSS}} - \sqrt{2 \cdot V_{\text{IN\_max}} \cdot V_{\text{Spikes}} \cdot V_{\text{tol}}} = 800 - \sqrt{2 \cdot 265 \cdot 150 \cdot 80} = 200 \text{ V} \]

Where \( V_{\text{tol}} \) is a margin for the components tolerance.

The value of \( V_R \) lower than \( V_{\text{Ropt}} \) and \( V_{\text{Rbrk}} \) is used to calculate the primary/secondary turns ratio \( n \):

Equation 28

\[ n = \frac{V_R}{V_{\text{OUT}} + V_{\text{Fsec}}} = \frac{98}{21.7 + 0.4} = 4.42 \]

Where \( V_{\text{Fsec}} \) = secondary diode forward drop voltage.

When \( V_R \) is lower than \( V_{\text{Ropt}} \), the dynamic is not optimized but the HVLED815PF device is working without problem.

Real value used: \( n = 4.52 \rightarrow V_R = 100 \text{ V} \)
2.5 Current sense resistor

Current sense resistor value is determined by the average LED current $I_{\text{OUT}}$.

Equation 29

$$R_s = \frac{n}{2} \cdot \frac{V_{\text{ILED}}}{I_{\text{OUT}}} = \frac{4.52}{2} \cdot \frac{0.2}{0.46} = 0.98\Omega$$

This formula is exact if:

- The peak voltage on the ILED pin is smaller than the maximum headroom voltage for all mains voltage range.
- OVP protection is set 20% over the maximum output peak voltage.
- Perfect transformer coupling.
- The LED driver works in the TM mode for over an half of the semi-period.

For different designs, fine tuning may be needed, but once the final values are selected, repeatability from unit to unit is excellent.

Real value used: $R_s = 1\ \Omega$

2.6 Primary inductance

The primary inductance $L_p$ sets the working frequency.

For the best regulation is better to limit the minimum frequency at maximum mains voltage (265 V) to 90 KHz, in this way when the voltage is around the peak of the semi-period (and the instantaneous power is higher), the LED driver operates in transition mode (TM). In wide range application, at minimum mains voltage (88 V), this frequency drops to the minimum $f_{\min} \approx 40$ KHz.

Equation 30

$$L_p = \frac{\sqrt{2} \cdot V_{\text{lin}}}{f_{\min} \cdot \left(1 + \frac{\sqrt{2} \cdot V_{\text{lin}}}{V_R}\right) \cdot \frac{V_{\text{ILED}}}{2 \cdot R_s}} = \frac{\sqrt{2} \cdot 88}{\left(1 + \frac{\sqrt{2} \cdot 88}{98}\right) \cdot 50 \cdot 10^3 \cdot \frac{1.5}{2 \cdot 1}} = 1.5\ mH$$

The increase $f_{\min}$ reduces the primary inductance and the transformer can be smaller. In this case $K_{R_s}$ can be used to compensate divergence of $I_{\text{OUT}}$ from the case with optimal frequency.

Real value used: $L_p = 1.5\ mH$
2.7 Secondary/auxiliary turn ratio

The operating range of \( V_{CC} \) is between 11.5 V and 23 V. The mid voltage is around 17 V. The drop voltage on the limiting resistor \( R_{lim} \) (R9) and the auxiliary rectifier diode (D2) at the nominal operating point is set to 1 V.

**Equation 31**

\[
V_{drop\ AUX} = V_{Faux} + V_{Rlim} = V_{Faux} + I_{CC} \cdot R_{lim}
\]

Then is defined the secondary/auxiliary turn ratio.

**Equation 32**

\[
\frac{N_S}{N_{AUX}} = \frac{V_{OUT} + V_{Fsec}}{V_{CC} + V_{drop\ AUX}} = \frac{22 + 0.7}{12 + 1}
\]

Two conditions must be checked:

1. In case of an open circuit the output voltage is a bit upper at the threshold \( V_{OUT\ OVP} \) in this situation \( R_{lim} \) must limit the current to 25 mA.

**Equation 33**

\[
R_{lim} = \frac{N_{AUX}}{N_S} \cdot \frac{(V_{OUT\ OVP} + V_{Fsec}) - V_{2min}}{I_{CC\ max}}
\]

\[
R_{lim} = \frac{V_{drop\ AUX} - V_{Faux}}{I_{CC}}
\]

The higher value of \( R_{lim} \) must be used in the design, if greater \( R_{lim} \) is determined for the open circuit conditions, the secondary/auxiliary turn ratio to compensate the drop on \( R_{lim} \) must be recalculated.

2. If requested, wide range output voltage at the constant current \( V_{CC} \) must be increased to 21 V.

To demonstrate the high voltage startup functionality in this design \( V_{CC} \) is lower, then:

Real value used: \( \frac{N_S}{N_{AUX}} = 1.75 \rightarrow V_{CC} = 12 \text{ V} \)

2.8 Feed forward

**Equation 34**

\[
R_{dmg} = \frac{N_{AUX}}{N_f} \cdot \frac{L_p \cdot R_{FF}}{T_D \cdot R_S} = \frac{N_{AUX}}{N_f} \cdot \frac{N_S}{N_p} \cdot \frac{L_p \cdot R_{FF}}{T_D \cdot R_S} = \frac{1}{1.75} \cdot \frac{1}{4.52} \cdot \frac{1.5 \times 10^{-3} \times 45}{100 \times 10^{-9} \times 1} = 86k\Omega
\]

Real value used: \( R_{dmg} = 91 \text{ k}\Omega \)
2.9 OVP protection

In Section 2.1 on page 10 the selected value $V_{OUT\_OVP} = 29$ V, then:

Equation 35

$$R_\text{b} = \frac{R_{\text{Img} \times V_{\text{ref}}}}{V_{\text{OUT\_OVP} \times \frac{N_s}{N_{\text{Aux}}} - V_{\text{ref}}}} = \frac{91 \times 10^3 \times 2.5}{29 \times 1.74 - 2.5} = 16.2k\Omega$$

Real value used: $R_\text{fb} = 16k\Omega$

2.10 AC modulation

To obtain the high power factor and low THD, a signal proportional to rectified mains is applied to the ILED pin.

The other components of the network that switching the range can be calculated, but the non-linear behavior of Qr due the modulation of the Qr collector requires a fine tuning of the network; using the next recommended value for the components, the only value to be calculated is R3 to optimize the modulation at 85 - 90 V.

Equation 36

$$R_p3 = \frac{R_{p1} + R_{p2} + R_{ps}}{(K_{ACL} - 1)} = 6.2k\Omega$$

With:
- $R_{p1} = R_{p2} = 180 k\Omega$
- $R_{ps} = 120 k\Omega$
- $R_{pc} = 51 k\Omega$
- $R_{pe} = 15 k\Omega$
- $R_{r1} = R_{r2} = 120 k\Omega$
- $R_{r3} = 62 k\Omega$
- $C_{r3} = 4.7 \mu F$
- $D_{r} = BZV55-C20$
- $Q_{r} = MMBTA42$
3 Supporting material

Documentation
1. HVLED815PF - “Offline LED driver with primary-sensing and high power factor up to 15 W” datasheet.
2. AN4129 - “STEVAL-ILL044V1: 9 W Triac dimmable, high power factor, isolated LED driver based on the HVLED815PF (for US market)”.

4 Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tbody>
<tr>
<td>08-Sep-2014</td>
<td>1</td>
<td>Initial release.</td>
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