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**Inrush-current limiter circuits (ICL) with Triacs and Thyristors (SCR)  
and controlled bridge design tips**

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**Introduction**

At application start-up, a high current can be sunk from the mains due to transient energy demand to start the system. Such inrush current could come from motor start-up, DC capacitor charge or the low value of resistor impedance at cold temperature.

A high inrush current can cause several issues for the system like component failure (fuse, bridge diode, etc.) but also represents an excessive current stress on the power grid compared to the nominal current sensed in steady state. Indeed, if nothing is implemented to limit the inrush current, the start-up current can easily be 10 to 20 times higher than the steady-state current. The power grid wires and other current protection components have then to be rated to deliver such high current for a short time. Moreover, the sudden current variation will lead to Line voltage dips. These fluctuations will decrease the power delivered to other loads. Then lamps or displays connected on the line could show brightness variation called the flicker phenomenon. To avoid such unwanted phenomenon, the IEC 61000-3-3 Electromagnetic standard defines the maximum voltage fluctuation which can be accepted, and so the maximum repetitive current, according to the application case.

Today, one of the major sources of high inrush current comes from the DC capacitors which are charged by a diode bridge. This document lists the different topologies which can be implemented with SCR (silicon-controlled rectifier) or triacs to implement an inrush-current limitation (ICL) circuit. Tips are given to design such circuits, with a particular focus on the controlled bridge solution.

This document is split into different sections which deal each a specific topic and which can be read separately (references are given to other sections if the reader requires further explanation).

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# 1 ICL circuit topologies

## 1.1 Bypass solutions

Bypass solutions are the solutions traditionally used for inrush-current limiter (“ICL”) circuits. The capacitor inrush-current is limited by a resistor (refer to  $R_{LIM}$  in *Figure 1* to *Figure 4*) which can be either a fixed-value resistor or a temperature-variable resistor. Temperature-variable resistors present usually a negative thermal coefficient (NTC) so that the resistor will have a high impedance value in cold-state, i.e. at start-up, and a low impedance value at steady-state. The low-value resistor is required at steady-state to limit the power losses dissipated by this resistor which becomes redundant as soon as the start-up is finished. But to reduce the NTC resistor losses, a better solution is then to turn on a switch in parallel to bypass its impedance.

Designers were used to use a mechanical relay for the bypass switch (cf. S1 on *Figure 4*). But such technologies have several drawbacks, for example:

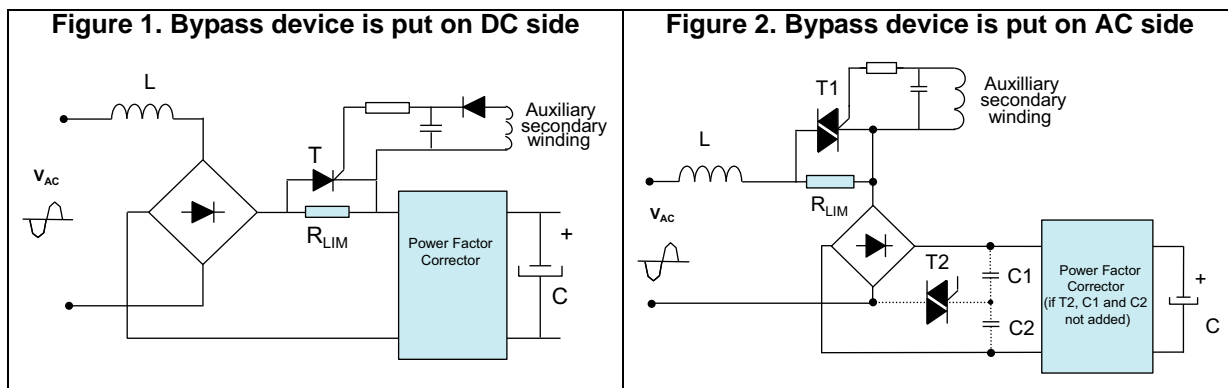
- High current consumption for the coil
- Risk of relay opening in case of machine vibrations
- Acoustic noise due to the mechanical contact
- Risk of explosion in flammable environment (due to switching spark)
- Poor reliability (especially if the relay is switched on or off when a high DC voltage or a high current is present)
- Bulky solution

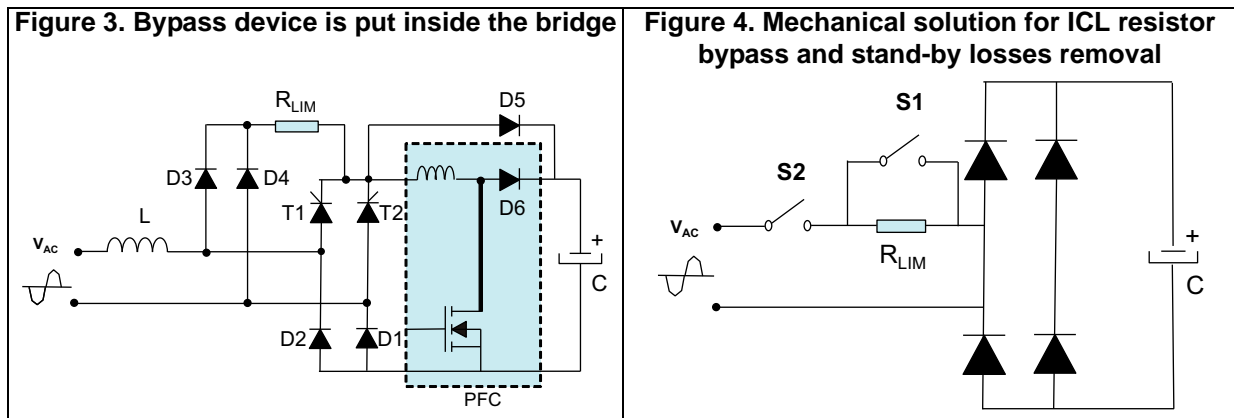
Below figures give the three different solutions which can be used:

*Figure 1*: Bypass device is put on DC side and is implemented with a single SCR

*Figure 2*: Bypass device is put on AC side and is implemented with a single Triac

*Figure 3*: Bypass device is put inside the bridge and is implemented with two SCRs in a mixed bridge.





The schematic in *Figure 2* is the only one able to operate with an AC voltage doubler circuit (implemented with Triac T2, which could be an AVS08 or AVS12 device; and capacitors C1 and C2). The current which charges both C1 and C2 is actually always passing through  $R_{LIM}$  or Triac T1. In case a voltage doubler (with T2, C1 and C2) is implemented in *Figure 1* and *Figure 3* schematics,  $R_{LIM}$  resistor can only limit the current charging C1 capacitor. So the inrush-current could be limited if the application is plugged into the mains during a negative voltage half-cycle.

Please also note that a voltage doubler is useful only if no PFC circuit is used. Indeed a PFC is able to regulate the DC bus to a constant level even if the AC line voltage varies between 90 to 270 V.

The schematic in *Figure 3* could eventually be able to operate with an AC voltage doubler circuit but the two SCRS (T1 and T2) should be placed on the same bridge leg (with for example, T2 cathode connected on T1 anode) instead of a common-cathodes circuit. This means that both SCRs could then not be supplied from the same voltage supply.

Mixed bridge solutions avoid a device to be added in series with the diode bridge. Such a solution is then preferred versus the single-SCR or Triac solutions for applications where a high power efficiency is required.

## 1.2 Soft-start solutions

The drawback of the solutions presented in *Figure 1* to *Figure 4*, is that the  $R_{LIM}$  resistor is always connected to the line (through the diode bridge) even if the application is in stand-by mode.

To reduce the losses which can be dissipated by the application, for example due to the high voltage which is still applied on the DC side through  $R_{LIM}$ , a switch has to be used in series with the line voltage (as shown in *Figure 4* where S2 is open to disconnect the diode bridge in stand-by mode and thus remove the stand-by losses). Such a solution for sure increases the total solution cost.

Another smarter solution involves simply removing  $R_{LIM}$  resistor. *Figure 1* to *Figure 3* schematics could actually work if  $R_{LIM}$  resistor is replaced by an open circuit. The whole solution for ICL function and stand-by losses suppression is then implemented by one or two SCRs, or a single Triac, instead of one ICL resistor and two mechanical relays as shown on *Figure 4*. For the schematic of *Figure 3*, D3 and D4 diodes can also be removed. The solid-state technology could then be cheaper than the mechanical technology solution

and will bring also the advantages already listed in [Section 1.1: Bypass solutions](#) (increased reliability, acoustic noise suppression, etc.).

$R_{LIM}$  removal solution with SCR and Triac ICL function can work if the three following conditions are satisfied:

1. An inductor is present in series with the Line (refer to L in previous schematics).
2. The control circuit is able to implement a progressive soft-start of the device previously used as a bypass switch.
3. An auxiliary supply is present to supply the MCU before the DC output capacitor is charged (refer to C in above schematics) so that the MCU can ensure the inrush-current limiter soft-start.

It should be noted that condition 3 should be fulfilled in most circuits where the consumption in stand-by mode is a concern. Indeed, the stand-by mode means that the most part of the circuit is unpowered but some basic functions have still to be ensured (like MCU reactivation in case a RF or IR signal is received).

These applications use a low-power auxiliary supply to provide the MCU with enough energy during the stand-by mode. A bigger power supply is then activated during normal operation mode.

It should also be noted that condition 1 should be fulfilled almost for free as most applications using a DC bridge feature an SMPS or a motor inverter. And the high-switching frequency of such circuits requires that an EMI filter is added at the application line input. Most EMI filters feature a common mode inductor which presents a spurious differential-mode inductance (like L in the previous schematic) due to the copper turns of the choke.

[Figure 4](#) gives a PSPICE simulation result for the schematic of [Figure 2](#) under these conditions:

- The circuit is operating in doubler mode (T2 Triac is ON)
- The Line voltage is a 120 V RMS 60 Hz voltage
- Output capacitors (C1 and C2) are both 220  $\mu$ F capacitors
- The value of the differential-mode inductor is 100  $\mu$ H
- The PFC circuit is replaced by an open-circuit

T1 Triac control sequence is the following one:

1. Triac is first turned on with a 8.1 ms delay (so approximately 0.23 ms shorter than a line half-cycle)
2. Then, the turn-on delay is decreased by 0.13 ms at each next half-cycle (this is done by applying a gate pulse control with an 8.2 ms period).
3. The gate pulse width is limit to 0.2 ms to avoid that the gate current will be applied at the beginning of the next cycle; especially for the 1rst triggering pulse, as otherwise the Triac will allow a current conduction for the full next half-cycle; the inrush-current would not thus be limited anymore.

Used Triac model is a T1235T device.

Figure 5. DC capacitor soft-start with Triac solution in doubler mode

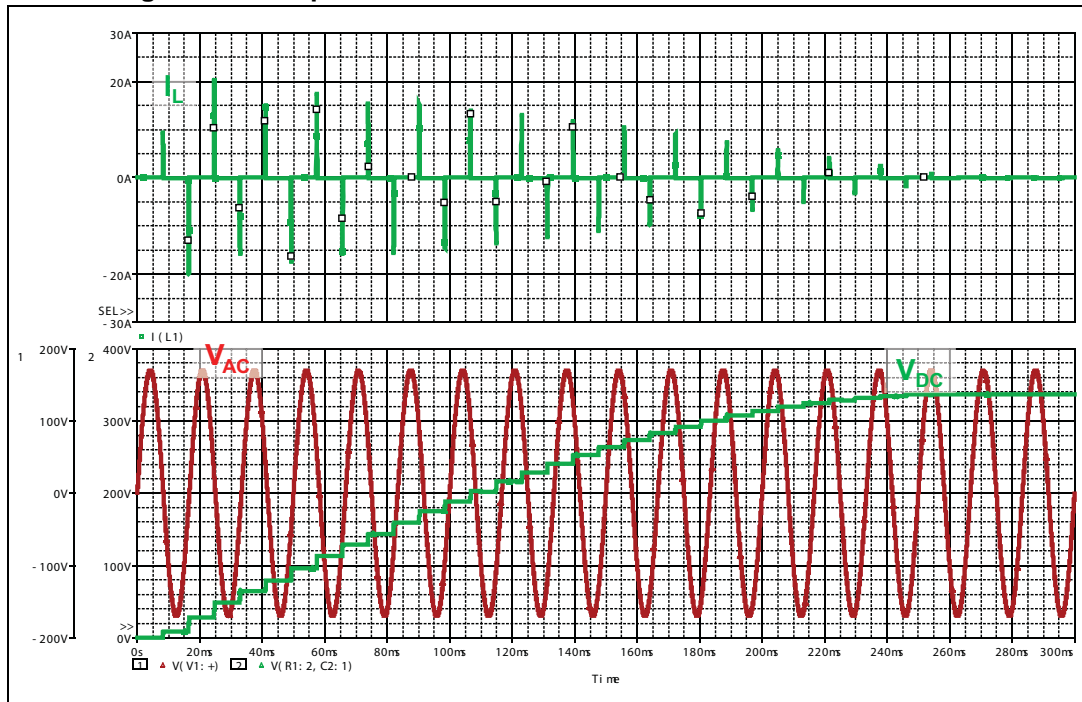


Figure 5 clearly shows that the L inductor current, so the Line input current, is well limited to a peak value lower than 20 A while output voltage ( $V_{DC}$  which is the voltage across both C1 and C2 in series) is charged slowly to two times the peak  $V_{AC}$  voltage in approximately 0.25 s. A 20 A peak current value allows the appliance to fulfill the IEC 61000-3-3 standard while limiting the maximum relative line voltage change below 4%. Indeed to reach a 4% Line voltage variation, a 20 A RMS current has to be drawn from the mains. So with a 20 A peak current, the standard is fulfilled with a good margin.

## 2 Control circuits

### 2.1 Auxiliary winding solutions

[Figure 1](#) and [Figure 2](#) both show that the power device (respectively the SCR and the Triac) are controlled by an auxiliary winding.

This winding is sometimes implemented by adding a secondary winding on the flyback converter of the application supply or on the PFC inductor. This means that a gate current will be applied to the SCR or the Triac as soon as the flyback or the PFC is controlled.

For sure, such a solution cannot work with the soft-start solutions presented in [Section 1.2: Soft-start solutions](#) where the SCR or the Triac has to be controlled before that the output DC capacitor is charged, and so before that the PFC or the flyback is activated.

In case a secondary flyback supply is used to supply the PFC control circuit, then the auxiliary winding could not be added on this secondary supply transformer as a flyback (like the PFC) could not be activated with a predefined delay to achieve the SCR or Triac progressive soft-start (as shown in [Figure 5](#)).

### 2.2 Opto-coupler

#### 2.2.1 Typical schematic

[Figure 6](#) shows a typical example of how an opto-transistor can be connected to drive a SCR used in a mixed bridge. The SCR cathode is then connected to the High-voltage DC bus (HVDC point), while its anode is connected either to the Line or to the Neutral.  $V_{DD2}$  is the supply of the control circuit.  $V_{DD1}$  is the supply used to provide a gate current to the SCR or the Triac (then a negative voltage should be preferred, as explained in AN3168). As  $V_{DD1}$  is referenced to HVDC point,  $V_{DD1}$  and  $V_{DD2}$  supplies have to be insulated from each other.

*Note:* For the typology of [Figure 1](#), the opto-transistor schematic would be the same as for [Figure 6](#) except that SCR anode is connected at the upper output of the diode bridge.

For the schematic of [Figure 3](#), both SCR cathodes are connected to HVDC, the auxiliary supply ( $V_{DD1}$ ), used to provide a gate current to the SCR, needs then to have its reference connected also to HVDC as shown in [Figure 6](#).

Such a topology can easily be implemented using a secondary winding added on a flyback transformer as shown in [Figure 7](#). It could be noted that this secondary winding could be the winding traditionally used to supply the converter IC, as such a winding is no more required if the IC features a current source to ensure its start-up. Then the second supply ( $V_{DD2}$ ), implemented with the secondary transformer winding, is referenced to DC bus ground (refer to GND2 on [Figure 7](#)) and then can supply the SMPS IC control circuit and MCU.

Figure 6. SCR triggering circuit with an opto-transistor

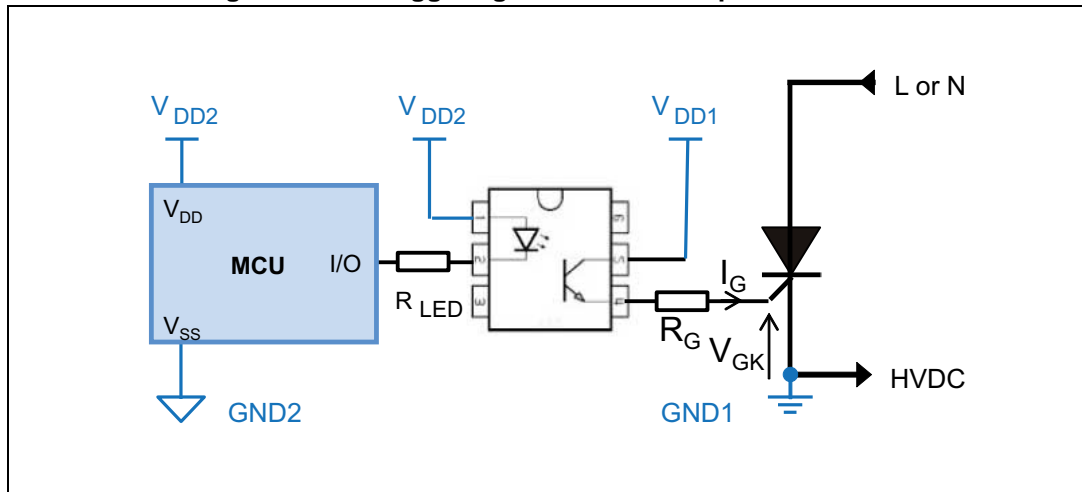
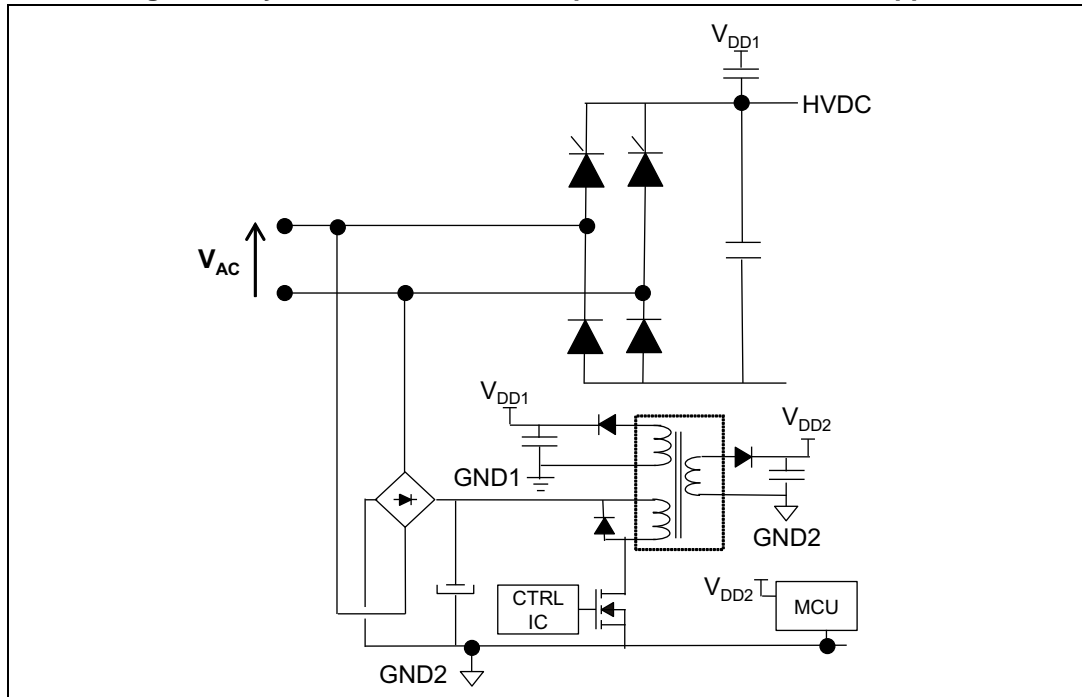


Figure 7. Flyback SMPS solution to provide MCU and SCR supplies



### 2.2.2 Gate resistor selection

The gate resistor  $R_G$  has to be selected to apply a current higher than the SCR  $I_{GT}$ . This resistor has then to satisfy the equation below, where  $V_{CE(sat)}$  is the opto-transistor collector-emitter saturation voltage and  $V_{GK}$  the gate-to-cathode SCR voltage (cf. [Figure 6](#)).

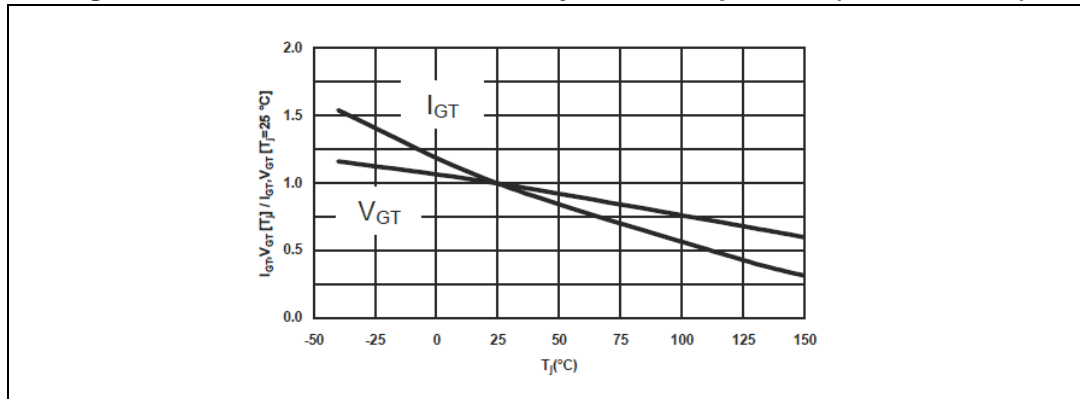
Equation 1

$$R_G < \frac{V_{DD1} - V_{CE(sat)} - V_{GK}}{I_{GT}(T_J)}$$



In the above equation, we note that the SCR  $I_{GT}$  is varying with the junction temperature, that is why it is indicated as " $I_{GT}(T_j)$ ". The gate current of any Triac or SCR indeed increases when the device junction temperature decreases (as show in [Figure 8](#) for example for the TN5050H SCR). The highest gate current to apply occurs when the device has to be started at the minimum ambient temperature. Then, once the device is on, its junction temperature is always above the ambient temperature due to its own power losses.

**Figure 8. Gate current variation versus junction temperature (TN5050H SCR)**



In order to ensure that the SCR will be well triggered whatever the conditions, the best is to take into account the worst case for each parameter. This means that we assume that:

- $V_{DD1}$  is at its lowest level (we assume 10% below its nominal value of 5 V here)
- $V_{CE(sat)}$  equals the maximum specified value (which is usually 1 V for a photo-Darlington, or 0.4 V for a photo-transistor).
- $V_{GK}$  equals the maximum  $V_{GT}$  specified value (for example 1 V for a TN5050H).
- $T_j$  equals to the minimum ambient temperature of the application (usually 0 °C to -10 °C).

The selected resistor is a 5% accuracy resistor; so the worst case occurs when  $R_G$  is 5% higher than its standard value.

For our calculation, we consider a TN5050H device which is a 1200 V 50 A SCR with a 50 mA gate current. This device is also available in automotive grade (TN5050H-12WY) and is allowed to work with 150 °C junction temperature.

In order to allow a control by a single MCU I/O pin, a photo-transistor is enough (there is no need of a photo-Darlington with a better gain between the LED current and detector current).

If the minimum ambient temperature is -10°C, according to the TN5050H device datasheet curve, the maximum  $I_{GT}$  at -10°C is approximately 30% higher than the value specified for 25 °C. This means a gate current higher than 65 mA ( $1.3 \times 50 = 65$ ) has to be applied.

The gate resistor to select has to lower than:

#### Equation 2

$$R_{OUT} < \frac{V_{DD1min} - V_{CE(sat)max} - V_{GKmax}}{I_{GT(-10^\circ C)} \cdot 1.05} = \frac{4.5 - 0.4 - 1}{65 \cdot 10^{-3} \cdot 1.05} = 45 \Omega$$

The closest standard is then 39 Ohm for a 5% accuracy series.

### 2.2.3 LED current setting

The minimum current to apply to the LED is for sure linked to the gate current to apply and also to the current transfer ratio (CTR) of the photo-coupler.

For most photo-couplers, the CTR can be considered as constant from 25 °C to -10 °C. So the datasheet minimum specified CTR can be considered for our calculation.

As previously stated, we assume a photo-transistor (not a photo-Darlington). Then we can consider a 50% minimum CTR.

The LED resistor (refer to  $R_{LED}$  on [Figure 6](#)) has then to satisfy the equation below, where  $V_F$  is the opto-transistor emitter LED forward voltage and  $V_{OL}$  the MCU I/O pin low-level output voltage.

#### Equation 3

$$R_{LED} < \frac{V_{DD2} - V_F - V_{OL}}{I_{GT}(T_j)/CTR}$$

To ensure we always apply a current at least higher than the required  $I_{GT}$  at the photo-coupler output, we also take into account here the worst case:

$V_{DD2}$  is at its lowest level (we assume 10% below its nominal value of 5 V)

$V_F$  equals to the maximum specified value of the LED (which is usually around 1.5 V).

Maximum low output level for the MCU pin which sinks the LED current (we assume 0.8 V for the LED current level sunk by this I/O)

$T_j$  equals the minimum ambient temperature of the application (-10°C as considered previously).

The selected resistor is a 5% accuracy resistor; so the worst case occurs when  $R_G$  is 5% higher than its standard value.

This gives:

#### Equation 4

$$R_{LED} < \frac{V_{DD2min} - V_{Fmax} - V_{OLmax}}{I_{GT}(-10^\circ C)/CTR_{min} \cdot 1.05} = \frac{4.5 - 1.5 - 0.8}{65 \cdot 10^{-3} / 50 \cdot 1.05} = 1612 \Omega$$

The closest standard is then 1500 Ohm for a 5% accuracy series. The nominal current applied to the LED (for the nominal  $V_{DD2}$ ,  $V_{OL}$ ,  $V_F$  and  $R_G$  values) is then in the range of 2 mA. This is well below the maximum advised current for the LED which is usually in the range of 5-10 mA. So the photo-coupler reliability will be better ensured and the CTR ratio should not decrease too much during the application life-time.

## 2.3 Pulse transformer

A pulse transformer is a very easy way to implement an insulated control circuit for power devices like bipolar transistors, SCR or Triacs. Such transformers are magnetic voltage transformers. The ratio between primary and secondary voltages ( $U_1$  and  $U_2$ ) is given by the equation below where  $N_1$  and  $N_2$  are respectively the turns number of the primary and

secondary windings. This ratio “n” is often called the “turns ratio” in pulse transformers datasheet.

#### Equation 5

$$n = \frac{N2}{N1} = \frac{U2}{U1}$$

The number of windings of pulse transformers is also often referred to as “1:1” or “2:1”. This respectively means that for the 1<sup>st</sup> transformer, the secondary voltage equals the primary one, while for the 2<sup>nd</sup> case, the secondary voltage is half the primary one.

One particular point to take into account when designing a pulse transformer is the maximum “Voltage x time” product. The “V x μs” product is usually given for the maximum voltage pulse duration which can be supplied by the secondary winding (but not the product value applied to the primary winding). Indeed, the voltage applied to the coil integrated overtime gives an indication of the magnetic core saturation. We call E x T this voltage-time product as if a square voltage pulse is applied. The integral of the secondary voltage will equal the peak output voltage multiplied by the pulse width. We can then estimate the maximum length of voltage pulse applied to the transformer primary with equation below, where  $U1_{Peak}$  is the peak level of the applied square-pulse ( $U1_{Peak}$  would be close to the MCU VDD voltage if [Figure 9](#) schematic is used).

#### Equation 6

$$tp_{max} = \frac{E \times T}{n \cdot U1_{Peak}}$$

If the applied pulse lasts longer than  $tp_{max}$  then the secondary voltage collapses to zero and the primary winding current increases fast due to the primary inductor saturation.

To avoid such core saturation, the voltage applied at the primary should not have any DC content. Even if a square pulse shorter than  $tp_{max}$  is applied, a second pulse cannot be applied after. This applies even if the 2<sup>nd</sup> pulse is applied several hours later as the magnetic core flux remains in the last position inside the magnetic core hysteresis cycle.

To be sure that the primary voltage will not have any DC voltage component, a Zener diode (referred to as Dz in [Figure 9](#)) has to be used. This Zener diode allows a negative voltage to be applied to the primary winding for the time required to decrease the primary winding current back to zero. D1 diode is used to avoid the VDD supply to be short-circuited when the bipolar transistor (Tb) is turned on.

It should be noted that the schematic of [Figure 8](#), which drives simultaneously both SCRs of the mixed bridge, can only be used for short pulse control. Actually this will avoid the reversed SCR leakage current to increase as explained in [Section 3.1](#). In case long-pulse or DC gate control has to be implemented, the schematic of [Figure 7](#) has to be duplicated for each SCR, with a MCU I/O pin dedicated to each SCR (T1 controlled during positive half-cycle and T2 controlled during negative half-cycle).

The SCR gate resistor has to be selected with the same approach as seen in [Section 2.2.2](#). The equation is then:

Equation 7

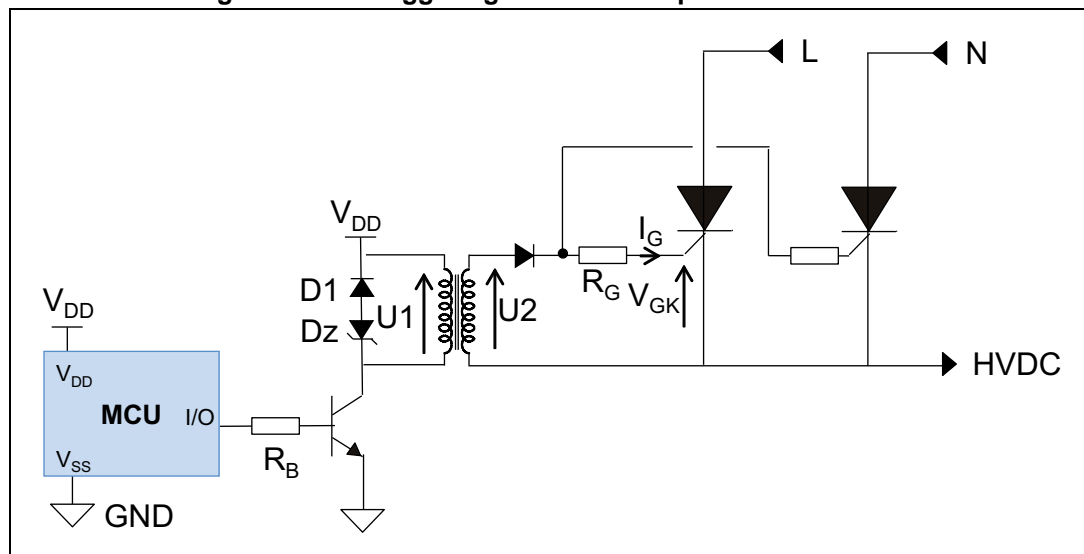
$$R_G < \frac{U_2 - V_F - V_{GK}}{I_{GT}(T_j)}$$

where  $V_F$  is D2 diode forward voltage drop.

It should be noted that the secondary winding current, due to the gate current, has theoretically no effect on the magnetic core saturation. The secondary winding is indeed supplied in order to limit the magnetic flux variation given by Lenz's law. But in practice, as the magnetic coupling is not perfect between secondary and primary, the secondary current will cause an early saturation and the voltage pulse width would then be reduced. If the pulse transformer output current capability is not clearly given in the transformer datasheet, practical experimentation has to be performed to confirm if the chosen pulse transformer fits the application.

As already said, in case a DC or PWM signal (with a high duty cycle which could generate too high OFF state losses of each SCR) is applied to each SCR gate, it is better to use one pulse transformer for each SCR. A diode bridge can then also be used to enlarge the gate current pulse width and provide a gate current even while a negative voltage is applied to the primary by the Zener diode. A capacitor can also be used to smooth the voltage applied to the each SCR gate.

Figure 9. SCR triggering circuit with a pulse transformer

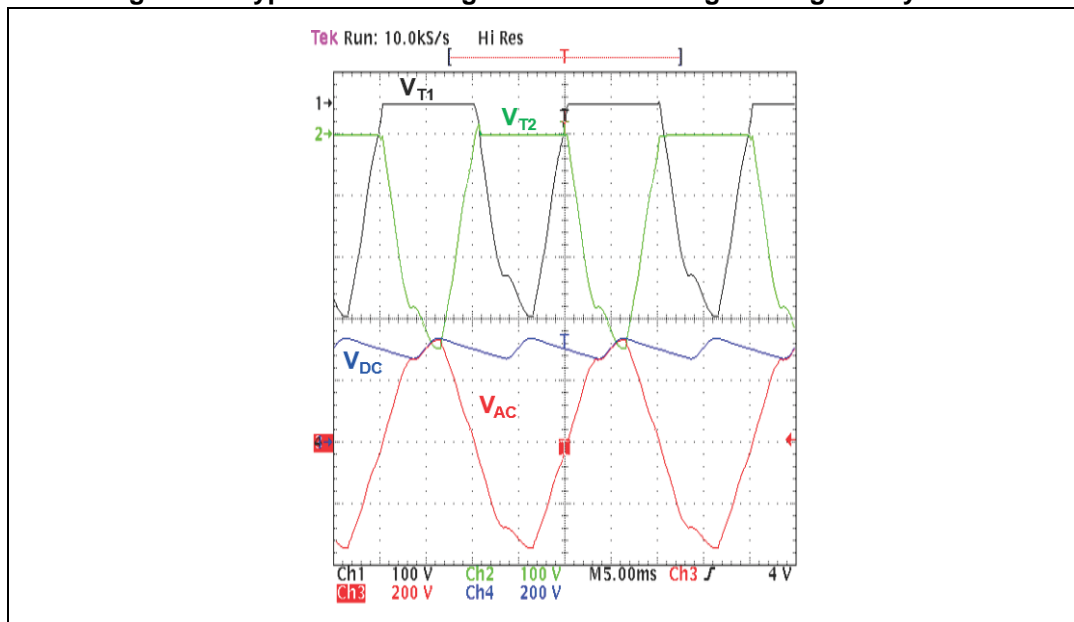


### 3 Mixed-bridge design tips

#### 3.1 Impact of gate current on leakage current

*Figure 10* gives the typical voltage across T1 and T2 SCRs used in a mixed-bridge (cf. *Figure 3*) without any PFC circuit. During this test, T1 and T2 are both triggered by a square gate current while  $V_{AC}$  is respectively positive and negative (i.e. the gate current pulse is 10 ms long for a 50 Hz line frequency).  $V_{T1}$  and  $V_{T2}$  voltages are then equal to zero as these SCR are ON, for the half-cycle where they are triggered, even if they conduct current only when the  $V_{AC}$  voltage goes higher than the output DC voltage, somewhere close to the peak line voltage (as here no PFC is used).

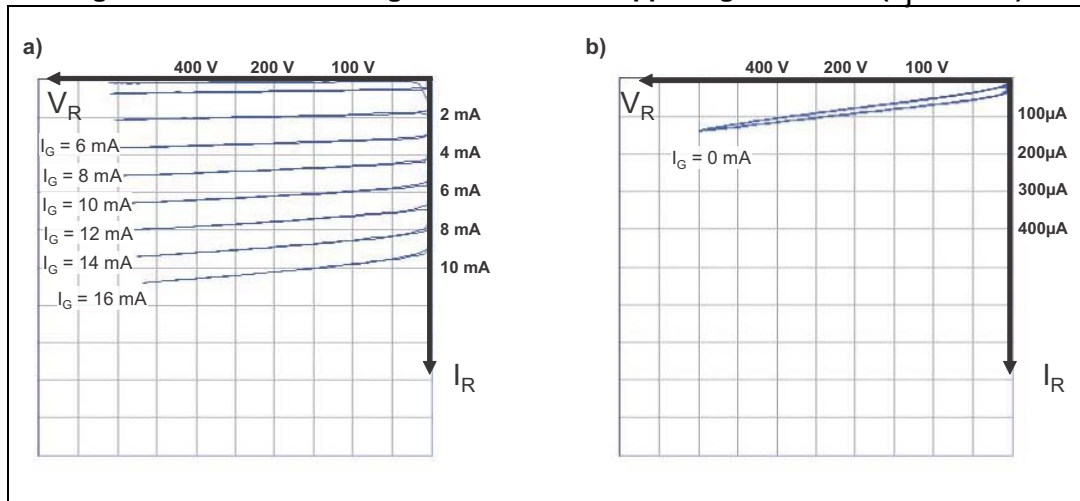
**Figure 10. Typical SCR voltages in a mixed-bridge during steady-state**



*Figure 10* thus clearly shows that when one SCR is triggered (or conducting), the other one is reverse biased.

This is an important point to note. Indeed, the leakage current of a SCR can increase when a gate current is applied. *Figure 11* for example gives a typical leakage current measurement when a reverse voltage is applied to a TYN1012 (1000 V 12 A SCR, with a 15 mA  $I_{GT}$ ) at a 125 °C junction temperature. *Figure 11.a* gives the measurement results when a gate current, from 0 to 16 mA, is applied. In this case, the leakage current at 400 V is above 10 mA for a 16 mA applied gate current. This is more than 100 times higher than the leakage current which is measured without any gate current (100  $\mu$ A typically, for a 2 mA max specified  $I_{DRM}/I_{RRM}$  value in our datasheet). This leakage current increase is due to the internal bipolar transistors of the SCR; the leakage current is indeed applied to a bipolar transistor base. The leakage current is then amplified due to the transistor gain.

Figure 11. TYN1012 leakage current versus applied gate current ( $T_j = 125^\circ\text{C}$ )



This high leakage current can cause a non-negligible power loss increase. The equation below gives the average losses per SCR assuming that the leakage current ( $I_R$ ) is constant whatever is the voltage. This equation takes then into account this DC leakage current multiplied by the line voltage average value for one half-cycle (as no voltage is applied to the SCR for the positive half-cycle if it is triggered).

**Equation 8**

$$P_{OFF} = \frac{\sqrt{2} \cdot V_{RMS} \cdot I_{R(AV)}}{\pi}$$

Assuming a 10 mA DC leakage current, for a 230 V application, gives a 1 W extra loss per SCR! This could significantly impact the application efficiency.

There are two different solutions to avoid such extra loss:

1. The first one involves applying a gate current only to the SCR which has to conduct. This means that one driver is dedicated to a single SCR (so 2 photo-couplers or pulse transformers should then be required to control the whole bridge).
2. The second one involves applying just a short gate current pulse. Then a single driver can be used to drive both SCRs at the same time. Indeed a SCR remains ON as soon as its anode current has become higher than the latching current. If the gate pulse lasts less than 0.1 ms; then the losses calculated previously are 100 times lower for a 50 Hz application (as the pulse duty cycle for a 10 ms period will be 1%).

The second solution is easy to implement especially for applications using a PFC. Indeed for such applications, the time when the SCR has to be switched on is perfectly known, as it is the time where the PFC MOS is turned on by the MCU. So the SCR triggering signal could be synchronized with the 1st MOS turn-on. A single SCR gate pulse is indeed enough for applications where the PFC senses a continuous current. For discontinuous operation mode, the losses due to the leakage current will depend on the SCR gate control duty cycle. Then a solution with separate drivers could be preferred.

It should be noted that such a phenomenon of leakage current with an applied gate current is less an issue for sensitive SCRs (with  $I_{GT}$  lower than 100 µA). In this case applying a 100 µA gate current has almost no impact on the leakage current. But sensitive SCRs cannot be proposed for mixed bridge applications where we need devices able to withstand a high

dV/dt rate and thus avoid the SCR to turn-on during a full half-cycle once the application is hot-plugged to the line. For example the TN5050H is able to withstand at least a minimum rate of 1000 V/μs at a 150 °C junction temperature. Its (dV/dt) capability is typically more than 5 times higher for a 25 °C ambient temperature.

### 3.2 On-state power losses

The ON state voltage, versus its Anode current, of a SCR or Triac can be approximated by below linear law:

#### Equation 9

$$V_T(I_T) = V_{t0} + R_d \cdot i_T$$

where  $V_{t0}$  and  $R_d$  are 2 parameters given in ST Triac and SCR datasheet.

Then the average losses dissipated by the SCR, is given by this equation (refer to AN533 for further information):

#### Equation 10

$$P_{ON} = V_{t0} \cdot I_{AV} + R_d \cdot I_{RMS}^2$$

If a PFC is used, the Line current shape can be assumed to be a sinusoidal waveform.

[Equation 10](#) gives two different ones according to the inrush-current limiter used solution:

For SCR on DC side, or Triac solutions: these devices see the whole line current.

so the ON-state losses equal to:

#### Equation 11

$$P_{ON} = V_{t0} \cdot \frac{2 \cdot I_{PEAK}}{\pi} + R_d \cdot \frac{I_{PEAK}^2}{2}$$

with  $I_{PEAK}$  is the peak line current.

For mixed-bridge solution: each SCR sees only half of the line current.

So the ON-state losses per SCR equal to:

#### Equation 12

$$P_{ON} = V_{t0} \cdot \frac{I_{PEAK}}{\pi} + R_d \cdot \frac{I_{PEAK}^2}{4}$$

with  $I_{PEAK}$  is the peak line current.

If the application doesn't use a PFC, or if the line current power factor does not equal to one, then [Equation 10](#) can be used with below average and RMS values of the line current:

**Equation 13**

$$I_{AV} = \frac{I_{DC}}{\eta}$$

where  $I_{DC}$  is the average output DC current (provided by C on [Figure 3](#)) and  $\eta$  is the PFC converter efficiency (if any).

**Equation 14**

$$I_{RMS} = \frac{\sqrt{2} I_{DC}}{PF}$$

where PF is the power factor of the line current.

If the PFC efficiency or the line current power factor is not known, then device average and RMS current can directly be defined by measuring the line input current with an amperemeter.

The line current average measurement has to be performed within a half-cycle window in order not to get a null value, as the current is alternating. Another method could consist on measuring the average current after the diode bridge (assuming that the rectifier power efficiency is close to 100%).

Please also note that in case of a mixed bridge solution, the average current of each SCR is half the measured average line current. And the RMS current of each SCR is the measured RMS Line current divided by 1.41 (square root of 2).

### 3.3 Protection towards voltage surges

As a mixed bridge, like every diode bridge, is connected directly to the AC line voltage input, there is a risk of damage to the bridge and the PFC silicon devices (like bypass diode D5 in [Figure 3](#)) if a voltage surge is applied.

According to the IEC 61000-4-5 standard which describes how surges have to be performed, the surge voltage has to be applied at different angles (0°: zero positive voltage; 90°: peak positive voltage; 270°: peak negative voltage; etc.) and for both negative and positive polarities. The surge generator is coupled through capacitors and surge has to be applied between the two line terminals (line and neutral) for differential-mode test, and between one of these two terminals and the Protective-Earth for common-mode test. We explain here, for the three different cases, how a mixed bridge behaves during a differential mode surge test. Indeed a differential-mode test is usually the worst case for the mixed bridge stress, as common-mode surges can easily be clamped using Gas Discharge Tubes and low voltage varistors between both line and neutral and the earth.

For further information about the test schematic and test conditions, please refer to the IEC 61000-4-5 standard.



### 3.3.1 IEC61000-4-5 differential-mode positive surge applied at peak mains voltage

The surge test which is commonly considered to be the worst case is when a positive surge is applied at the positive peak mains voltage. The resulting input peak voltage then reaches a higher value than if the surge is applied at a different angle.

For a mixed bridge, this case is not necessarily the worst one. Most of the time, the mixed bridge is conducting at peak line voltage, unless the application is off or in stand-by mode. There are a lot of applications which are disconnected from the Line when they are off. So a surge voltage could not be applied in this case.

If we assume the bridge SCRs and diodes are conducting when the surge is applied, then the surge energy will apply a supplementary current to the SCR and the diode. But this is not necessarily an issue, as an SCR and a diode have a very high overcurrent capability. ST datasheets give for each SCR a curve of maximum peak current ( $I_{TSM}$ ) versus the pulse duration of this current. The overcurrent capability for a 20  $\mu$ s current pulse is then 60 to 100 times higher than the device current rating ( $I_{T(RMS)}$ ).

For example, we have performed a 4 kV positive surge test applied at a 90° angle with the schematic of [Figure 3](#) (without PFC). We used a 2  $\mu$ H inductor for L and a single 100  $\mu$ F capacitor for C in order to be close to the worst application case. The SCRs are two TN5050H 1200 V 50 A devices, D1 and D2 diodes, and D5 bypass diode are STBR6012 devices (which is the Automotive grade version of the 60 A 1200 V 175 °C diode). The  $R_{LIM}$  resistor is disconnected (as the 2 diodes in series) so that the tested schematic is the one used for soft-start solutions and so that the whole surge current is applied to the mixed bridge.

For a 90° angle, T1 and D1 (cf. [Figure 3](#)) are conducting. The surge energy will then increase the current level and will cause D5 to turn-on due to the voltage held by the PFC inductance. Diode D5 thus allows the surge current to be by-passed and avoid damaging the PFC freewheeling diode (D6).

[Figure 3](#) shows T1 current (so D1 and D5 current too) reaching a 1730 A peak current during the surge. The current pulse width is equivalent to a 30  $\mu$ s long half-sinus. Such a current stress is applied when the two device junction temperatures were both around 40°C. The current level here is well below the STBR6012 and TN5050H current typical capability for such a temperature.

In case the applied surge current is above the SCR or diode current capability, there are basically two ways to reduce this overcurrent (both could be used together):

1. Increasing the differential inductor will help reduce the applied peak current, but it will also slightly increase the overcurrent pulse width. Using an inductor with a higher serial parasitic resistance will have an even bigger impact to reduce the peak current but at the price of higher power losses during normal operation.
2. Adding a varistor at Line input will help reduce the peak voltage applied to the circuit, and so the overcurrent as well. The lower the voltage rating of the varistor and the higher the varistor diameter, the better will be the voltage clamping and the bridge devices surge current reduction.

Figure 12. 4 kV surge test at 90° on a mixed-bridge with TN5050H SCR

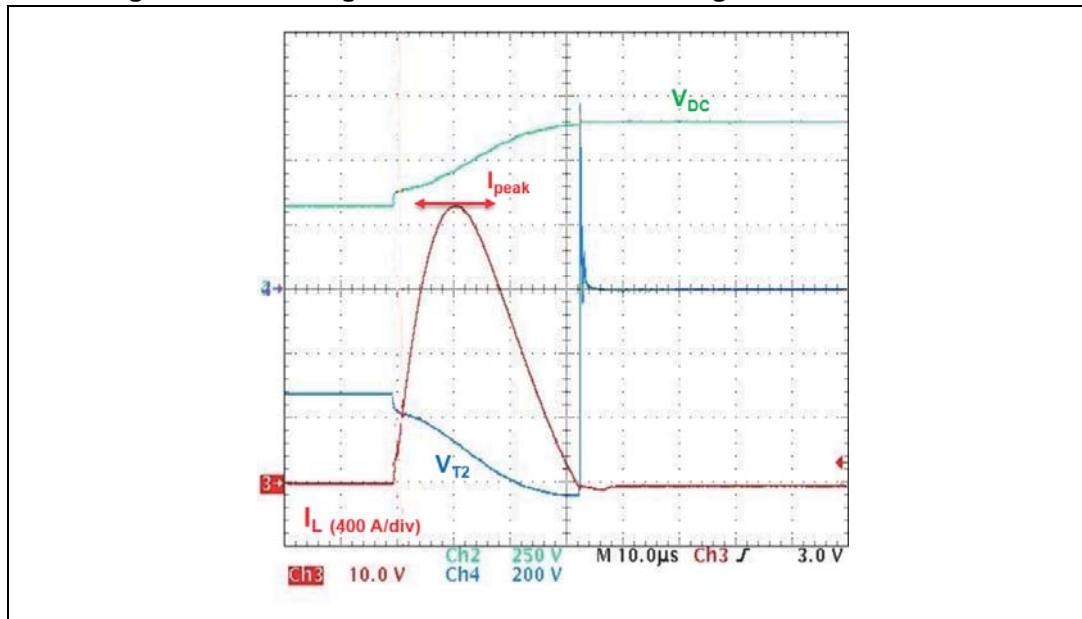


Figure 12 also shows that  $V_{DC}$  output voltage is increased by the surge current energy. The DC voltage increases then by 325 V, from the peak line voltage (325 V) to 650 V. As this voltage is reversely applied to T2 (as diode D1 is also conducting when T1 is ON) and D2, at least 800 V devices have to be used for T2 and D2. As the TN5050H and the STBR6012 are a 1200 V devices, the voltage margin is very high.

In case the reverse voltage exceeds the SCR or diode capability, limiting the surge current by using an input varistor, as previously stated, will help here too. But a better voltage limitation could be achieved by using a higher-value output capacitor or a capacitor with a lower internal parasitic series resistance.

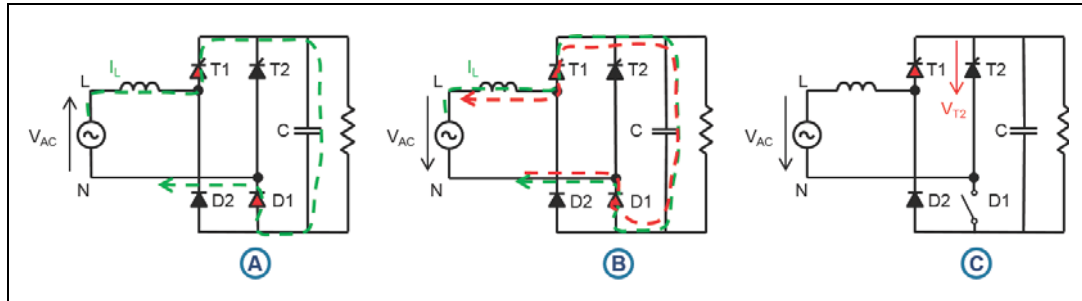
The schematic of Figure 3 has also been submitted to a 6 kV surge test with the same tests conditions as detailed above for the result presented on Figure 12. T2 and D2 reverse voltage reached then a maximum level of 840 V, which is still well below the maximum  $V_{RRM}$  capability of the STBR6012 (1200 V) and below the maximum transient voltage the TN5050H can withstand given by its  $V_{DSM}$  parameter which equals 1300 V for the TN5050H.

For a 6 kV surge, T1 overcurrent reaches 2600 A for the same 30  $\mu$ s duration. Such a current stress is above TN5050H specified  $I_{TSM}$  current capability and STBR6012 IFSM current capability. But both devices were not damaged even after 20 surges (applied with a 1 min repetition period). The circuit is then able to withstand typically a 6 kV surge.

It should be noted that the  $I_{TSM}$  curve is measured while the SCR is in the OFF state before the surge current is applied. If the SCR is already ON before an overcurrent is applied (as it is the case in above test), the SCR is able to withstand a higher current as its whole die area is already conducting. This is why the circuit can sustain here typically a 6 kV surge level.

### 3.3.2 IEC61000-4-5 differential-mode negative surge applied at peak mains voltage

Figure 13. Mixed-bridge behavior sequences for negative surge test at 90°



**Phase A:** normal mixed bridge operation before the surge is applied.  $V_{AC}$  voltage is positive, so T1 and D1 are conducting. The Line current ( $I_L$ , cf. dashed green line) is circulating from L to N through T1, D1 and the output capacitor.

**Phase B:** a negative surge is applied coupled to the Line.  $V_{AC}$  becomes then negative. This means that a negative current (represented by the red dashed Line) will now be circulating from N to L. This current will increase to reach the level of the Line current during phase A leading to the line current to reach zero.

**Phase C:** as explained before, the Line current has decreased following  $V_{AC}$  inversion. When  $I_L$  current reaches zero, D1 diode turns off. T1 should also turn off but as an SCR usually has more carriers to recombine compared to a diode (due to the double injection of the 2 embedded PN junctions in a SCR), T1 can still be ON when D1 turns off. Furthermore, as the Line voltage is supposed to be positive at this moment, T2 is not triggered by the control circuit (this is done to avoid leakage current increase as explained in [Section 3.1](#)). This means that now the whole Line voltage is applied across T2 (refer to the  $V_{T2}$  arrow in red to highlight this point) as T1 is still on.

Phase C has to be carefully managed. If the voltage increases above the breakdown voltage of the SCR, the device may be damaged by breakover. It should be noted that for most of the cases, if the surge current is not too high, the SCR could turn-on by breakover without failure. But such an operating mode is not guaranteed for most SCR and AC switches, so it is better to implement a solution to prevent this. Two solutions are presented here.

#### SCR overvoltage protection by crowbar strategy

One solution is to use a Transil overvoltage protection device connected between the SCR Anode and Gate (as shown on [Figure 14](#) where we see the Transil protection is active as soon as a 1 kV negative surge is applied). In this case, during phase C, the voltage will increase up to the Transil breakdown voltage ( $V_{BR}$ ). The Transil diode will then start to conduct and will apply a current to the SCR gate and trigger it. [Figure 14](#) gives a result showing such behavior:

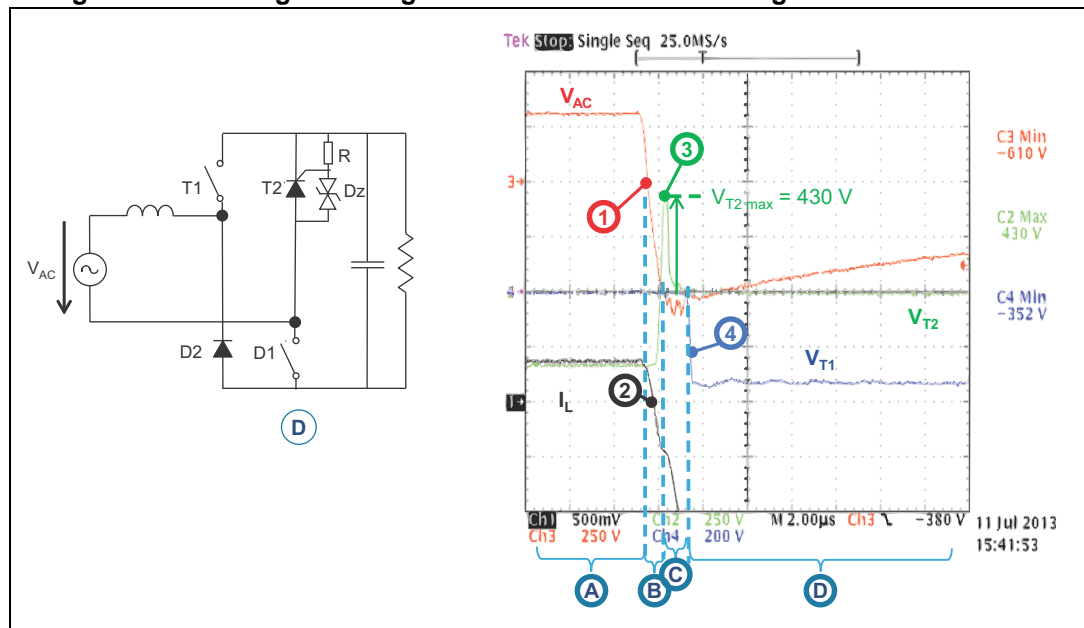
Phase A ends at point 1 where voltage  $V_{AC}$  becomes negative.

Phase B ends at point 2 where the line current reaches zero. In fact, due to D1 diode recombination, phase B ends a little bit later (the light-blue dashed line appears, where we see a voltage increase across T2, this means that D1 is really OFF).

During phase C, T2 turns on at point 3 where the voltage exceeds the Transil breakdown voltage. The maximum voltage applied to T2 is limited to 430 V. Then as T2 is ON, D2 can also turn on and applies the surge energy, which charges the output capacitor. As D2 is ON, a reverse current will circulate through T1 and recombine its minority carriers. This phase ends at point 4 where we see that a negative voltage is applied across T1 (this means that T1 actually turns off).

Phase D starts after point 4. The surge current is applied to the output capacitor through T2 and D2. T1 and D1 are off. This phase ends when the surge current reaches zero leading to T2 and D2 turn-off. The AC voltage will come back to a positive voltage as the surge energy is dissipated. T1 will turn back on only if it is triggered again.

**Figure 14. 1 kV negative surge test at 90° on a mixed-bridge with TN5050H SCR**



In [Figure 14](#) we did not use on purpose a 400 A/div scale for  $I_L$  current, as in [Figure 12](#) as we wanted to highlight point 2 where  $I_L$  reaches zero. The surge current for a 4 kV surge also reaches here a 1730 A maximum level, which is below the typical TN5050H  $I_{TSM}$  (for a 40 °C junction temperature as in our test) and STBR6012  $I_{FSM}$  for a 30 µs pulse width.

For the Transil, we used a 1.5KE400CA device for our tests (performed with [Figure 3](#) schematic without PFC, with a 2 µH inductor for L and a 100 µF capacitor for C; TN5050H SCR and STBR6012 for D1, D2 and D5 diodes;  $R_{LIM}$  resistor disconnected). This Transil diode allows the clamping voltage to be limited to a very low peak level (430 V), and this is a particularly important point as during phase C, the absolute value of the negative voltage applied to D1 equals the sum of  $V_{T2}$  and  $V_{DC}$ . For a 325 V output DC voltage, this means that D1 sees a 755 V negative peak voltage (which is OK for the STBR6012). A higher voltage Transil or a lower energy Transil (1.5KE400CA is a 1500 W Transil) will lead to a higher clamping voltage, and so a higher voltage applied to D1.

The resistor connected between T2 gate and cathode (cf. [Figure 14](#) or [Figure 15](#)) is used to deviate the current coming from Dz Transil diode. Indeed, each time a  $dV/dt$  voltage transient is applied to Dz, a current will circulate through the Transil due to its internal parasitic capacitor. This current may trigger T2. This is why resistor R is added. Usually a 50 to 100 Ohm value allows the  $dV/dt$  withstand of the SCR not to be decreased too much.

It should also be noted that the circuit given in [Figure 14](#), the Dz Transil diode is connected in parallel to the output DC capacitor when D1 is on. Then, in case for example of a positive surge applied with a  $0^\circ$  to  $180^\circ$  angle, the DC voltage will be applied to the series association of Dz and the R resistor.

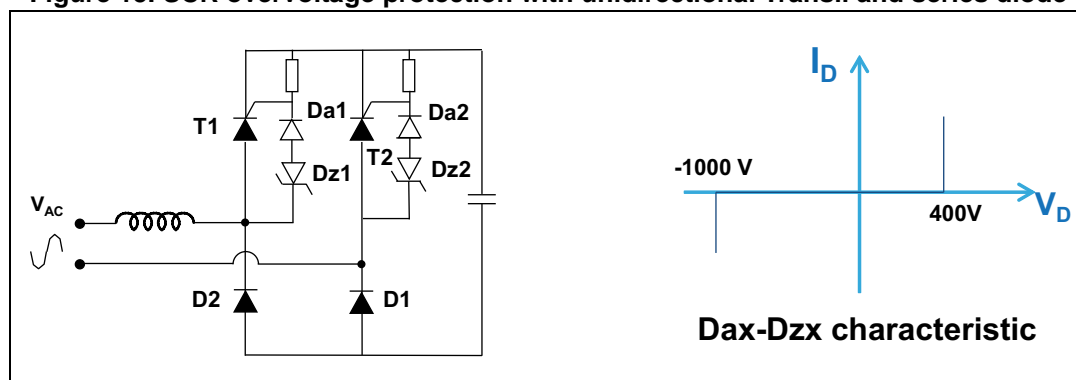
On [Figure 12](#), we have seen that the DC voltage can reach a 650 V peak value. With a 1.5KE400CA device and a 50 Ohm resistor in series, the voltage across the Transil will approximately reach 500 V, and so its current will reach 3 A. Such a current stress is OK for the 1.5KE400CA which is able to sustain a 5 A peak current for a 10/1000 $\mu$ s waveform (as guaranteed in the device datasheet). But a 3 A current through R resistor also means a 150 V reverse voltage applied to the G-K junction. This level is well above the maximum reverse voltage which can be applied to the G-K junction of any SCR.

Also for different circuits, and especially in case the output capacitor value is lower, the DC voltage can reach a higher value, leading to a higher stress to the Transil which could be damaged as here, for reverse voltages, SCR T1 and T2 will not be triggered. And the applied voltage could be applied a too long time.

For these two reasons, it would be better to use the circuit shown in [Figure 15](#), where a diode (Da1 or Da2) is added in series with a 1.5KE400A unidirectional Transil (Dz1 or Dz2). A 1 A 1000 V diode is enough like for example the STTH110 (or STTH112 for a 1200 V voltage capability).

The static characteristic of the series association is then the one shown in [Figure 15](#) For a forward 400 V applied voltage, the SCR will be triggered. For a reverse voltage up to 1000 V, no current will be deviated by the Transil. A bidirectional Transil can still be used in series with Da1 and Da2 to reach a 1400 V reverse voltage capability of this series association.

**Figure 15. SCR overvoltage protection with unidirectional Transil and series diode**



### SCR overvoltage protection with clamping devices

In case a turn-on of the SCR above 430 V is not desired, or in case the surge current exceeds the SCR  $I_{TSM}$  capability when the device is triggered by the Transil, there is another solution: using voltage suppressors such as metal oxide varistors at the bridge input instead of Transil diodes between anodes and gates. [Figure 15](#) gives a typical front-end schematic with such a solution. Varistors MOV1 and MOV2 are put behind the EMI filter in order to limit their absorbed current thanks to the filter impedance (especially the differential-mode inductance of common-mode choke L1).

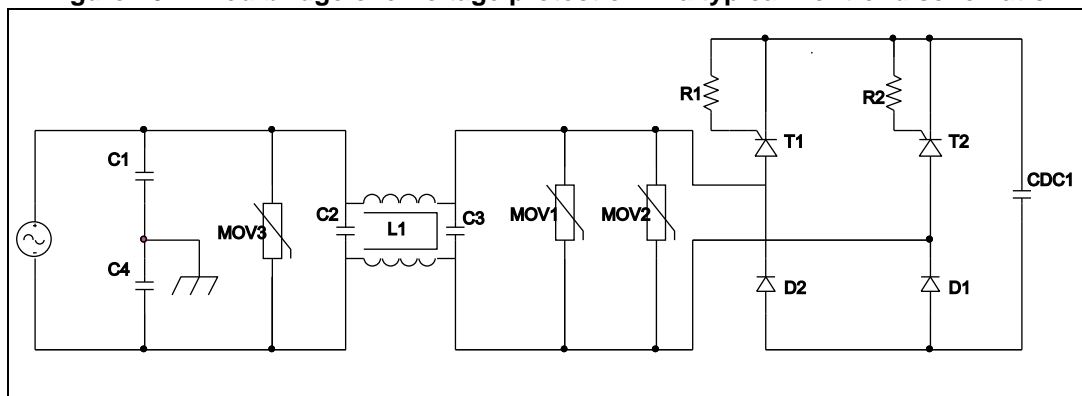
Several varistors can be used in parallel to better clamp the voltage surge and avoid turning on T2 in case of a negative surge applied at a  $90^\circ$  angle (or T1 turn-on in case of a positive

surge applied at 270°). Please note that T1 and T2 do not need to be protected anymore by Transil in this solution.

The surge withstanding level will then depend on the varistor capability to clamp the surge voltage below the T1/T2 SCR  $V_{DSM}/V_{RSM}$  and D1/D2 diodes  $V_{RRM}$ . The SCR overcurrent is no longer an issue. For example, with four 385 V 14 mm MOV in parallel, and with a typical EMI filter, the mixed-bridge voltage was limited to 1100 V even for a 6 kV surge, which is well below the TN5050H VDSM capability and typical STBR6012 breakdown voltage. The circuit is then typically able to sustain a 6 kV surge.

This solution with MOV protection is also efficient to protect the SCR when the surges are applied while the thyristors are OFF. Indeed, if the maximum voltage is well clamped below the  $V_{DSM}/V_{RSM}$  level, the devices will remain OFF and no current surge will be applied to them.

**Figure 16. Mixed-bridge overvoltage protection in a typical front-end schematic**



### 3.3.3 IEC61000-4-5 differential-mode positive surge applied at zero mains voltage

In case a positive surge is applied at a 0° angle (or a negative surge applied at 180°), T1 will absorb (or T2) the surge current if it is already triggered or if a Transil diode is used as shown in [Figure 11](#).

With the schematic previously used ([Figure 3](#) schematic without PFC, with a 2  $\mu$ H inductor for L and a 100  $\mu$ F capacitor for C; TN5050H SCR and STBR6012 for D1, D2 and D5 diodes;  $R_{LIM}$  resistor disconnected), in case of SCR conduction, the surge current will reach 1730 A for a 4 kV surge, which is below the TN5050H  $I_{TSM}$  capability.

In case a higher surge voltage is applied, the overcurrent could exceed the SCR overcurrent capability. For a 0° or 180° angle, as the SCR does not conduct any current, its current capability is then not higher than the  $I_{TSM}$  curve given in the device datasheet, as previously explained.

To avoid damage of the SCR damage in case a higher voltage is applied, the following solution could be implemented:

1. First, MOV varistors have to be implemented at the parallel of the mixed bridge input (as shown in [Figure 15](#)) to limit the maximum voltage below the SCR  $V_{DSM}/V_{RSM}$  and diode  $V_{RRM}$  level.
2. Secondly, as the SCR has to remain OFF (to avoid a too high current applied through it), its triggering signal has to be delayed in order not to start at the early beginning of

the half-cycle. This should not impact the power factor too much if the delay is not too long.

### 3.3.4 Determination of the surge current

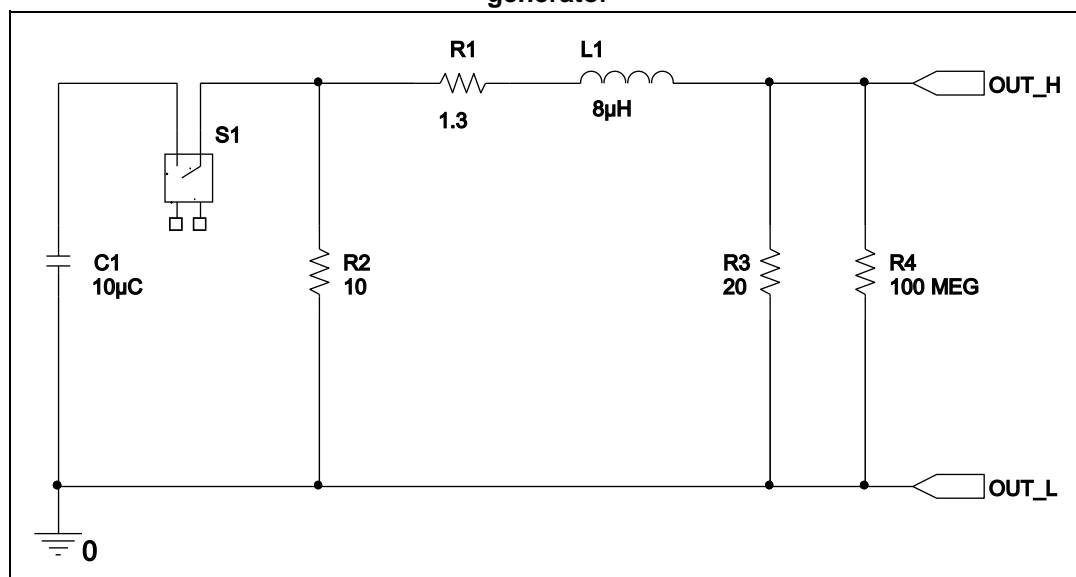
It could be very useful to determine at design-level, what would be the surge current for a given front-end circuit. This will allow the right SCR or diode P/N to be selected before performing the IEC 61000-4-5 surge tests.

The surge current can then be simulated with a circuit simulation (for example with PSPICE software). For such a simulation, a surge generator has to be modeled to provide the 1.2/50  $\mu$ s voltage waveform in open-circuit and the 8/20  $\mu$ s current waveform in short-circuit as described in the IEC 61000-4-5 standard. [Figure 16](#) gives a schematic of such a generator. Switch S1 has to be switched on when the surge has to be applied. Capacitor C1 has to be charged initially to the desired voltage surge level (1 kV, 2 kV, 4 kV, etc.).

Terminals “OUT\_H” and “OUT\_L” have to be coupled to the simulated schematic to analyze. This coupling could be done directly, if possible, or through coupling capacitors as is done in a real IEC 61000-4-5 surge test (which is done usually with one 18  $\mu$ F capacitor for differential-mode test, or 9  $\mu$ F capacitor with a 10 Ohm resistor in series for common-mode test, connected to the generator OUT\_H output).

The simulated current obtained was 10% higher than the real measured current but with a pulse width 30% longer than during the experimentation. For sure, the accuracy of the simulated current will depend in great part on the accuracy of the component models used for the front-end schematic, and especially on all the components (capacitor, inductor, semiconductors) resistor values. But such an approach can already give a rough estimation of the board behavior, according to the used DC capacitors and differential-mode inductors.

**Figure 17. Schematic to simulate a 1.2/50  $\mu$ s voltage and 8/20  $\mu$ s current surge generator**





## 4 Conclusion

Some basic guide lines have been given to implement circuits to limit the inrush-current that could occur at bridge plug-in or after Line voltage dips or interrupts.

Several topologies, using SCR or Triacs, have been presented. Some guidelines have been given about the selection criteria. These criteria mainly depend on the application performance requirements, for example the need for a voltage doubler, or the application power range, etc.

The major control circuits used in this kind of application, with opto-transistors and pulse transformers, have also been presented. Some guidelines have been given on how to design such circuits and ensure a correct operation with the selected Thyristor (SCR) or Triac, and diode.

We have particularly given some tips on how to design the mixed bridge circuit to protect the design effectively from an overvoltage. Experimental results show that a 4 kV to 6 kV withstanding level of the bridge, and consequently of the whole application including the PFC if any, can easily and cost-effectively be achieved when right EMI filter and overvoltage protection devices are selected.

## 5 References

[1] AN533, "SCRs, Triacs, and AC Switches: Thermal management precautions for handling and mounting", ST Application Note.

[2] AN1966, "Triac overvoltage protection using a Transil™", ST Application Note.

[3] AN2703, "Parameter list for SCRs, Triacs, AC Switches, and Diacs", ST Application Note.

[4] AN4363, "How to select the Triac, ACS, or ACST that fits your application", ST Application Note.



## 6 Revision history

**Table 1. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
21-Apr-2015	1	Initial release.
07-Mar-2016	2	Mixed bridge diodes reference modification from STTH6010 to STBR6012 (1200 V instead of 1000 V).

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