AN1131
APPLICATION NOTE

MIGRATING APPLICATIONS FROM ST72511/311/314/124 TO ST72521/321/324

by Microcontroller Division Applications

1 INTRODUCTION

This application note provides information on migrating ST72511/311R, 314N, 314/124J applications to the ST72521/321R, 321/324J family. The ST72521/321R, 321/324J family is designed and manufactured in a more recent technology.

Table 1. Migration Cross-Reference Table

From	ST72(T)511R	ST72(T)311R	ST72(T)314N	ST72(T)314J	ST72(T)124J
To	ST72(F)521R	ST72(F)321R	ST72(F)321R	ST72(F)324J *	ST72(F)324J *

Note: If Timer A OC2 and IC2 functions are used in the ST72314 application then you have to migrate your application to ST72321 instead of ST72324.

2 FEATURE OVERVIEW

Table 2. 64-Pin Package Migration

Feature	ST72314N	ST72311R	ST72511R	ST72321R	ST72521R
Package	64-pin (no change)				
Program Memory	CFlash/ROM	EPROM/OTP/ROM		HDFlash/ROM	
Operating Supply	3.0V to 5.5V			3.8V to 5.5V with f_{CPU} = 8MHz 3.0 to 3.6V with f_{CPU} max = 4MHz	
Register Map	128 bytes			128 bytes (minor changes)	
RESET	Transistor based pull-up CMOS V_{IL} and V_{IH}			Real pull-up resistor V_{IL}=0.16.V_{DD} and V_{IH}=0.85.V_{DD}	
I/Os	44	48 (no change)			
Slow Mode	Yes			Yes (minor programming difference)	
Active-HALT	4096 t_{CPU} delay on wake-up			no delay on wake-up	
Main Clock Out	$f_{OSC}/2$			f_{CPU}	
Watchdog	Yes			Yes (minor timing change)	
16-bit Timer	Yes			Yes (minor change in PWM and One Pulse modes)	
ART-PWM Timer	No	Yes (no change)			
SPI	Yes			Yes (control bits moved from Miscellaneous register to SPI register)	
SCI	Yes			Yes (baudrate increased, prescaler enhanced)	
I^2C	No			Yes (upward compatible)	
ADC	8-bit			10-bit (upward compatible)	
CAN	No		Yes	No	Yes (no change)
LVD	3 Levels (4.5V/4V/3.5V)	1 Level (4.5V)		3 Levels (4.5V/4V/3.5V)	
CSS	Yes (fixed frequency)	No		Yes (adapted frequency)	
Emulator	ST7MDT2-EMU2B and ST7MTD2-DVP2			ST7MDT20M-EMU3 and ST7MDT20-DVP2 (planned)	
Prog. tools	ST7MDT2-EPB2			ST7MDT20M-EPB	

Table 3. 44-Pin Package Migration

Feature	ST72314J	ST72324J	ST72321J
Package	44-pin (no change)		
Program Memory	CFlash/ROM	HDFlash/ROM	
Operating Supply	3.0V to 5.5V	3.8V to 5.5V with f_{CPU} = 8MHz 3.0 to 3.6V with f_{CPU} max = 4MHz	
Register Map	128 bytes	128 bytes (minor changes)	
RESET	Transistor based pull-up CMOS V_{IL} and V_{IH}	Real pull-up resistor V_{IL}=0.16.V_{DD} and V_{IH}=0.85.V_{DD}	
I/Os	32 (no change)		
Slow Mode	Yes	Yes (minor programming difference)	
Active-HALT	4096 t_{CPU} delay on wake-up	no delay on wake-up	
Main Clock Out	f_{OSC}/2	f_{CPU}	
Watchdog	Yes	Yes (minor timing change)	
16-bit Timer	Yes	Yes (minor change in PWM and One Pulse modes)	
		IC2, OC2 and PWM functions not available on Timer A	No change
ART-PWM Timer	No (no change)		Yes (upward compatible)
SPI	Yes	Yes (control bits moved from Miscellaneous register to SPI register)	
SCI	Yes	Yes (baudrate increased, prescaler enhanced)	
I^2C	No (no change)		Yes (upward compatible)
ADC	8-bit	10-bit (upward compatible)	
CSS	Yes (fixed frequency)	Yes (adapted frequency)	
Emulator	ST7MDT2-EMU2B and ST7MTD2-DVP2	ST7MDT20J-EMU3 and ST7MDT20-DVP2 (planned)	
Prog. tools	ST7MDT2-EPB2	ST7MDT20J-EPB	

3 HARDWARE COMPATIBILITY

3.1 PIN-OUT

The TQFP64 package devices in both families are fully pin-to-pin compatible.The only rule to observe, is that all pins labelled NC (not connected) on the ST72511/311R, 314N, 314/124J package MUST be left unconnected on the application board to be compatible with the ST72521/321R, 321/324J.

Note: The NMI in the ST72511/311R, 314N, 314/124J has been renamed called TLI (Top Level Interrupt) in the ST72521/321R, 321/324J.

3.2 HARDWARE CONFIGURATION

3.2.1 Oscillator load capacitance

Once characterization have been done crystal/ceramic manufacturer, adjustment might be necessary as the ST72521/321R, 321/324J oscillator has been optimized to reduce consumption.

3.2.2 Not Connected I/Os

The ST72314R devices are pin to pin compatible with the ST72311R/511R/321R/521R with the exception of four I/O ports which are not available (pin 28, 30, 63 and 64 are “NC”) in the ST72314R. These four I/Os have to be configured to a fixed value (output push-pull as an instance) or with an external 10KΩ pull-up to avoid unwanted consumption (by default these I/Os are floating in the ST72521/321R, 321/324J devices)

3.2.3 Asynchronous $\overline{\text{RESET}}$ pin

The noise immunity of the $\overline{\text{RESET}}$ pin has been improved by increasing the hysteresis of the schmitt trigger voltage and the low/high voltage level as given in Table 4. Also, the R_{ON} resistive transistor has been changed to a real resistor so it is not dependent on V_{DD}.

Table 4. $\overline{\text{RESET}}$ Pin Characteristics

Symbol	ST72311/511R, 314N, 314J			ST72321/521R, 321J, 324J			Unit
	Min	Typ	Max	Min	Typ	Max	
V_{IL}			$0.3xV_{DD}$			$0.16xV_{DD}$	V
V_{IH}	$0.7xV_{DD}$			$0.85xV_{DD}$			
V_{hys}		0.4			2.5		
R_{ON} 1)	20	40	60	20	30	150	kΩ
R_{ON} 2)	80	100	120				

Notes:

1. V_{DD}= 5V, 2. V_{DD}= 3.3V

4 TIMING

4.1 CYCLE ACCURACY

All timings are compatible between the ST72511/311R, 314N, 314/124J and the ST72521/321R, 321/324J devices except internal timings linked to the cycle accuracy. This means that all software with timings based on fixed processor cycle times (a practice not recommended) has to be checked out in detail. An example of this would be a software wait loop implemented as a sequence of NOP instructions as opposed to polling a busy bit).

This internal difference does not affect the general timings.

4.2 CLOCK SECURITY SYSTEM (CSS)

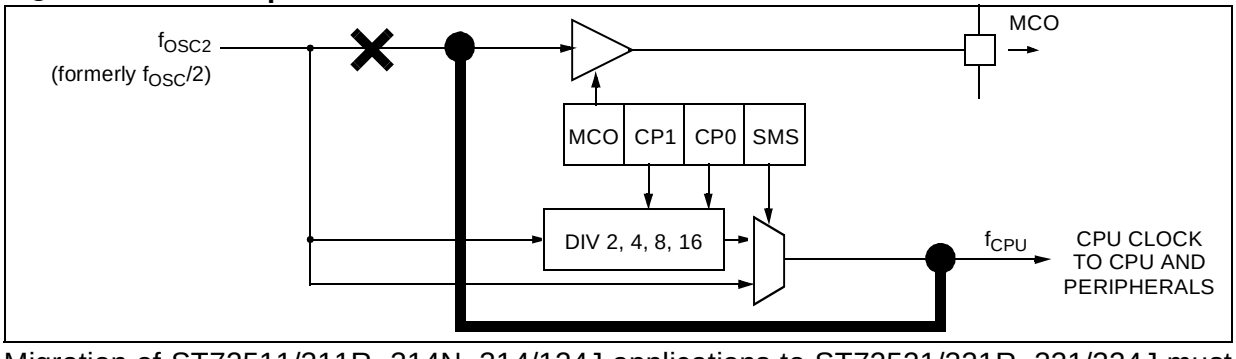
The backup oscillator of CSS available in the ST72314R device has a fixed frequency between 190kHz and 430kHz.

In the ST72521/321R, 321/324J devices, the backup oscillator frequency varies according to the initial frequency range (selected by option byte by the user) This allows to be as close as possible from the original clock frequency.

4.3 MAIN CLOCK OUT (MCO)

For more flexibility and to keep in line with the ST72F264 family, the MCO has been modified in the ST72521/321R, 321/324J to output f_{CPU} instead of $f_{OSC}/2$. This change is shown in Figure 1.

Figure 1. MCO Output



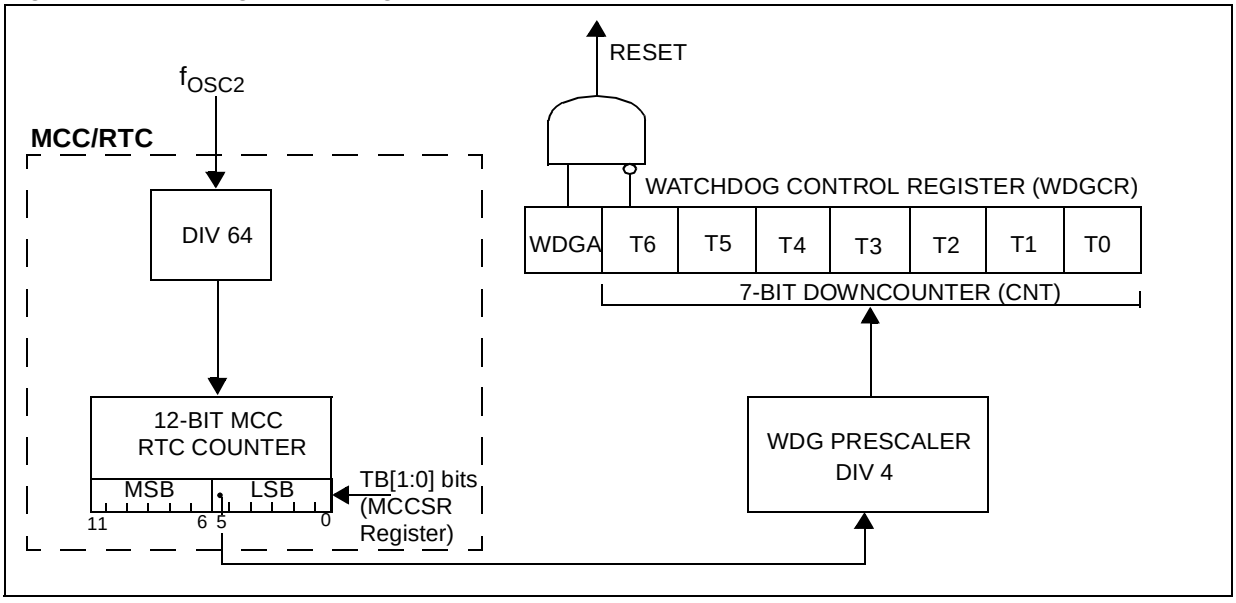
Migration of ST72511/311R, 314N, 314/124J applications to ST72521/321R, 321/324J must take this modification into account, especially for the following reasons:

1. When the application puts the ST7 in SLOW mode, the MCO output frequency is modified accordingly, unlike the ST72511/311R, 314N, 314/124J where it is kept fixed at $f_{OSC}/2$.
2. Entering HALT mode with the MCO enabled keeps the MCO line at high level whereas it is kept low in the ST72511/311R, 314N, 314/124J.
3. When exiting HALT mode, MCO is output only after a 4096 (or 256) cycle delay for clock stabilization unlike in the ST72511/311R, 314N, 314/124J where it is output almost immediately.

4.4 WATCHDOG TIMINGS

In the ST72521/321R, 321/324J, the watchdog timeout does not have an exact duration like in the ST72511/311R, 314N, 314/124J. It may vary between the min. and max. times specified in Figure 2. To guarantee upward compatibility, you have to take this into account when you develop your software. The reason for this change is that the watchdog counter has been grouped with the Active-HALT counter and SLOW mode prescaler to enhance power consumption and EMC performance.

Figure 1. Watchdog Block Diagram



The watchdog counter is no longer clocked by f_{CPU} (as it was in the ST72511/311R, 314N, 314/124J) but by f_{OSC2} divided by approx. 16384 (f_{OSC2} is the PLL output frequency when the PLL is activated or $f_{OSC}/2 = f_{CPU}$ if the PLL is disabled).

In the ST72521/321R, 321/324J datasheet, the linear relationship between the 7-bit value to be loaded in the Watchdog Counter (CNT) and the resulting timeout duration in milliseconds is described. This can be used for a quick calculation without taking the timing variations into account. If more precision is needed, use the formulae in Figure 2.

Figure 2. Exact Timeout Duration (t_{min} and t_{max})

WHERE:

t_{min0} = (LSB + 128) x 64 x t_{OSC2}

t_{max0} = 16384 x t_{OSC2}

t_{OSC2} = 125ns if f_{OSC2}=8 MHz

CNT = Value of T[6:0] bits in the WDGCR register (7 bits)

MSB and LSB are values from the table below depending on the timebase selected by the TB[1:0] bits in the MCCSR register

TB1 Bit (MCCSR Reg.)	TB0 Bit (MCCSR Reg.)	Selected MCCSR Timebase	MSB	LSB
0	0	2ms	4	59
0	1	4ms	8	53
1	0	10ms	20	35
1	1	25ms	49	54

To calculate the minimum Watchdog Timeout (t_{min}):

IF $CNT < \left[\frac{MSB}{4}\right]$ **THEN** $t_{min} = t_{min0} + 16384 \times CNT \times t_{osc2}$

ELSE $t_{min} = t_{min0} + \left[16384 \times \left(CNT - \left[\frac{4CNT}{MSB}\right]\right) + (192 + LSB) \times 64 \times \left[\frac{4CNT}{MSB}\right]\right] \times t_{osc2}$

To calculate the maximum Watchdog Timeout (t_{max}):

IF $CNT \leq \left[\frac{MSB}{4}\right]$ **THEN** $t_{max} = t_{max0} + 16384 \times CNT \times t_{osc2}$

ELSE $t_{max} = t_{max0} + \left[16384 \times \left(CNT - \left[\frac{4CNT}{MSB}\right]\right) + (192 + LSB) \times 64 \times \left[\frac{4CNT}{MSB}\right]\right] \times t_{osc2}$

Note: In the above formulae, division results must be rounded down to the next integer value.

Example:

With 2ms timeout selected in MCCSR register

Value of T[6:0] Bits in WDGCR Register (Hex.)	Min. Watchdog Timeout (ms) t_{min}	Max. Watchdog Timeout (ms) t_{max}
00	1.496	2.048
3F	128	128.552

Note: The timing variation shown in Figure 2 is due to the unknown status of the prescaler when writing to the WDGCR register.

4.5 CAN CLOCK

In the ST72511 the CAN is directly clocked by f_{OSC2}, hence not modified in slow mode. In the ST72521 the CAN clock is f_{CPU} like for all other peripherals. This means that in slow mode the CAN clock is also divided leading to a slower baudrate. Therefore in slow mode the bit timing must be adjusted or the CAN cell must be put in sleep mode.

5 REGISTER MAP

In the ST72521/321R, 321/324J, some register addresses and bit locations are changed. These changes have made it possible to use the free locations to add new features.

Note: For easy software migration, two general rules have to be followed:

- All “reserved” byte memory areas must never be “read” or “write”.
- All “reserved” or “unused” bits must be left unchanged when accessing the byte.

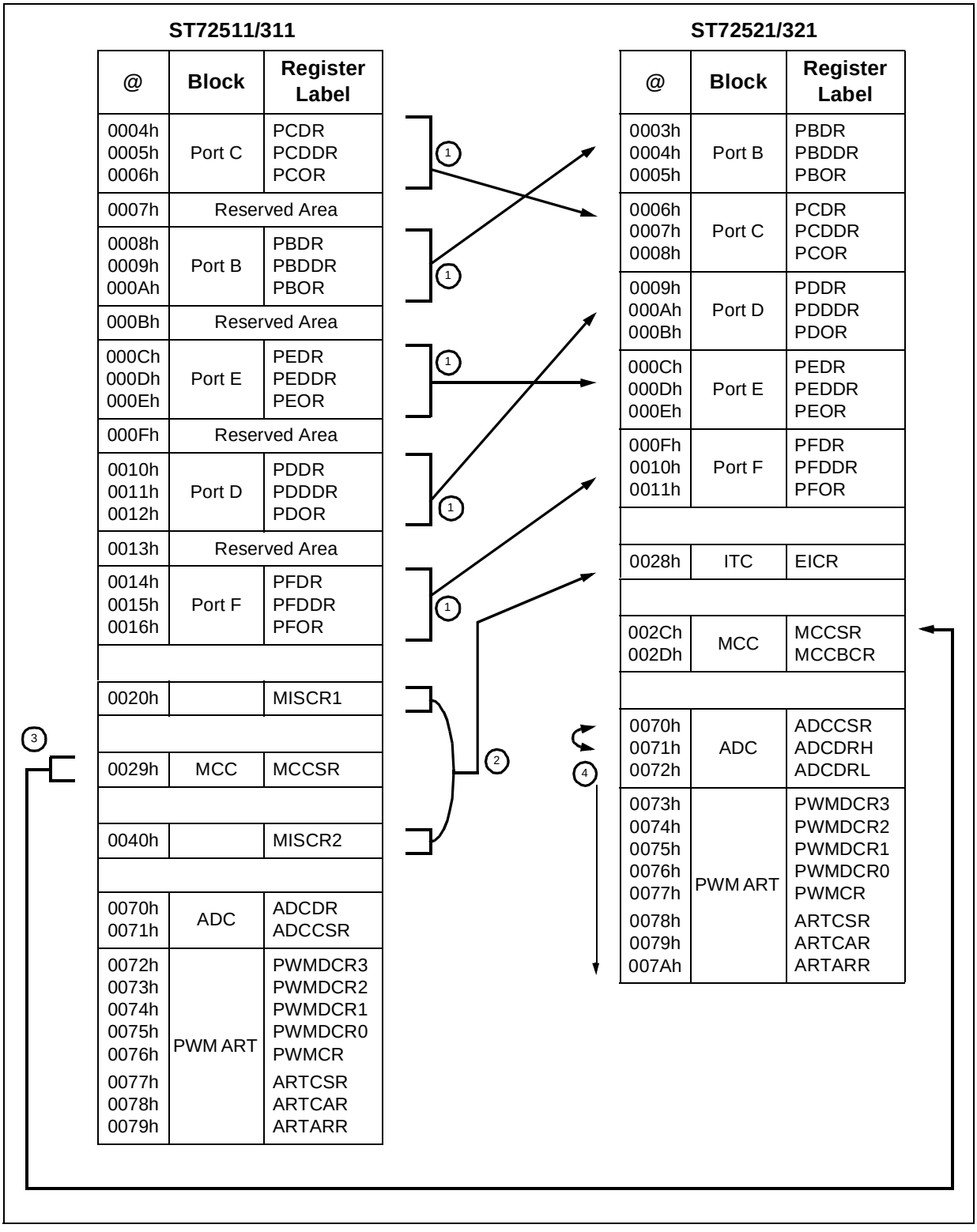
5.1 REGISTER ADDRESS

These changes are classified in four groups:

1. I/O port register addresses changed
2. Miscellaneous registers changed (see Section 5.2 for more details)
3. MCCSR register address moved
4. ADC registers swapped

Note: These register address changes can be easily performed if you group all the register definitions in a single header file.

Figure 3. Register Map Modifications



5.2 BIT LOCATION

The bit location changes only impact the ST72511/311R, 314N, 314/124J Miscellaneous registers which have been split into three different registers as shown below.

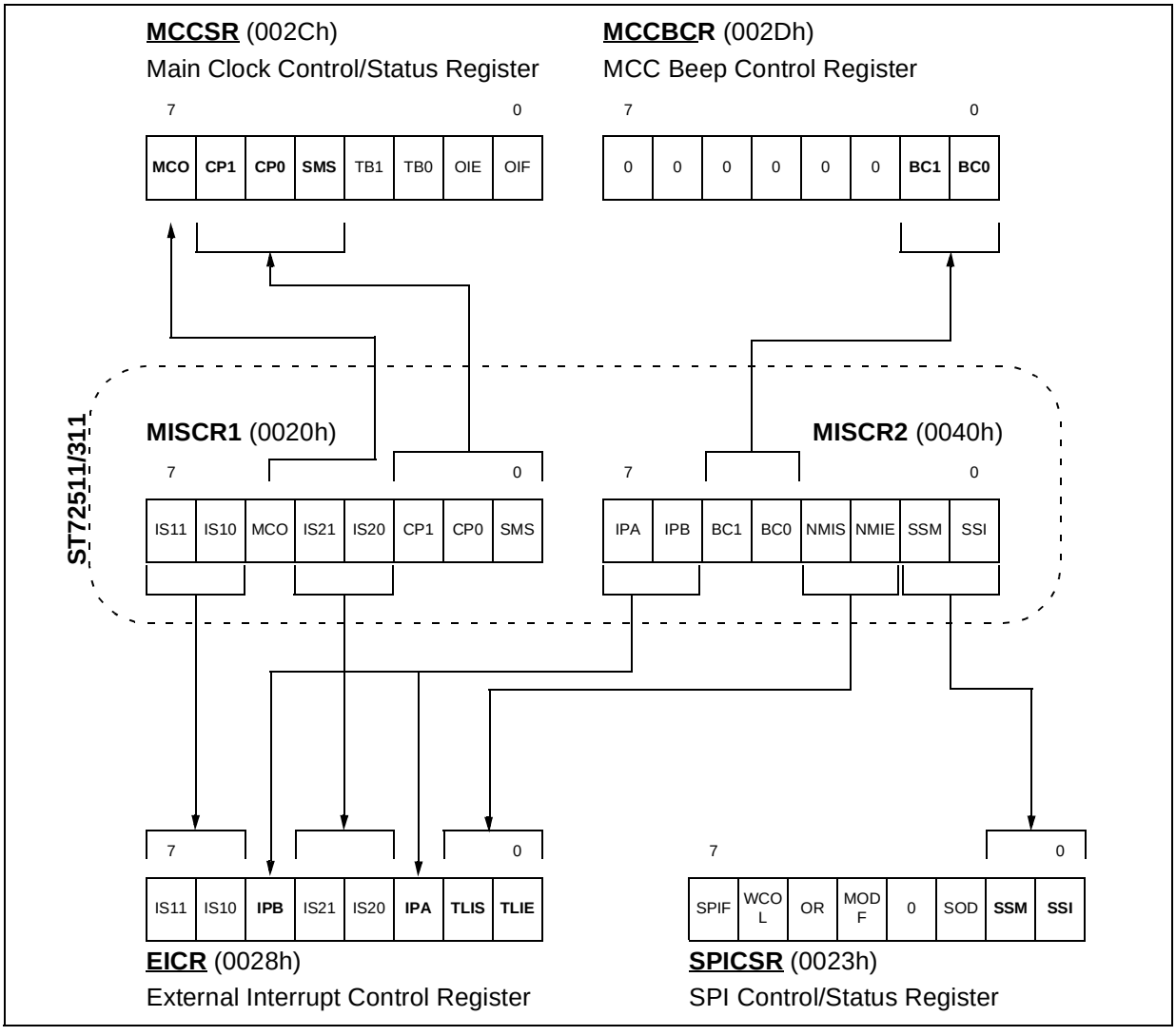
5.2.1 Main Clock System

Two registers (MCCSR and MCCBCR) manage all the features linked to the ST7 main clock system (clock-out, beep, slow and active-halt modes)

Note: The CP[1:0] bits have been modified as follows:

CP1	CP0	ST72311R/511R	ST72321R/ST72521R
0	1	$f_{OSC}/16$	$f_{OSC}/8$
1	0	$f_{OSC}/8$	$f_{OSC}/16$

Figure 4. Miscellaneous Register Bit Changes



5.2.2 External Interrupt

A single EICR register manages all the features linked to the external interrupt sources (I/O port interrupt sensitivity and TLI)

5.2.3 SPI/$\overline{SS}$ pin

The SPI $\overline{SS}$ pin alternate function is controlled from the SPI peripheral in the SPICSR register.

6 I/O PORT

6.1 EXTERNAL INTERRUPT HANDLING

To guarantee upward compatibility, the three following points have to be taken into account when you develop your application software:

– In the ST72511/311R, 314N, 314/124J, parasitic interrupts occur when software changes the I/O port configuration. In the ST72521/321R, 321/324J, these parasitic interrupts no longer occur.

– In the ST72511/311R, 314N, 314/124J, the IPA and IPB control bits can be written at any time. In the ST72521/321R, 321/324J, these two bits can be written only when interrupts are masked (I[1:0]=”10” in the CC register).

– In the ST72521/321R, 321/324J pending interrupts are cleared by software changing the value of the ISx[1:0], IPA or IPB bits. In the ST72511/311R, 314N, 314/124J this is the case only for the ISx[1:0] bits.

7 PERIPHERALS

7.1 16-BIT TIMER

The 16-bit timer of the ST72511/311R, 314N, 314/124J has been modified in the ST72521/321R, 321/324J to solve some issues related to PWM and One Pulse modes. If you use either of these two modes, you may need to change your software when transferring code from the ST72511/311 to the ST72521/321.

ST72324J family devices have one limitation versus ST72314/124J: in ST72324J, Input Capture 2 (IC2) and Output Compare 2 (OC2) functions are not available on Timer A.

All other modes of the timer do not change.

7.1.1 PWM Mode

To avoid any uncontrolled status on the PWM output, a double buffering on the output compare registers (2 x 16 bits) is implemented in the ST72521/321R, 321/324J. This double buffering is not present in the ST72511/311R, 314N, 314/124J.

In the ST72521/321R, 321/324J PWM mode, any new values written in the four OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2 event) to avoid spikes on the PWM output.

Note: Any modification on the OC1R and OC2R registers must be done just after the OC2 event (using the ICF1 interrupt routine for example).

7.1.2 One Pulse Mode

To be used more efficiently, the One Pulse mode sequence of the ST72511/311R, 314N, 314/124J has been improved in the ST72521/321R, 321/324J. When the ICAP1 event occurs (on falling or rising edge) the following sequence occurs:

– 1. IC1R is loaded with the value of the counter when the event occurred (not FFFDh as in the ST72511/311R, 314N, 314/124J)

– 2. The counter is immediately reset to FFFCh (not at the end like in the ST72511/311R, 314N, 314/124J)

– 3. OLVL2 is applied to OCMP1 pin if OC1E=1

– 4. ICF1 is set

7.1.3 ST72324J Timer A Limitations

If the Timer A IC2/OC2 functions are required when migrating from ST72314/124J then you should migrate to the ST72321J. Timer A on the ST72324 only has one IC and one OC function. This has the following impact on the application software:

– The OC2HR and OC2LR registers are reserved (see Note 2).

– The IC2HR and IC2LR registers are reserved (see Note 2).

– The FOLV2 and OLVL2 i control bits in the CR1 register must be kept cleared.

– The OC2E and IEDG2 control bits in the CR2 register must be kept cleared.

– The ICF2 and OCF2 flags must always be masked (meaningless).

– The PWM generated by timer A has a frequency given only by the timer overflow value (FFFFh) and the prescaler ratio selected by the CR2 CC[1:0] control bits.

Notes:

1. Migration from the ST72314 to the ST72324 must take into account the discrepancy in Timer A functionality between these two devices.
2. A dummy read to the OC2LR and IC2LR registers has to be performed at the end of the Timer A interrupt routine.

7.2 SPI

7.2.1 Baud Rate

On the ST72521/321R, 321/324J the baud rate configurations are extended to $f_{CPU}/4$ and $f_{CPU}/32$. The SPR2 bit in the SPICR register controls these new baud rates. To keep the SPI

baud rate compatible with the ST72511/311R, 314N, 314/124J the SPR2 bit must be left cleared.

7.2.2 HALT mode

The ST72521/321R, 321/324J is able to exit from HALT mode through a SPI interrupt. This is not the case in the ST72511/311R, 314N, 314/124J. To guarantee upward compatibility, if the SPI is used in slave mode, the SPI interrupt must be masked (via the SPE or SPIE bits) during HALT mode to avoid any unwanted wake-up event.

7.3 10-BIT ADC

To meet application requirements for increased resolution, the ST72521/321R, 321/324J has a 10-bit ADC compared to the 8-bit ADC in the ST72511/311R, 314N, 314/124J. For upward compatibility, both ADCs have identical control registers and operating modes. The 8 most significant bits of the ST72521/321R, 321/324J data register (ADCDRH) are used in place of the ADCDR register of the ST72511/311R, 314N, 314/124J.

7.4 SCI

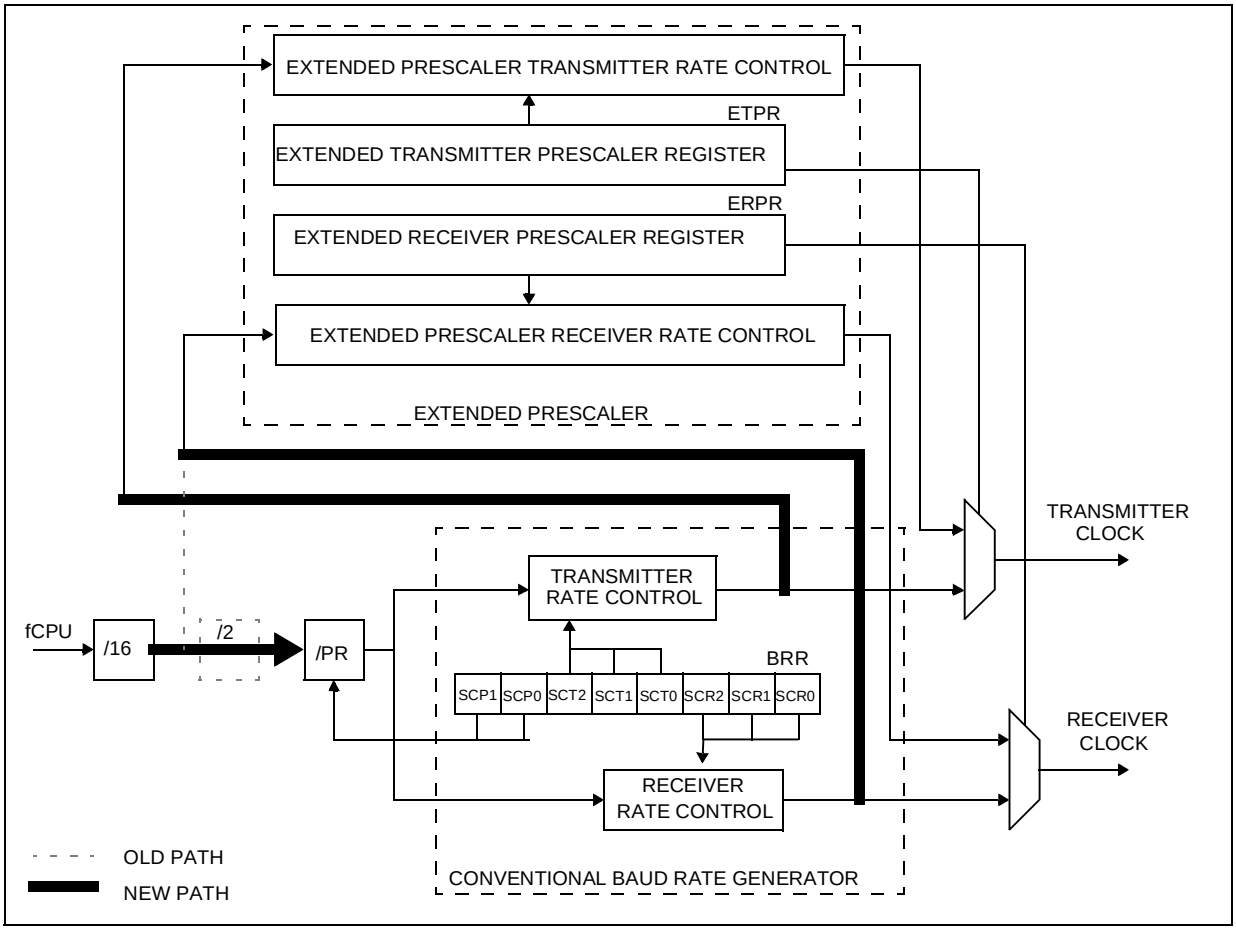
7.4.1 SCI Prescaler

To reach higher communication speeds and to increase the number of possible frequencies, the SCI prescaler has been modified in the ST72521/321R, 321/324J. These changes will require a simple software change to program the correct baud rate. The two changes are listed below and illustrated in Figure 5:

– The division by 2 of the input clock is removed in the ST72521/321R, 321/324J to reach higher speed.

– The enhanced prescaler is cascaded with the conventional prescaler after the PR prescaler to increase the number of possible frequencies.

Figure 5. SCI Baud Rate Prescalers



7.4.2 SCI TDO pin

In the ST72511/311R, 314N, 314/124J, the TDO alternate function is released when the TE bit is reset.

In the ST72521/321R, 321/324J, the TDO alternate function is released if both the TE and RE bits are reset. As a consequence, when the SCI is used for reception (through RDI) the TDO pin can not be used as a standard I/O.

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