AN4209
Application note

Design methodology for repetitive voltage suppressors (RVS) in repetitive mode: STRVS

Introduction

The silicon transient voltage suppressor (TVS) device such as the Transil™ was initially specified with a power surge capability to respond to industrial standard test conditions, especially against high-energy single transient voltages. Today, many components in switched mode power supplies are continuously subjected to very short transient voltages. Little data is given in TVS specifications regarding the repetitive mode operation. Therefore, it is not easy for the designer to accurately assess the clamping voltage and power losses under these conditions.

This application note introduces the new repetitive voltage suppressor STRVSX features, specifically adapted to the repetitive mode operation. A design guideline is presented and selection processes are described.

Contents

1 STRVS parameters

This section defines the electrical and thermal characteristics of the STRVS.

1.1 Electrical parameters

Figure 1. Typical reverse characteristic $V_R = (I_R)$ of an STRVS device

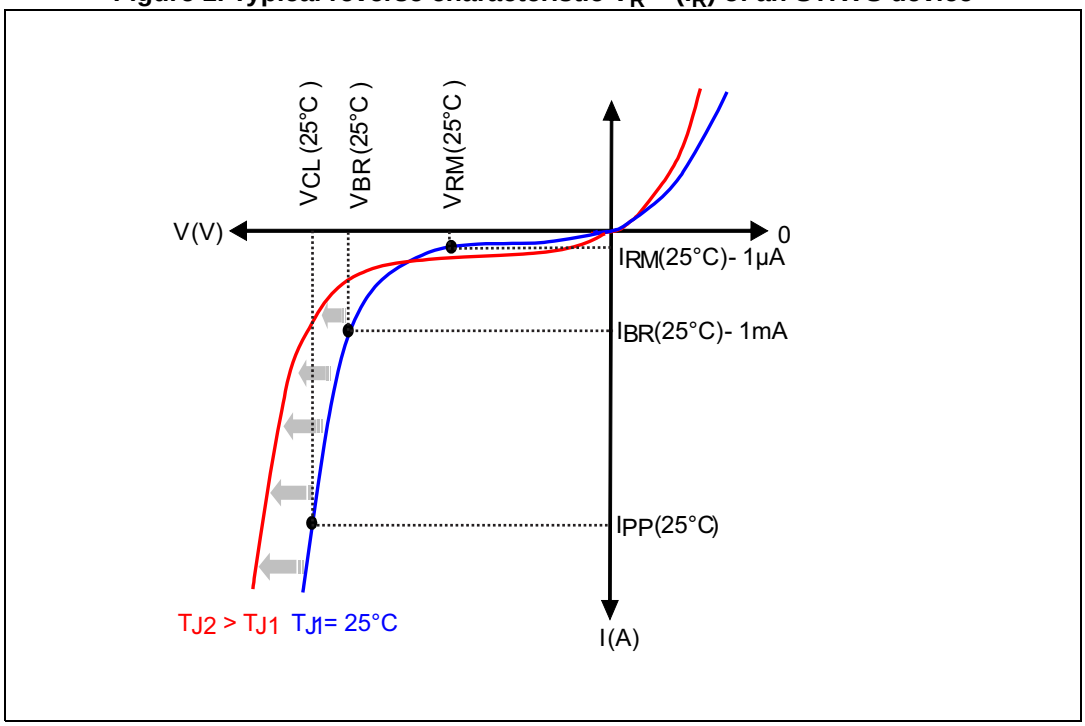


Figure 1 shows the typical reverse characteristic given at two temperatures of an STRVS device.

Stand-off voltage (V_{RM})

The stand-off voltage is specified for I = I_{RM} = 1 µA and T_j = 25 °C. Under these conditions, the device is still acting as an open circuit. This parameter is one of the key parameters in circuit protection.

Breakdown voltage (V_{BR})

The breakdown voltage corresponds to the voltage from which the STRVS starts to go into the avalanche region. This parameter is specified for I = I_{BR} = 1 mA and T_j = 25 °C. The V_{BR} parameter follows a linear variation with junction temperature as shown in *Equation 1*.

Equation 1

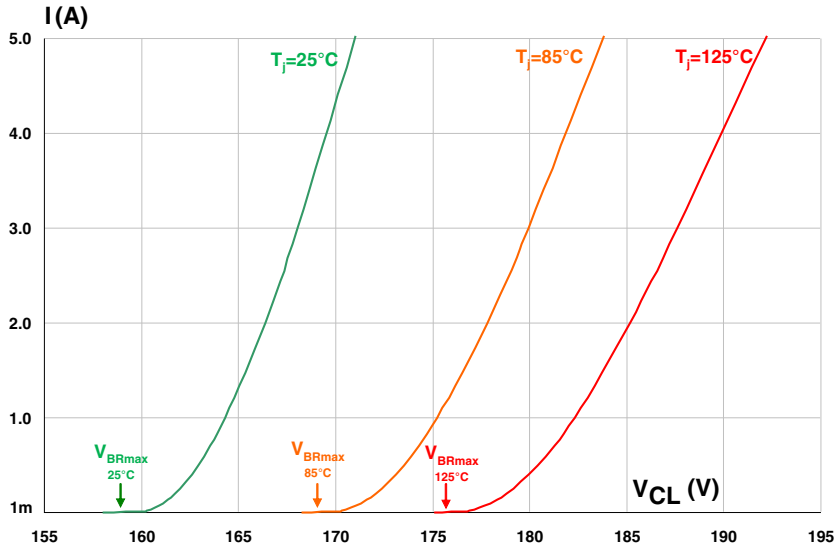
$$V_{BR}(T_j) = V_{BR}(T_{REF}) \cdot \left(1 + \alpha_T \cdot (T_j - T_{REF})\right)$$

Where T_{REF} = reference temperature expressed in °C, generally given at 25 °C and αT = temperature coefficient in 1/°C.

Clamping voltage (V_{CL})

The clamping voltage is the total voltage across the STRVS over the peak pulse current I_{PP} at a given temperature. A range of typical values provides the characteristics of the clamping voltage for given values of peak current (I_{PP}), and three controlled junction temperatures: 25 °C, 85 °C and 125 °C. All curves start from V_{CL}(1 mA) = V_{BRmax}. *Figure 2* illustrates V_{CL} curves of an STRVS185X02B. These curves are useful for verifying the suitability of the allowable clamping voltage in application.

Figure 2. Clamping voltage characteristic over temperatures of an STRVS185X02B



1.1.1 Simplified electrical model

A linear model can be employed to approximate the V_{CL} = f (I_{PP}) characteristics of the STRVS. A straight line is used to approximate the actual curve inside the working area imposed by the application conditions (see *Figure 3*). The line intersects the horizontal axis at the voltage V_{CL0}. The slope of the line is inversely proportional to the dynamic resistance R_D. The equivalent circuit that models this equation is shown in *Figure 4.*

Figure 3. Simplified characteristics of an STRVS device

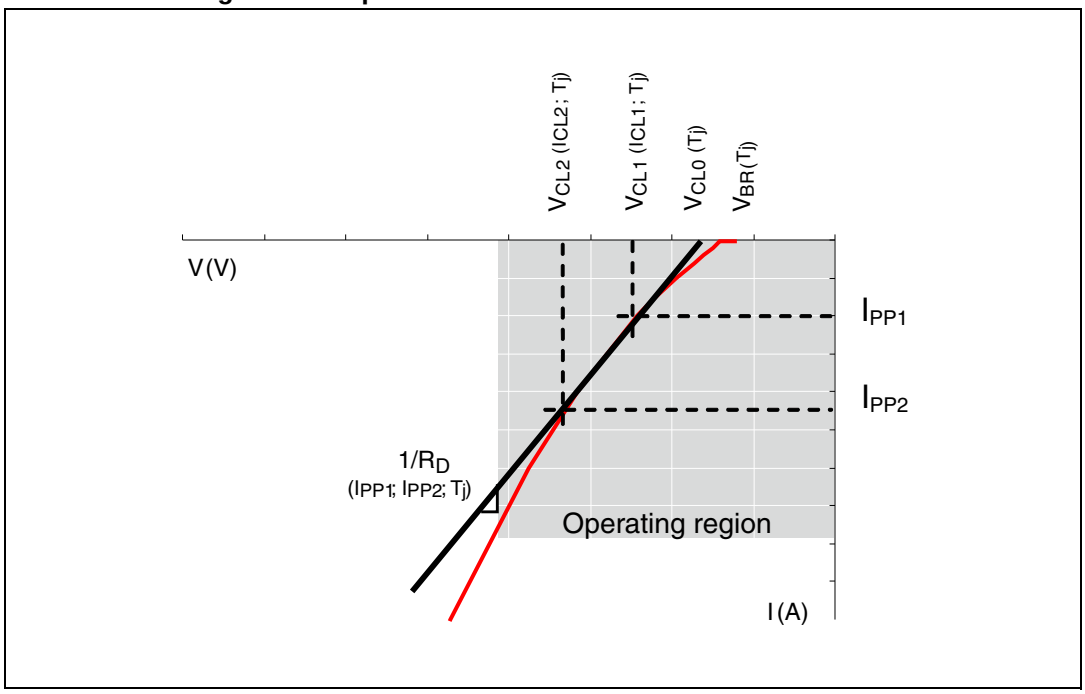
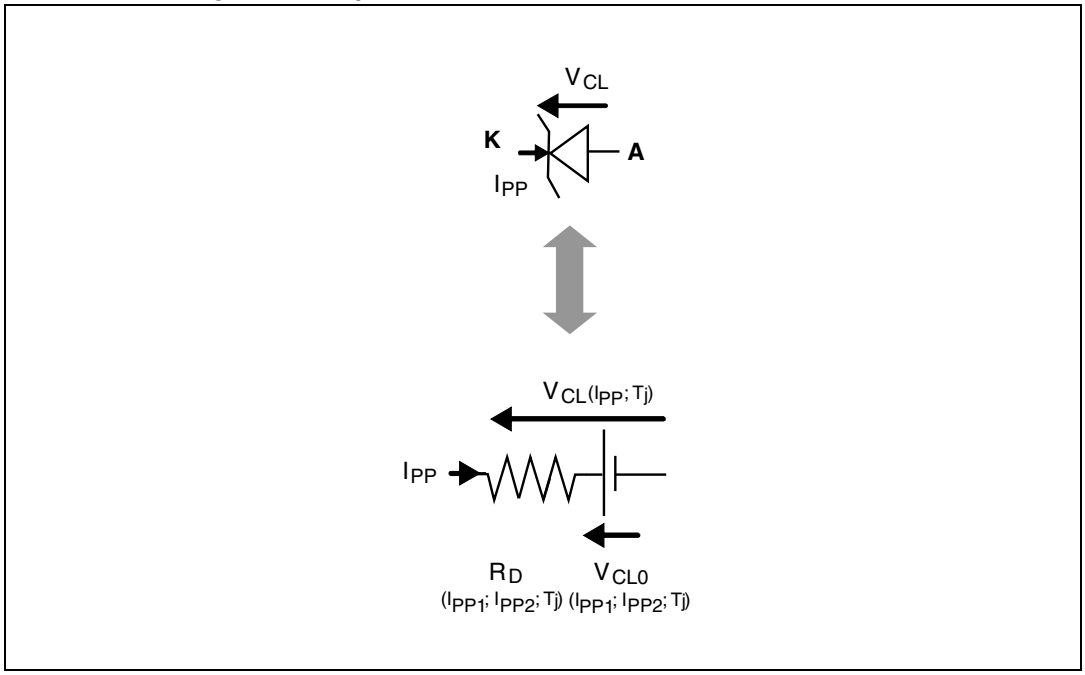


Figure 4. Simplified electrical model of an STRVS device



A simple rule to calculate R_D and V_{CL0} is to use $I_{PP2}=I_{peak}$ of the application and $I_{PP1} = I_{PP2} / 2$

The clamping voltage is defined in *Equation 2*.

Equation 2

$$V_{CL}(I_{PP};T_j) = V_{CL0}(I_{PP1};I_{PP2};T_j) + R_D(I_{PP1};I_{PP2};T_j) \cdot I_{PP}$$

R_D can be calculated as shown in *Equation 3*.

Equation 3

$$R_D(I_{PP1};I_{PP2};T_J) = \frac{V_{CL2}(I_{PP2};T_j) - V_{CL1}(I_{PP1};T_j)}{I_{PP2} - I_{PP1}}$$

V_{CL0} is shown in *Equation 4*

Equation 4

$$V_{CL0}(I_{PP1};I_{PP2};T_j) = V_{CL1}(I_{PP1};T_j) - R_D(I_{PP1};I_{PP2};T_j)\cdot I_{PP1}$$

This model will be useful to assess the power dissipation of the device.

1.2 Thermal parameters

1.2.1 Steady state parameters

Thermal resistance ($R_{th(j\text{-}Ref)}$)

The thermal resistance represents the package's dissipation capability from the junction (active die surface) to a specified reference point (case, lead, board, ambient, etc…). Its value is defined as the temperature difference between two specified points, divided by the dissipated power under thermal equilibrium conditions.

Equation 5

$$R_{TH(j\text{-}Ref)} = \frac{T_j - T_{Ref}}{P_D}$$

Where:

$R_{th(j\text{-}Ref)}$	Junction-to-reference thermal resistance expressed in °C/W
P_D	Average dissipated power of the die, expressed in W
T_j	Junction temperature of the die expressed in °C
T_{Ref}	Temperature of the reference point expressed in °C

The previous equation can be easily reworked to estimate the junction temperature in steady mode operation as shown in *Equation 6*.

Equation 6

$$T_j = R_{TH(j\text{-}Ref)}\cdot P_D + T_{Ref}$$

In STRVSX specifications, the junction-to-lead ($R_{th(j\text{-}l)}$) and junction-to-ambient ($R_{th(j\text{-}a)}$) thermal resistances are commonly provided to help designers. These parameters are determined under standard test conditions with specific board dimensions and layers in compliance with the JEDEC standard.

Table 1 shows typical thermal resistances for available packages.

Table 1. Typical package performance comparison for minimum footprint and 35 µm copper thickness on board

Thermal resistance	Package				Unit
	DO-15	DO-201	SMB	SMC	
Junction-to-lead, $R_{th(j-l)}$	35	23	13	12	°C/W
Junction-to-ambient $R_{th(j-a)}$	105	100	185	150	°C/W

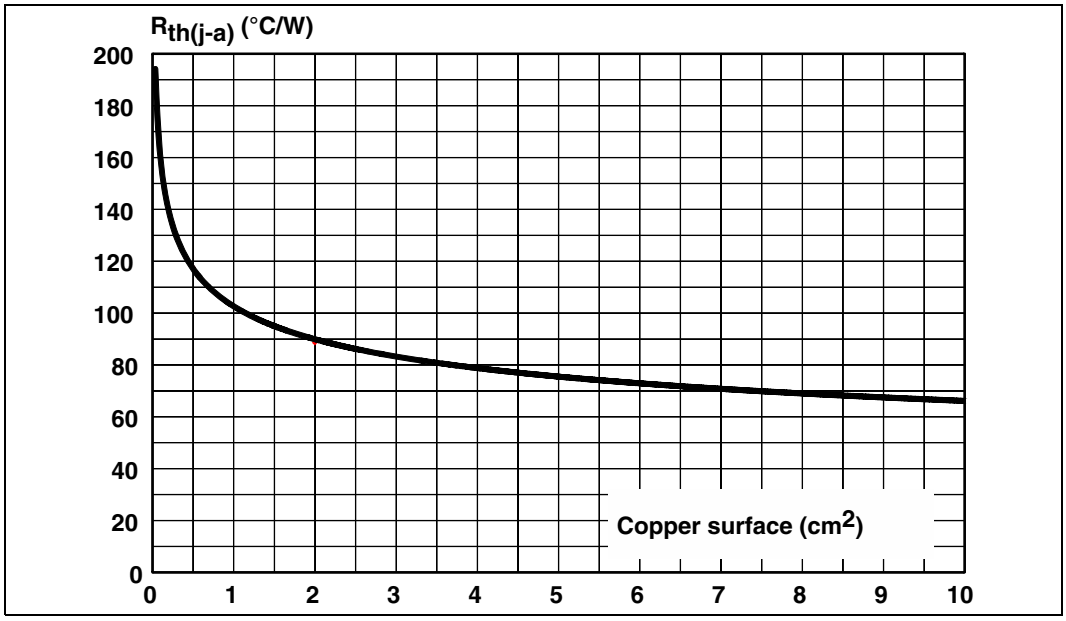
Junction-to-ambient thermal resistance ($R_{th(j-a)}$)

The thermal resistance $R_{th(j-a)}$ is the heat dissipation capability from the junction surface of the die to the ambient, via all paths. Its value is strongly dependent on the type of board, the copper plane underneath the device, the neighboring components interacting through the PCB, and the mounting and cooling methods (free or forced airflow).

Actual performance of the product in real applications may be different. Values provided in datasheet are typical values and should be used with some measure of caution. It is useful for comparing the thermal performance of one package to another as shown in *Table 1*.

Therefore, this information may be used for the first pass of junction temperature calculation. The thermal resistance $R_{th(j-a)}$ value with minimum footprint is recommended when the user starts a design calculation. *Figure 5* shows the $R_{th(j-a)}$ dependency of a SMB package over copper plane area.

Figure 5. Junction-to-ambient thermal resistance over copper plane area of SMB package



Junction-to-lead thermal resistance ($R_{th(j-l)}$)

The thermal resistance $R_{th(j-l)}$ is the heat dissipation capability from the junction surface of the die to the package lead. This parameter is useful for estimating the junction temperature from a measurement of the lead temperature. The designer can determine the lead temperature of the device under application conditions with a fine gauge thermocouple or

infrared camera and calculate the junction temperature using *Equation 6*. The lead is the most interesting reference point to evaluate accurately the average operating junction temperature T_{javg}. The thermal resistance value $R_{th(j-l)}$ depends only on the package proprieties unlike $R_{th(j-a)}$.

1.2.2 Transient parameter

Transient thermal impedance ($Z_{TH(j-Ref)}(t_p)$)

The transient thermal impedance $Z_{TH(j-Ref)}(t_p)$ is the temporary variation of thermal resistance from an input power step function up to reaching a stable value as defined *Equation 7*.

Equation 7

$$\lim tp \rightarrow \infty Z_{th(j-Ref)}(tp) = R_{th(j-Ref)}$$

Transient thermal impedance can be calculated using *Equation 8*.

Equation 8

$$Z_{TH_{(j-Ref)}}(t_p) = \frac{T_j(t_p) - T_{Ref}}{P_{Step}}$$

Where:

$Z_{TH(j-Ref)}$	Junction to reference transient thermal impedance expressed in °C/W.
t_p	Pulse duration of the step power expressed in s.
P_{Step}	Step power function applied to the die expressed in W.
$T_{j(tp)}$	Junction temperature over the time width, expressed in °C.
T_{Ref}	Temperature of the reference point expressed in °C.

Junction to ambient, $Z_{TH(j-a)}$ and junction to lead, $Z_{TH(j-l)}$ transient thermal impedance curves are provided in the datasheet. However $Z_{TH(j-l)}$ should be preferred to evaluate the peak junction temperature to get a better assessment.

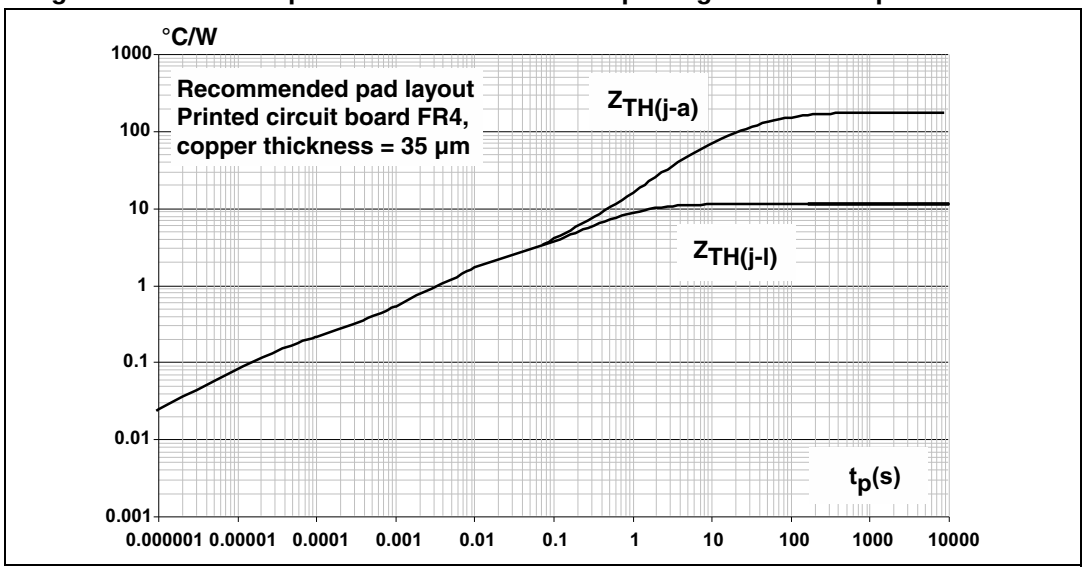
Thus from *Equation 8*, the dynamic change in temperature over the time can be determined using

Equation 9

$$T_j(t_p) = P_{Step} \cdot Z_{TH(j-l)}(t_p) + T_l$$

The transient thermal impedance diagram provides a quick and simple method to estimate the rise of junction temperature under transient conditions. *Figure 6* below illustrates transient thermal impedance diagrams of the SMB package. Note that thermal impedances increase until they reach their asymptotic limit corresponding to their thermal resistance $R_{th(j-l)}$ and $R_{th(j-a)}$.

Figure 6. Thermal impedance variation of SMB package versus the pulse duration



When the STRVS works under repetitive mode operation, the peak junction temperature T_{jpeak} must be below absolute rating T_{jmax} specified in the datasheet.

For an infinite pulse train case, T_{jpeak} is expressed as shown in *Equation 10*:

Equation 10

$$T_{j\,peak}(t_p) = P_D \cdot R_{TH(j-l)} + (P_{Step} - P_D) \cdot Z_{TH(j-l)}(t_p) + T_l$$

Note: The background average power P_D has been subtracted, to avoid counting this effect twice in calculating temperature rise.

In power conversion applications, two main cases occur. The time constants of the transient thermal impedance $\tau_{thermal}$ must be considered regarding the switching period t_{SW} in the application. *Figure 7* illustrates the impact of operating frequency on the ripple temperature.

The time constant of a thermal system is dependent on its transient thermal impedance curve. A sufficient estimation of thermal constant can be easily made from the simple RC thermal model representing the $Z_{th(j\text{-}Ref)}$ curve.

Equation 11

$$Z_{th(j\text{-}Ref)}(t) = R_{th(j\text{-}Ref)} \cdot (1 - e^{(-t/t_{au})})$$

Equation 12

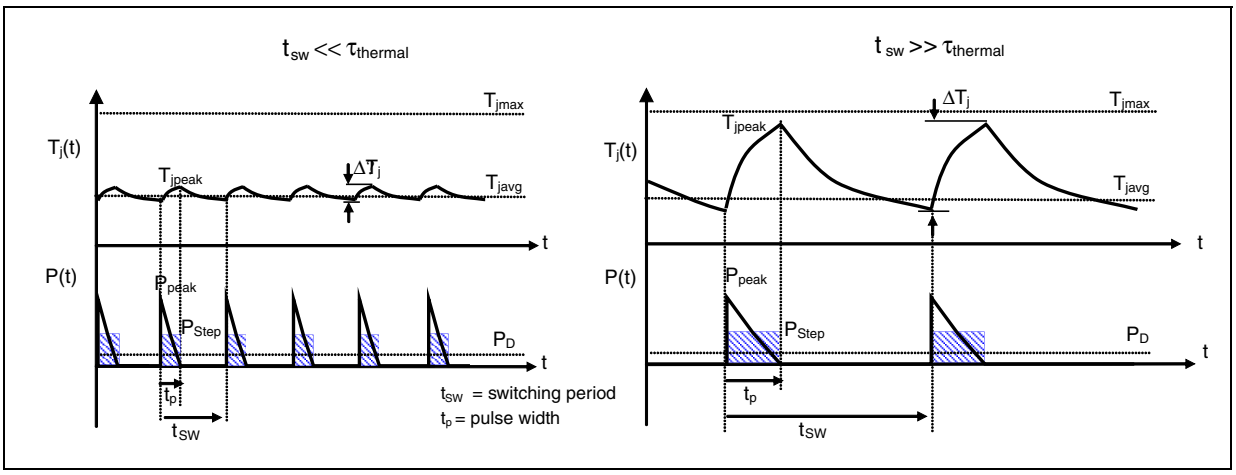
$$t_{au} = -t(\ln(1-Z_{th}(t)/R_{th})$$

Equation 12 applied to *Figure 6* for an application working switching period t_{sw}, around 10 µs, gives t_{au} much greater than t_{sw} due to the low value of $Z_{th(@\ 10\ \mu s)}$ before the R_{th} value. In this case the junction temperature rises and falls with a negligible dynamic temperature ΔT_j near T_{javg} as shown in *Figure 7*.

Since $T_{jpeak} \approx T_{javg}$, only the average junction temperature evaluation is needed using *Equation 6*. Notice that this case represents 90% of switch mode power supply applications (F_{SW} > 20 kHz). Under these conditions, pulse widths are generally in the range of some tens to hundreds of nanoseconds and pulses may be viewed as a short block of constant power P_{STEP}, sustaining the junction temperature.

When t_{SW} is not negligible regarding the $\tau_{thermal}$ of the device (*Figure 7*), average temperature verification is not enough to ensure that the junction temperature of the die remains within specifications. Consequently, the instantaneous peak junction temperature T_{jpeak} must be verified using *Equation 10*

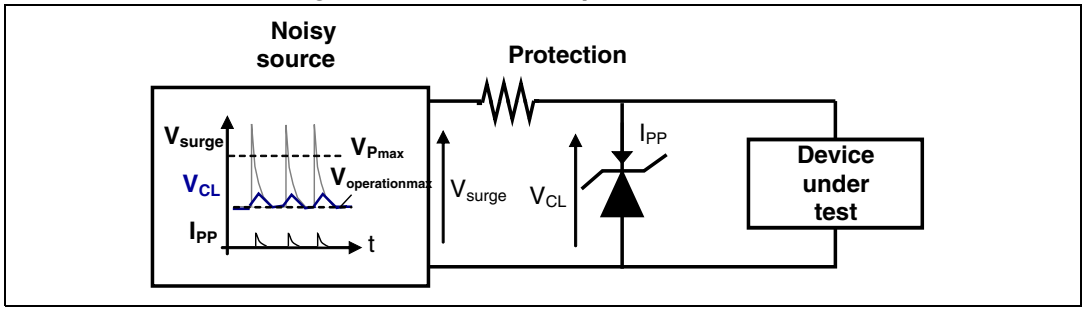
Figure 7. Switching frequency effect on the junction temperature variation in repetitive mode.



2 General design procedure

This section presents general design guidelines. *Figure 8* shows a simplified schematic where an STRVS device is inserted between the noisy source and the vulnerable device to protect it against repetitive transient surges.

Figure 8. Basic STRVS protection circuit



2.1 Key Rules

To ensure that absolute ratings are not exceeded, designers have to evaluate the worst case conditions in the application to select the suitable device. The three criteria shown in *Table 2* are required:

Table 2. Basic design criteria

Criteria		Application conditions	Device parameter
1	Be invisible under operating voltage (standby). Leakage current should have no effect on normal circuit performance	Maximum operating voltage, $V_{operationmax}$	Stand-off voltage $V_{operationmax} < V_{RM}$
2	Protect device against repetitive electrical overstress by instantly clamping spike voltages to a nondestructive level.	Voltage protection, V_{Pmax}	Clamping voltage V_{CLtyp} (I_{PPmax};125 °C) < V_{Pmax}
3	Maintain the junction temperature within specifications to guarantee a high reliability. This point must be obeyed in transient and steady state working mode.	Repetitive current, I_{PPmax}	Power dissipation, $T_j < T_{jmax}$

2.2 Transil selection process

This proposed methodology is based on a systematic approach to match the general case study. The device selection uses a recursive process. Steps are described below:

2.2.1 Step 1: STRVS preselection

In the absence of transient voltages, the STRVS should act as an open circuit and should have no effect on normal circuit performance (Criteria 1 in *Table 2*). The preselection begins with V_{RM} parameters where the leakage current will not exceed 1 µA @ 25 °C when $V_{operationmax}$ is applied. Then, all STRVS having a $V_{BR} > V_{Pmax}$ can be removed from consideration to ensure the circuit protection (Criteria 2 *Table 2*). Note that V_{Pmax} represents the admissible clamping voltage which includes a safety margin generally 15% below the absolute rating of the end-component to protect.

At this time, several STRVS may cover both criteria 1 and criteria 2. In the first pass using the highest rated voltage available is recommended. This generally minimizes the standby consumption and power dissipation.

The smallest package available is primarily chosen to optimize the solution from the thermal point of view with minimum loop numbers.

2.2.2 Step 2: Clamping voltage assessment

The designer has to check the clamping voltage $V_{CLtyp}(I_{PPmax};125°C)$ (Criteria 2 *Table 2*) by using curves provided in the datasheet. This point has to be verified in the worst case application and thus the current I_{PPmax} flowing though the device must be identified.

Under steady state operation, we recommend that designers should ensure that T_{jpeak} should not exceed 125 °C. This step requires a current measurement because the STRVS current is generally unknown. If so, it is recommended the designer starts the evaluation with the highest pre-selected rated voltage and with the biggest package available to avoid a thermal failure. When the peak current can be predicted or simulated, the clamping voltage can be directly calculated.

While the $V_{CLtyp}(I_{PPmax};125\ °C) > V_{Pmax}$ is true (Criteria 2 *Table 2*), the rated voltage is decreased by recursion until the lowest pre-selected STRVS can be identified at a cost of a higher power dissipation and quiescent current consumption.

2.2.3 Step 3: Dissipated power calculation

Power dissipation assessment is requested to evaluate the maximum and average junction temperature of the device. Power dissipation is performed with the V_{CLtyp} characteristic given at 125°C overestimating losses.

By using *Equation 6* and/or *Equation 10*, operating junction temperature of the device can be computed.

In case of $T_{jpeak} < 125°C$, the result corresponds to the smallest package solution compatible with design rules. Otherwise, the user should return to step 1 or 2 to go over the available electrical characteristics and package performances of the device. When dissipated power is too high, a second option is to use STRVS in serial configuration in order to spread the heat flow between packages.

2.2.4 Step 4: In-situ test

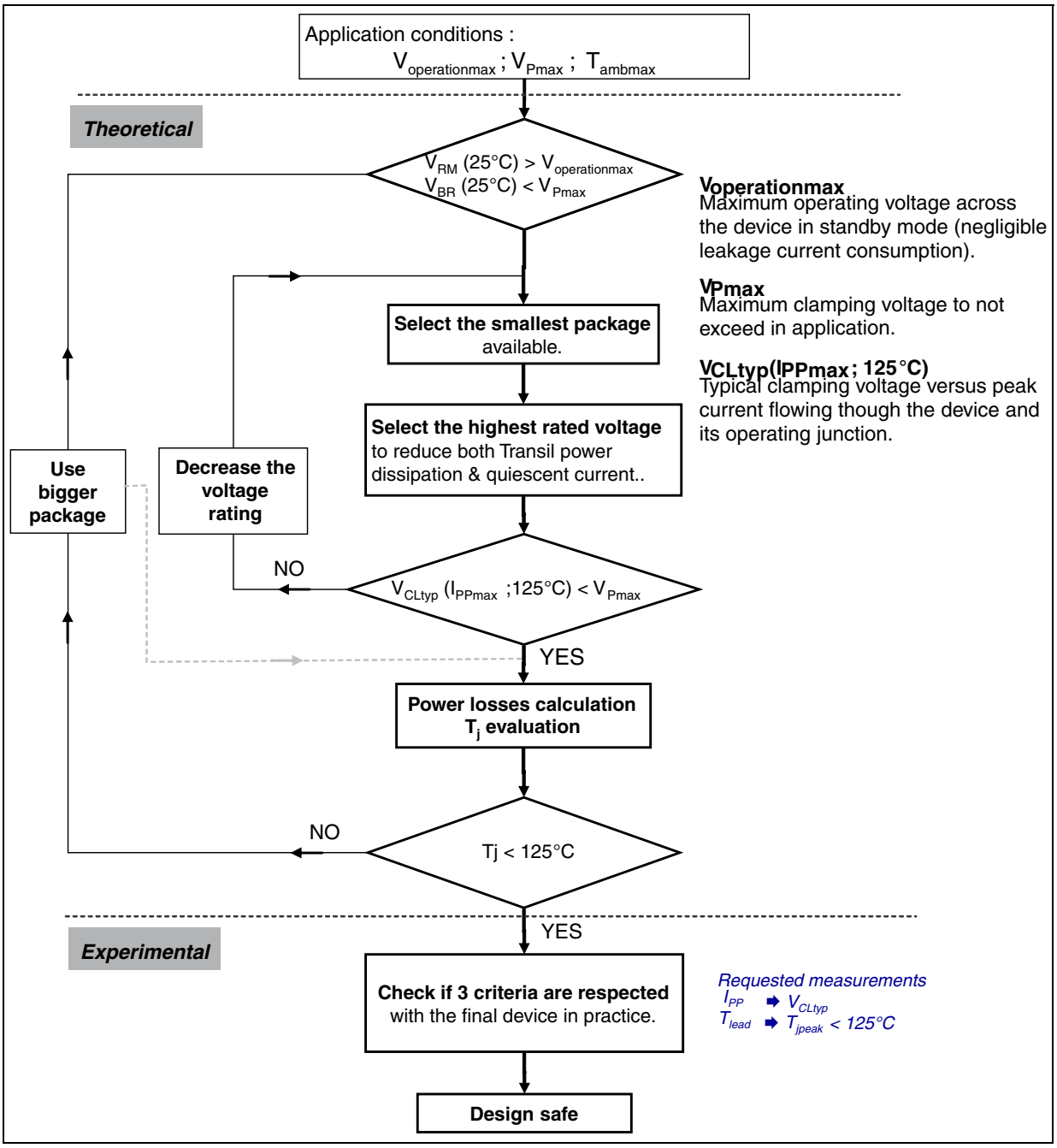
In the last step, we recommend checking the application to ensure that all criteria are respected with the final selected device.

This step requires a current waveform and lead temperature measurement to calculate the actual junction temperature and the clamping voltage.

2.3 Transil selection flowchart

Figure 9 summarizes the selection procedure:

Figure 9. Device selection process overview



3 Design example

The case study corresponds to protection of a MOSFET device. Because of stray inductance in series with the power switch STP50NF25, fast transient over voltages appear across it at each switching period. A STRVS device is therefore inserted in parallel to protect the switch.

Applications conditions are shown in *Table 3*:

Table 3. Worst case application conditions (maximum values)

$V_{operationmax}$	F_{SW}	I_{PP}	T_{ambmax}	V_{DSS}	Package
120 V	100 kHz	Unknown	50 °C	250 V	SMD

3.1 STRVS pre-selection

Considering a safety margin of 15% V_{Pmax} is given by *Equation 13*.

Equation 13

$$V_{Pmax} = V_{DSS} \cdot 0.85 = 212 \text{ V}$$

Considering the criteria 1 and 2, several STRVS can be pre-selected as shown in *Table 4*

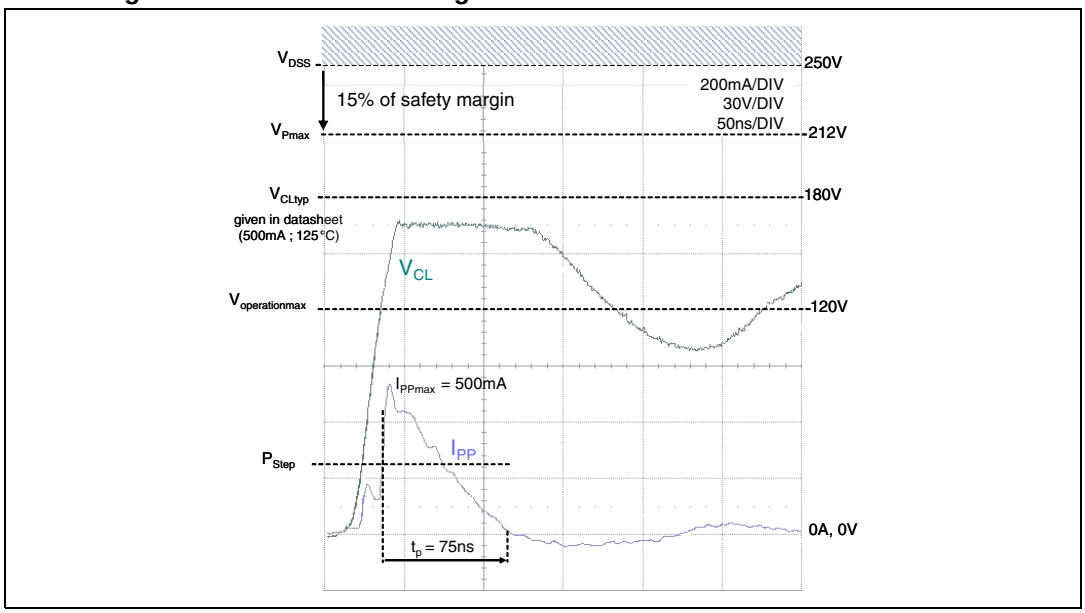
Table 4. Possible pre-selected devices

Order code	V_{RMmax} @ [1 µA, 25 °C]	V_{BRmax} @ [1 mA, 25 °C]	α_{Tmax} @ [1 mA]	Package
STRVS182X02F/C	128 V	158 V	$10.8 \cdot 10^{-4}$/°C	DO-201/SMC
STRVS185X02B/E	128 V	158 V	$10.8 \cdot 10^{-4}$/°C	SMB/DO-15
STRVS222X02F	154 V	189 V	$10.8 \cdot 10^{-4}$/°C	DO-201
STRVS225X02E	154 V	189 V	$10.8 \cdot 10^{-4}$/°C	DO-15

3.2 Clamping voltage assessment

Since the application requires a surface mount package (SMD) protection, STRVS185X02B is primarily selected. Based on the methodology, the current will be sensed in application with a DO-15 package to minimize the thermal issue. Current and voltage waveforms across the device are shown below during the clamping time.

Figure 10. Current and voltage waveforms across the STRVS185X02B.

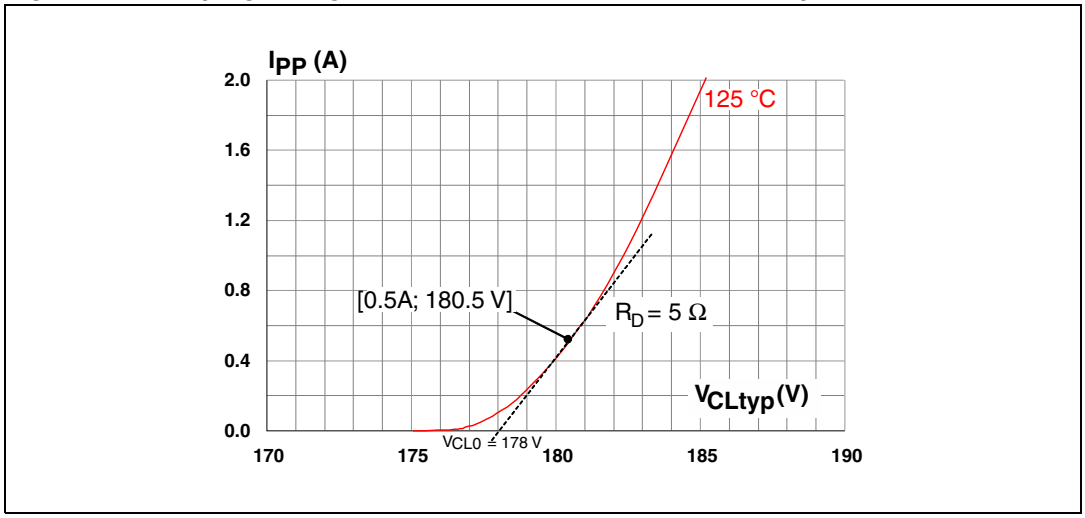


Let's verify with the current measurement and device features that:

V_{CLtyp}(500 mA;125°C) < V_{Pmax}.

From *Figure 11*,V_{CLtyp} (500 mA;125°C) ≈ 181 V

Figure 11. Clamping voltage characteristics of STRVS185X02B provided in datasheet.



Since V_{CLtyp} (500 mA;125°C) < V_{Pmax}, STRVS185X02B could be selected.

3.3 Dissipated power calculation

Let's verify that T_{jpeak} < 125 °C, and V_{CLtyp}(500 mA; T_{javg}) < V_{Pmax}.

3.3.1 Power losses calculation:

The curve is fitted in operating region to find R_D, V_{CL0} (see *Figure 11*):

From *Equation 4*, R_D equals:
$R_D(400mA;600mA;125°C) = R_D = 5\ \Omega$

From *Equation 5*, V_{CL0} is calculated as:
$V_{CL0}(400mA;600mA;125°C) = V_{CL0} = 178V$

The dissipated power during the clamping time is now calculated:

$$P_{Step} = \frac{1}{t_p}\int_0^{t_p} V_{CL}(t)\cdot I_{PP}(t)dt$$

$$P_{Step} = \frac{I_{PPmax}\cdot(3\cdot V_{CL0} + 2\cdot I_{PPmax}\cdot R_D)}{6}$$

$P_{Step} = 44.9\ W$

The average power dissipation P_D is calculated:
$P_D = t_p \cdot F_{SW} \cdot P_{step}$
$P_D = 0.34\ W$

3.3.2 Peak and average junction temperature calculation:

Considering the low ΔT_j, due to the low value of t_{SW}, before the thermal cst time $\tau_{thermal}$ of the device (see *Section 1.2.2*), the peak and average junction temperature are considered identical:

From *Equation 5*, T_{jpeak} equals:
$T_{j_{peak}} = R_{TH(j-a)} \cdot P_D + T_{ambmax}$
$T_{j_{peak}} = 112\ °C$

$V_{CLtyp}(I_{PPmax}; 112°C) < V_{CLtyp}(I_{PPmax}; 125°C) < V_{Pmax}$, STRVS185X02B is selected.

The power switch and STRVS should be both safe.

3.4 In-situ verification

The designer verifies all criteria with the final protection device.

Due to neighboring components sharing the same PCB layout in the system, T_{jpeak} can be estimated more accurately with thermal measurement done from the lead. *Table 5* presents measurements results obtained with STRVS.

Table 5. Sample measurements

I_{PPpeak}	t_p	T_j
600 mA	65 ns	116 °C

Using the measurements from *Table 5*:

$P_{Step} = 54\ W$

$P_D = 0.351\ W$

$T_{j\ peak} = R_{TH(j-l)} \cdot P_D + T_l = 121\ °C$

$V_{CLtyp}(I_{PPmax}; 121°C) < V_{CL}(I_{PPmax}; 125\ °C)$

The component matches the application requirements.

4 Conclusion

This application note has presented design guidelines for the new protection device family STRVS dedicated to the repetitive operation mode.

The design procedure proposed by STMicroelectronics serves as basis of a quick and efficient design process to offer better protection. Note that this methodology is flexible and can fit a wide range the application requirements (such as safety margin, allowable T_{jpeak} values…).

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
04-Mar-2013	1	Initial release.
05-Sep-2013	2	Updated *Figure 1*.

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