Introduction

The silicon transient voltage suppressor (TVS) device such as the Transil™ was initially specified with a power surge capability to respond to industrial standard test conditions, especially against high-energy single transient voltages. Today, many components in switched mode power supplies are continuously subjected to very short transient voltages. Little data is given in TVS specifications regarding the repetitive mode operation. Therefore, it is not easy for the designer to accurately assess the clamping voltage and power losses under these conditions.

This application note introduces the new repetitive voltage suppressor STRVSX features, specifically adapted to the repetitive mode operation. A design guideline is presented and selection processes are described.
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1 STRVS parameters

This section defines the electrical and thermal characteristics of the STRVS.

1.1 Electrical parameters

Figure 1 shows the typical reverse characteristic given at two temperatures of an STRVS device.

**Stand-off voltage (V_{RM})**

The stand-off voltage is specified for I = I_{RM} = 1 µA and T_j = 25 °C. Under these conditions, the device is still acting as an open circuit. This parameter is one of the key parameters in circuit protection.

**Breakdown voltage (V_{BR})**

The breakdown voltage corresponds to the voltage from which the STRVS starts to go into the avalanche region. This parameter is specified for I = I_{BR} = 1 mA and T_j = 25 °C. The V_{BR} parameter follows a linear variation with junction temperature as shown in Equation 1.

**Equation 1**

\[ V_{BR}(T_j) = V_{BR}(T_{REF}) \cdot \left(1 + \alpha_T \cdot (T_j - T_{REF})\right) \]

Where T_{REF} = reference temperature expressed in °C, generally given at 25 °C and \( \alpha_T \) = temperature coefficient in 1/°C.
Clamping voltage ($V_{CL}$)

The clamping voltage is the total voltage across the STRVS over the peak pulse current $I_{PP}$ at a given temperature. A range of typical values provides the characteristics of the clamping voltage for given values of peak current ($I_{PP}$), and three controlled junction temperatures: 25 °C, 85 °C and 125 °C. All curves start from $V_{CL}(1 \text{ mA}) = V_{BR_{max}}$. Figure 2 illustrates $V_{CL}$ curves of an STRVS185X02B. These curves are useful for verifying the suitability of the allowable clamping voltage in application.

Figure 2. Clamping voltage characteristic over temperatures of an STRVS185X02B

1.1.1 Simplified electrical model

A linear model can be employed to approximate the $V_{CL} = f(I_{PP})$ characteristics of the STRVS. A straight line is used to approximate the actual curve inside the working area imposed by the application conditions (see Figure 3). The line intersects the horizontal axis at the voltage $V_{CLO}$. The slope of the line is inversely proportional to the dynamic resistance $R_D$. The equivalent circuit that models this equation is shown in Figure 4.
A simple rule to calculate $R_D$ and $V_{CL0}$ is to use $I_{PP2} = I_{peak}$ of the application and $I_{PP1} = I_{PP2} / 2$.

The clamping voltage is defined in Equation 2.

**Equation 2**

$$V_{CL}(I_{PP};T_j) = V_{CL0}(I_{PP};I_{PP2};T_j) + R_D(I_{PP};I_{PP2};T_j) \cdot I_{PP}$$
R_D can be calculated as shown in Equation 3.

**Equation 3**
\[ R_D(I_{PPN}, I_{PP2}, T_j) = \frac{V_{CL2}(I_{PP2}, T_j) - V_{CL1}(I_{PP1}, T_j)}{I_{PP2} - I_{PP1}} \]

V_{CL0} is shown in **Equation 4**

**Equation 4**
\[ V_{CL2}(I_{PP1}, I_{PP2}, T_j) = V_{CL1}(I_{PP1}, T_j) - R_D(I_{PP1}, I_{PP2}, T_j) \cdot I_{PP2} \]

This model will be useful to assess the power dissipation of the device.

1.2 Thermal parameters

1.2.1 Steady state parameters

**Thermal resistance (R_{th(j-Ref)})**

The thermal resistance represents the package’s dissipation capability from the junction (active die surface) to a specified reference point (case, lead, board, ambient, etc…). Its value is defined as the temperature difference between two specified points, divided by the dissipated power under thermal equilibrium conditions.

**Equation 5**
\[ R_{th(j-Ref)} = \frac{T_j - T_{Ref}}{P_D} \]

Where:
- \( R_{th(j-Ref)} \): Junction-to-reference thermal resistance expressed in °C/W
- \( P_D \): Average dissipated power of the die, expressed in W
- \( T_j \): Junction temperature of the die expressed in °C
- \( T_{Ref} \): Temperature of the reference point expressed in °C

The previous equation can be easily reworked to estimate the junction temperature in steady mode operation as shown in **Equation 6**.

**Equation 6**
\[ T_j = R_{th(j-Ref)} \cdot P_D + T_{Ref} \]

In STRVSX specifications, the junction-to-lead (R_{th(j-l)}) and junction-to-ambient (R_{th(j-a)}) thermal resistances are commonly provided to help designers. These parameters are determined under standard test conditions with specific board dimensions and layers in compliance with the JEDEC standard.

*Table 1* shows typical thermal resistances for available packages.
Junction-to-ambient thermal resistance ($R_{th(j-a)}$)

The thermal resistance $R_{th(j-a)}$ is the heat dissipation capability from the junction surface of the die to the ambient, via all paths. Its value is strongly dependent on the type of board, the copper plane underneath the device, the neighboring components interacting through the PCB, and the mounting and cooling methods (free or forced airflow).

Actual performance of the product in real applications may be different. Values provided in datasheet are typical values and should be used with some measure of caution. It is useful for comparing the thermal performance of one package to another as shown in Table 1.

Therefore, this information may be used for the first pass of junction temperature calculation. The thermal resistance $R_{th(j-a)}$ value with minimum footprint is recommended when the user starts a design calculation. Figure 5 shows the $R_{th(j-a)}$ dependency of a SMB package over copper plane area.

![Figure 5. Junction-to-ambient thermal resistance over copper plane area of SMB package](image)

<table>
<thead>
<tr>
<th>Thermal resistance</th>
<th>Package</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-lead, $R_{th(j-l)}$</td>
<td>DO-15, 35</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-ambient $R_{th(j-a)}$</td>
<td>DO-201, 100</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>SMB, 185</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SMC, 150</td>
<td></td>
</tr>
</tbody>
</table>

Junction-to-lead thermal resistance ($R_{th(j-l)}$)

The thermal resistance $R_{th(j-l)}$ is the heat dissipation capability from the junction surface of the die to the package lead. This parameter is useful for estimating the junction temperature from a measurement of the lead temperature. The designer can determine the lead temperature of the device under application conditions with a fine gauge thermocouple or
infrared camera and calculate the junction temperature using *Equation 6*. The lead is the most interesting reference point to evaluate accurately the average operating junction temperature $T_{j,avg}$. The thermal resistance value $R_{th(j-l)}$ depends only on the package properties unlike $R_{th(j-a)}$.

### 1.2.2 Transient parameter

**Transient thermal impedance ($Z_{TH(j-Ref)}(t_p)$)**

The transient thermal impedance $Z_{TH(j-Ref)}(t_p)$ is the temporary variation of thermal resistance from an input power step function up to reaching a stable value as defined *Equation 7*.

**Equation 7**  
\[
\lim_{t_p \to \infty} Z_{th(j-Ref)}(t_p) = R_{th(j-Ref)}
\]

Transient thermal impedance can be calculated using *Equation 8*.

**Equation 8**  
\[
Z_{th(j-Ref)}(t_p) = \frac{T_j(t_p) - T_{Ref}}{P_{Step}}
\]

Where:
- $Z_{TH(j-Ref)}$: Junction to reference transient thermal impedance expressed in °C/W.
- $t_p$: Pulse duration of the step power expressed in s.
- $P_{Step}$: Step power function applied to the die expressed in W.
- $T_j(t_p)$: Junction temperature over the time width, expressed in °C.
- $T_{Ref}$: Temperature of the reference point expressed in °C.

Junction to ambient, $Z_{TH(j-a)}$ and junction to lead, $Z_{TH(j-l)}$ transient thermal impedance curves are provided in the datasheet. However $Z_{TH(j-l)}$ should be preferred to evaluate the peak junction temperature to get a better assessment.

Thus from *Equation 8*, the dynamic change in temperature over the time can be determined using

**Equation 9**  
\[
T_j(t_p) = P_{Step} \cdot Z_{th(j-l)}(t_p) + T_j
\]

The transient thermal impedance diagram provides a quick and simple method to estimate the rise of junction temperature under transient conditions. *Figure 6* below illustrates transient thermal impedance diagrams of the SMB package. Note that thermal impedances increase until they reach their asymptotic limit corresponding to their thermal resistance $R_{th(j-l)}$ and $R_{th(j-a)}$. 
When the STRVS works under repetitive mode operation, the peak junction temperature $T_{j(\text{peak})}$ must be below absolute rating $T_{j(\text{max})}$ specified in the datasheet.

For an infinite pulse train case, $T_{j(\text{peak})}$ is expressed as shown in Equation 10:

\[
T_{j(\text{peak})}(t_p) = P_D \cdot R_{th(j-a)} + (P_{SW(j-a)} \cdot Z_{th(j-a)}(t_p)) + T_J
\]

**Note:** The background average power $P_D$ has been subtracted, to avoid counting this effect twice in calculating temperature rise.

In power conversion applications, two main cases occur. The time constants of the transient thermal impedance $\tau_{\text{thermal}}$ must be considered regarding the switching period $t_{SW}$ in the application. Figure 7 illustrates the impact of operating frequency on the ripple temperature.

The time constant of a thermal system is dependent on its transient thermal impedance curve. A sufficient estimation of thermal constant can be easily made from the simple RC thermal model representing the $Z_{th(j-\text{Ref})}$ curve.

**Equation 11**

\[
Z_{th(j-\text{Ref})}(t) = R_{th(j-\text{Ref})} \cdot (1 - e^{-t/\tau_{\text{a}}})
\]

**Equation 12**

\[
t_{\text{a}} = -t(\ln(1-Z_{th}(t))/R_{th})
\]

**Equation 12** applied to Figure 6 for an application working switching period $t_{SW}$ around 10 $\mu$s, gives $t_{\text{a}}$ much greater than $t_{SW}$ due to the low value of $Z_{th}(10 \mu$s) before the $R_{th}$ value. In this case the junction temperature rises and falls with a negligible dynamic temperature $\Delta T_J$ near $T_{j(\text{avg})}$ as shown in Figure 7.

Since $T_{j(\text{peak})} = T_{j(\text{avg})}$, only the average junction temperature evaluation is needed using **Equation 6**. Notice that this case represents 90% of switch mode power supply applications ($F_{SW} > 20$ kHz). Under these conditions, pulse widths are generally in the range of some tens to hundreds of nanoseconds and pulses may be viewed as a short block of constant power $P_{\text{STEP}}$ sustaining the junction temperature.
When $t_{SW}$ is not negligible regarding the $\tau_{thermal}$ of the device (*Figure 7*), average temperature verification is not enough to ensure that the junction temperature of the die remains within specifications. Consequently, the instantaneous peak junction temperature $T_{jpeak}$ must be verified using *Equation 10*.

*Figure 7. Switching frequency effect on the junction temperature variation in repetitive mode.*
2 General design procedure

This section presents general design guidelines. Figure 8 shows a simplified schematic where an STRVS device is inserted between the noisy source and the vulnerable device to protect it against repetitive transient surges.

Figure 8. Basic STRVS protection circuit

2.1 Key Rules

To ensure that absolute ratings are not exceeded, designers have to evaluate the worst case conditions in the application to select the suitable device. The three criteria shown in Table 2 are required:

Table 2. Basic design criteria

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Application conditions</th>
<th>Device parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Be invisible under operating voltage (standby). Leakage current should have no effect on normal circuit performance</td>
<td>Maximum operating voltage, ( V_{\text{operation max}} )</td>
</tr>
<tr>
<td>2</td>
<td>Protect device against repetitive electrical overstress by instantly clamping spike voltages to a nondestructive level.</td>
<td>Voltage protection, ( V_{\text{Pmax}} )</td>
</tr>
<tr>
<td>3</td>
<td>Maintain the junction temperature within specifications to guarantee a high reliability. This point must be obeyed in transient and steady state working mode.</td>
<td>Repetitive current, ( I_{\text{PP max}} )</td>
</tr>
</tbody>
</table>

2.2 Transil selection process

This proposed methodology is based on a systematic approach to match the general case study. The device selection uses a recursive process. Steps are described below:
2.2.1 Step 1: STRVS preselection

In the absence of transient voltages, the STRVS should act as an open circuit and should have no effect on normal circuit performance (Criteria 1 in Table 2). The preselection begins with $V_{RM}$ parameters where the leakage current will not exceed 1 µA @ 25 °C when $V_{operation_{max}}$ is applied. Then, all STRVS having a $V_{BR} > V_{P_{max}}$ can be removed from consideration to ensure the circuit protection (Criteria 2 Table 2). Note that $V_{P_{max}}$ represents the admissible clamping voltage which includes a safety margin generally 15% below the absolute rating of the end-component to protect.

At this time, several STRVS may cover both criteria 1 and criteria 2. In the first pass using the highest rated voltage available is recommended. This generally minimizes the standby consumption and power dissipation.

The smallest package available is primarily chosen to optimize the solution from the thermal point of view with minimum loop numbers.

2.2.2 Step 2: Clamping voltage assessment

The designer has to check the clamping voltage $V_{CL_{typ}}(I_{PP_{max}};125°C)$ (Criteria 2 Table 2) by using curves provided in the datasheet. This point has to be verified in the worst case application and thus the current $I_{PP_{max}}$ flowing through the device must be identified.

Under steady state operation, we recommend that designers should ensure that $T_{j_{peak}}$ should not exceed 125 °C. This step requires a current measurement because the STRVS current is generally unknown. If so, it is recommended the designer starts the evaluation with the highest pre-selected rated voltage and with the biggest package available to avoid a thermal failure. When the peak current can be predicted or simulated, the clamping voltage can be directly calculated.

While the $V_{CL_{typ}}(I_{PP_{max}};125°C) > V_{P_{max}}$ is true (Criteria 2 Table 2), the rated voltage is decreased by recursion until the lowest pre-selected STRVS can be identified at a cost of a higher power dissipation and quiescent current consumption.

2.2.3 Step 3: Dissipated power calculation

Power dissipation assessment is requested to evaluate the maximum and average junction temperature of the device. Power dissipation is performed with the $V_{CL_{typ}}$ characteristic given at 125°C overestimating losses.

By using Equation 6 and/or Equation 10, operating junction temperature of the device can be computed.

In case of $T_{j_{peak}} < 125°C$, the result corresponds to the smallest package solution compatible with design rules. Otherwise, the user should return to step 1 or 2 to go over the available electrical characteristics and package performances of the device. When dissipated power is too high, a second option is to use STRVS in serial configuration in order to spread the heat flow between packages.

2.2.4 Step 4: In-situ test

In the last step, we recommend checking the application to ensure that all criteria are respected with the final selected device.

This step requires a current waveform and lead temperature measurement to calculate the actual junction temperature and the clamping voltage.
2.3 Transil selection flowchart

Figure 9 summarizes the selection procedure:

**Figure 9. Device selection process overview**

- **Application conditions:**
  \[ V_{\text{operation max}} ; V_{\text{P max}} ; T_{\text{amb max}} \]

- **Theoretical**
  - \( V_{\text{RM (25°C)}} > V_{\text{operation max}} \)
  - \( V_{\text{EM (25°C)}} < V_{\text{P max}} \)
  - Select the smallest package available.
  - Select the highest rated voltage to reduce both Transil power dissipation & quiescent current.
  - Decrease the voltage rating
  - \( V_{\text{CLP (IPP max ; 125°C)}} < V_{\text{P max}} \)
  - Power losses calculation
    - \( T_{\text{j evaluation}} \)
  - \( T_{\text{j}} < 125°C \)

- **Experimental**
  - Check if 3 criteria are respected with the final device in practice.
  - Design safe

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**Requested measurements**

\[ I_{\text{P max}} \Leftrightarrow V_{\text{CLP}} \]

\[ T_{\text{lead}} \Leftrightarrow T_{\text{ground}} < 125°C \]
3 Design example

The case study corresponds to protection of a MOSFET device. Because of stray inductance in series with the power switch STP50NF25, fast transient over voltages appear across it at each switching period. A STRVS device is therefore inserted in parallel to protect the switch.

Applications conditions are shown in Table 3:

<table>
<thead>
<tr>
<th>$V_{\text{operation max}}$</th>
<th>$F_{\text{SW}}$</th>
<th>$I_{\text{PP}}$</th>
<th>$T_{\text{amb max}}$</th>
<th>$V_{\text{DS}}$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>120 V</td>
<td>100 kHz</td>
<td>Unknown</td>
<td>50 °C</td>
<td>250 V</td>
<td>SMD</td>
</tr>
</tbody>
</table>

3.1 STRVS pre-selection

Considering a safety margin of 15% $V_{\text{Pmax}}$ is given by Equation 13.

Equation 13

$V_{\text{Pmax}} = V_{\text{DS}} \cdot 0.85 = 212 \text{ V}$

Considering the criteria 1 and 2, several STRVS can be pre-selected as shown in Table 4

<table>
<thead>
<tr>
<th>Order code</th>
<th>$V_{\text{R max}} @ [1 \mu A, 25 \text{ °C}]$</th>
<th>$V_{\text{B max}} @ [1 \text{ mA, 25 \text{ °C}]$</th>
<th>$\alpha_{\text{T max}} @ [1 \text{ mA}]$</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>STRVS182X02F/C</td>
<td>128 V</td>
<td>158 V</td>
<td>$10.8 \cdot 10^{-4} \text{/°C}$</td>
<td>DO-201/SMC</td>
</tr>
<tr>
<td>STRVS185X02B/E</td>
<td>128 V</td>
<td>158 V</td>
<td>$10.8 \cdot 10^{-4} \text{/°C}$</td>
<td>SMB/DO-15</td>
</tr>
<tr>
<td>STRVS222X02F</td>
<td>154 V</td>
<td>189 V</td>
<td>$10.8 \cdot 10^{-4} \text{/°C}$</td>
<td>DO-201</td>
</tr>
<tr>
<td>STRVS225X02E</td>
<td>154 V</td>
<td>189 V</td>
<td>$10.8 \cdot 10^{-4} \text{/°C}$</td>
<td>DO-15</td>
</tr>
</tbody>
</table>

3.2 Clamping voltage assessment

Since the application requires a surface mount package (SMD) protection, STRVS185X02B is primarily selected. Based on the methodology, the current will be sensed in application with a DO-15 package to minimize the thermal issue. Current and voltage waveforms across the device are shown below during the clamping time.
Let’s verify with the current measurement and device features that:
\[ V_{\text{CLtyp}}(500 \text{ mA};125^\circ \text{C}) < V_{\text{Pmax}}. \]
From Figure 11, \( V_{\text{CLtyp}}(500 \text{ mA};125^\circ \text{C}) \approx 181 \text{ V} \)

Since \( V_{\text{CLtyp}}(500 \text{ mA};125^\circ \text{C}) < V_{\text{Pmax}} \), STRVS185X02B could be selected.
3.3 Dissipated power calculation

Let’s verify that $T_{\text{peak}} < 125^\circ\text{C}$, and $V_{\text{CL typ}}(500\text{ mA}; T_{\text{avg}}) < V_{\text{Pmax}}$.

3.3.1 Power losses calculation:

The curve is fitted in operating region to find $R_D$, $V_{\text{CL 0}}$ (see Figure 11):

From Equation 4, $R_D$ equals:

$$R_D = \frac{V_{\text{CL 0}}}{I_{\text{P max}} \cdot \frac{V_{\text{CL typ}}}{I_{\text{P max}}}} = R_b = 5\ \Omega$$

From Equation 5, $V_{\text{CL 0}}$ is calculated as:

$$V_{\text{CL 0}}(400\text{ mA}; 600\text{ mA}; 125^\circ\text{C}) = V_{\text{CL 0}} = 178\text{V}$$

The dissipated power during the clamping time is now calculated:

$$P_{\text{diss}} = \int_{t_p}^{t_p} V_{\text{CL}}(t) \cdot I_{\text{P}}(t) \, dt$$

$$P_{\text{diss}} = \frac{I_{\text{P max}} \cdot 3 \cdot V_{\text{CL 0}} + 2 \cdot I_{\text{P max}} \cdot R_b}{6}$$

$$P_{\text{diss}} = 44.9\ \text{W}$$

The average power dissipation $P_D$ is calculated:

$$P_D = t_p \cdot F_{\text{SW}} \cdot P_{\text{sw}}$$

$$P_D = 0.34\ \text{W}$$

3.3.2 Peak and average junction temperature calculation:

Considering the low $\Delta T_j$, due to the low value of $t_{\text{sw}}$ before the thermal cst time $t_{\text{thermal}}$ of the device (see Section 1.2.2), the peak and average junction temperature are considered identical:

From Equation 5, $T_{\text{peak}}$ equals:

$$T_{\text{peak}} = R_{\text{TH(j-amb)}} \cdot P_D + T_{\text{amb(max)}}$$

$$T_{\text{peak}} = 112^\circ\text{C}$$

$V_{\text{CL typ}}(I_{\text{P max}}; 112^\circ\text{C}) < V_{\text{CL typ}}(I_{\text{P max}}; 125^\circ\text{C}) < V_{\text{P max}}$, STRVS185X02B is selected.

The power switch and STRVS should be both safe.

3.4 In-situ verification

The designer verifies all criteria with the final protection device.

Due to neighboring components sharing the same PCB layout in the system, $T_{\text{peak}}$ can be estimated more accurately with thermal measurement done from the lead. Table 5 presents measurements results obtained with STRVS.

<table>
<thead>
<tr>
<th>$I_{\text{P peak}}$</th>
<th>$t_p$</th>
<th>$T_j$</th>
</tr>
</thead>
<tbody>
<tr>
<td>600 mA</td>
<td>65 ns</td>
<td>116 °C</td>
</tr>
</tbody>
</table>
Using the measurements from Table 5:
\[ P_{\text{meas}} = 54 \text{ W} \]
\[ P_{D} = 0.351 \text{ W} \]
\[ T_{\text{peak}} = R_{\text{TJ}} \cdot I_{\text{D}} + P_{D} + T_{J} = 121 \degree \text{C} \]
\[ V_{\text{CLIP}}(I_{\text{Pmax}}, 121 \degree \text{C}) < V_{\text{CL}}(I_{\text{Pmax}}, 125 \degree \text{C}) \]

The component matches the application requirements.

### 4 Conclusion

This application note has presented design guidelines for the new protection device family STRVS dedicated to the repetitive operation mode.

The design procedure proposed by STMicroelectronics serves as basis of a quick and efficient design process to offer better protection. Note that this methodology is flexible and can fit a wide range the application requirements (such as safety margin, allowable \( T_{\text{peak}} \) values...).
5 Revision history

Table 6. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>04-Mar-2013</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>05-Sep-2013</td>
<td>2</td>
<td>Updated Figure 1.</td>
</tr>
</tbody>
</table>
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