

Power-fail comparator for NVRAM supervisory devices

Introduction

Dealing with unexpected power loss

Inadvertent or unexpected loss of power can cause a number of system level problems. Memory loss, uncontrolled program status and indeterminate processor state are just a few of the issues which can occur during catastrophic power failure. Power-fail recovery is critical for applications created to perform machine control or instrumentation monitoring, therefore knowing the state of the operating system at the time of power loss is very important.

The function of the power-fail comparator is to provide several milliseconds of early warning that power is failing. This advance warning (see [Figure 1: "Power-fail warning"](#)) will allow a system to perform operations necessary to prepare for a controlled shutdown sequence. By using a special power-fail input (PFI) to monitor the unregulated supply voltage, a power fail output ($\overline{\text{PFO}}$) can be generated t_{PFD} after the supply falls below the power-fail threshold (V_{PFI}). This is made possible by the ability of a power supply to continue to function and to provide output power for a period of time after the input power to the power supply has failed. This facility enables the power supply to ride through missing half cycles or missing cycles in an AC supply ([Figure 2: "Supply hold-up"](#)).

Figure 1: Power-fail warning

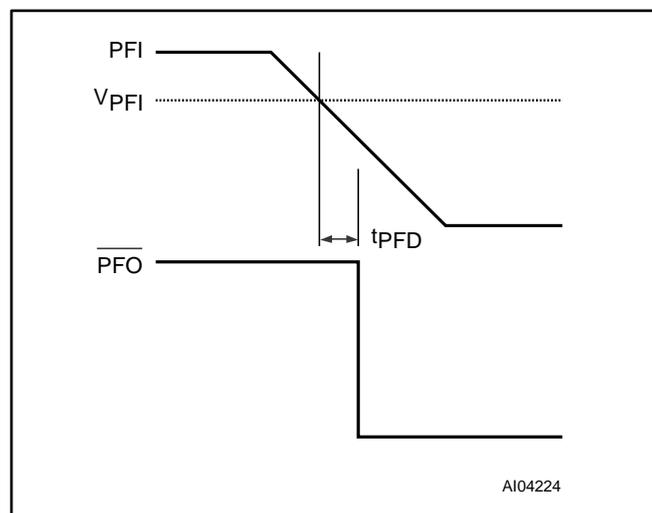
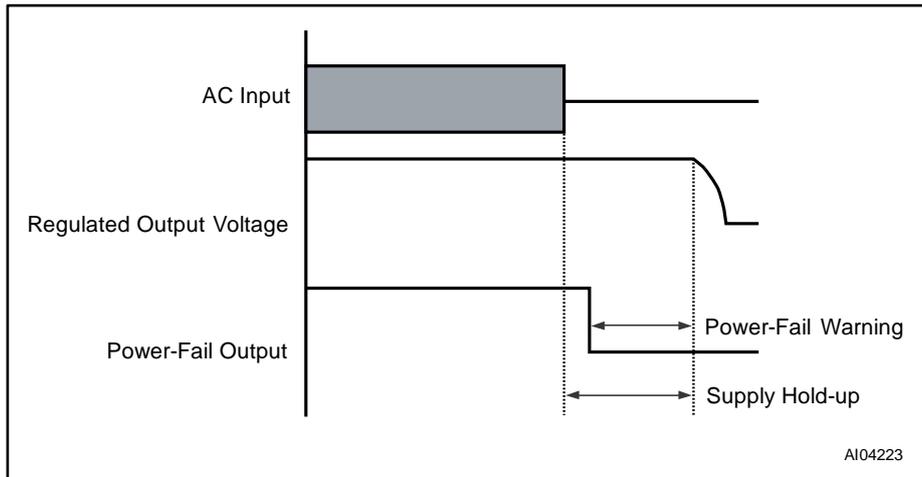
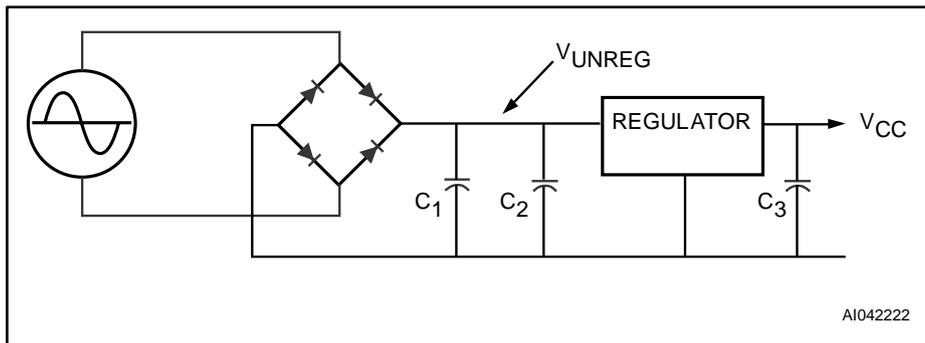


Figure 2: Supply hold-up



This is a result of the RC time constant inherent to most power supplies (see [Figure 3: "Typical power supply"](#)). This time constant is dominated by capacitors C_1 and C_3 (C_2 is usually quite small). C_1 will affect the V_{UNREG} slew rate during power-fail, while C_3 and C_1 will more directly affect the regulated V_{CC} slew rate. Thus when the AC input fails, this capacitance will continue to power the circuit for several milliseconds, typically in the order of 10 ms or more.

Figure 3: Typical power supply



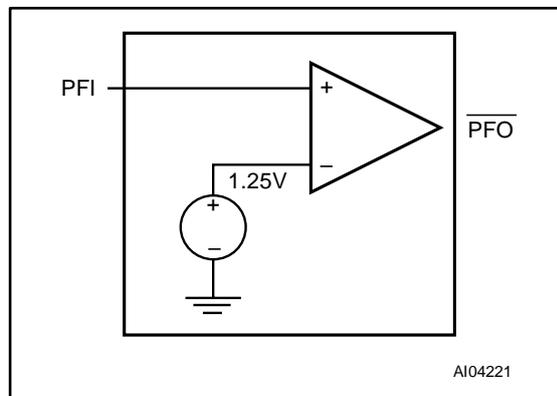
1 Functional description

An independent bandgap reference comparator is used to monitor the unregulated supply voltage by connecting this supply to the power-fail input pin. The RC time constant of the typical power supply will provide several milliseconds of operating voltage before decaying below a usable value. The power-fail input is constantly compared with an internal voltage reference of 1.25 V (see [Figure 4: "Power-fail comparator circuit"](#)). If the input voltage falls below 1.25 V, the power-fail output goes low. When it later goes above 1.25 V, the output returns high.

Adding two external resistors (see [Figure 5: "PFI/PFO in a typical system"](#)) as a voltage divider circuit allows the comparator to supervise any voltage above 1.25 V. The formula to calculate the trip point voltage of PFI (V_{PFI}), which is dependent upon R1 and R2 is:

$$V_{TRIP} = V_{PFI} \frac{(R1 + R2)}{R2} \quad \text{where } V_{PFI} = 1.25 \text{ V}$$

Figure 4: Power-fail comparator circuit



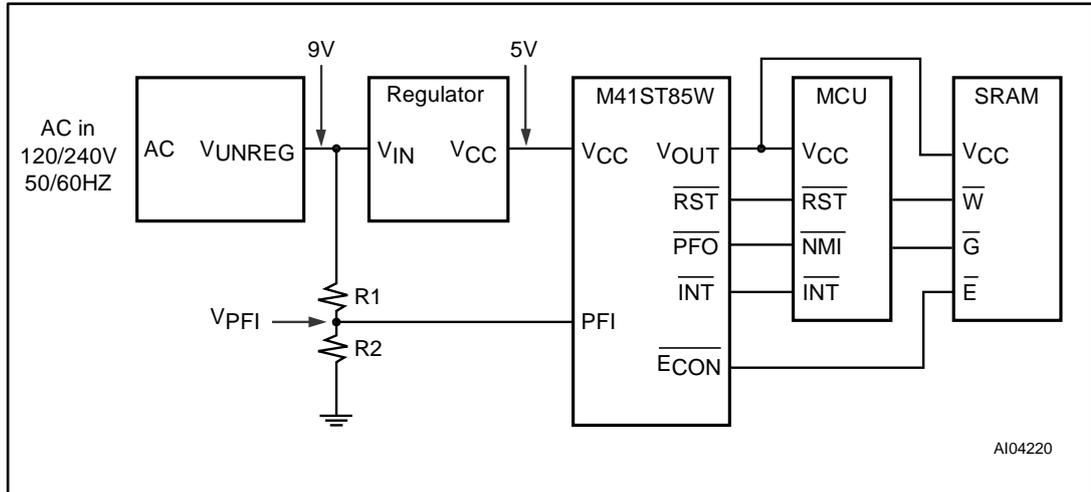
The sum of both resistors should be about 1 Mohm to minimize power consumption and to ensure the current in the PFI pin can be neglected compared with the current through the resistor network. The suggested resistor values are shown below (see [Table 1: "Look-up table for different trip points"](#)). The tolerance of the resistors should not exceed 1% to ensure the sensed voltage does not vary too much.

Table 1: Look-up table for different trip points

R1 (kOhms)	R2 (kOhms)	Vtrip (V)
750	130	8.5
910	130	10.0
820	100	11.5
820	91	12.5
1100	100	15.0

2 PFI/PFO operation in a system (how does it work?)

Figure 5: PFI/PFO in a typical system

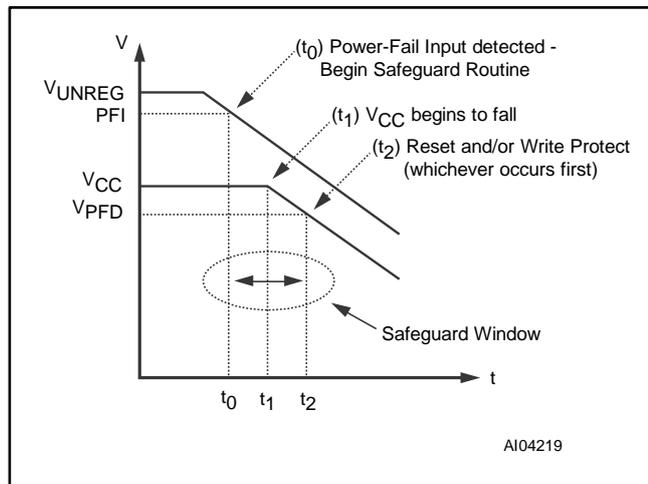


A typical power failure can be described by the following three events (see [Figure 6: "Power failure sequence"](#)):

1. PFI triggered (t_0): As V_{UNREG} falls below the V_{PFI} threshold, \overline{PFO} is asserted on the MCU's Non-Maskable Interrupt (NMI) pin. When NMI is asserted, the MCU halts its current task and begins saving critical data to the NVRAM (safeguard routine).
2. V_{CC} begins to fall (t_1): the MCU will continue functioning until the safeguard routine is complete or \overline{RESET} occurs.
3. \overline{RESET} asserted and/or Write Protect occurs (t_2):

At this point, the MCU needs to have completed the safeguard routine. This results in a safeguard window from PFI to \overline{RESET} /Write Protect ($t_2 - t_0$).

Figure 6: Power failure sequence



This safeguard window can be used for a number of purposes, depending on the application:

Power save

The MCU can switch off, one by one, all non-critical peripheral components to conserve energy for safeguard routines.

Data transfer

The MCU may transfer data from the scratch pad memory to the non-volatile memory. It takes only a few MCU cycles if using NVRAM, but can take several milliseconds when this data needs to be stored in an EEPROM or Flash memory.

Scratch pad RAM overwrite

Many applications are now required to run encode/decode algorithms (e.g. DES or RCA) for higher security.

Therefore it is sometimes preferable to overwrite the working space before power-down to prevent the contents of the RAM from being read illegitimately.

3 Advantages over traditional power monitoring

Typical power monitoring (or supervisory) devices offer features such as brown-out detect by monitoring the voltage at the V_{CC} pin, then asserting a RESET output when V_{CC} drops below a minimum level. Some may also include chip-enable gating or chip-enable write protection which will disable access to the memory, thereby protecting the SRAM contents from errant writes by an MCU that is operating in an undervoltage condition. These are good features and necessary to avoid catastrophic data loss, but unfortunately do not occur early enough to allow the MCU to gracefully enter a fail-safe state. Any of the following scenarios will result in unsatisfactory system shutdown:

Loss of processor state

When the RESET occurs, any information not already stored to the NVRAM will be lost. This includes the processor state, the program status, and any information still in the scratch pad RAM, but not in the NVRAM.

RESET occurs during a write cycle

If the MCU is writing to memory when RESET occurs, that data will most likely be corrupted. This applies to EEPROM and Flash memories as well as NVRAM.

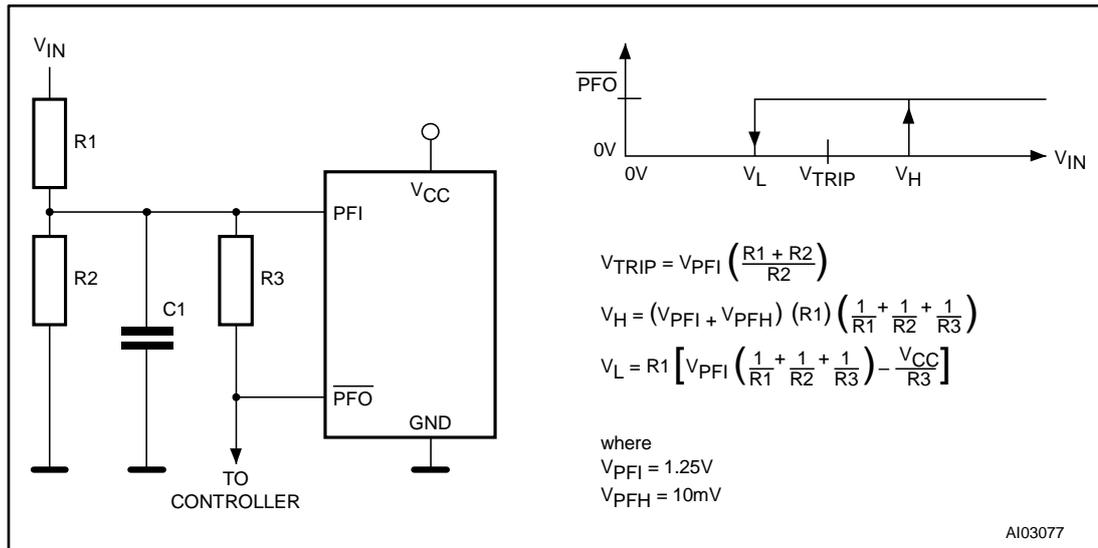
Write protect occurs before RESET

If the NVRAM gates off access to the SRAM prior to processor RESET, the processor may continue accessing/writing the NVRAM expecting that the data written is secure (when it has in fact, been lost).

4 Hysteresis

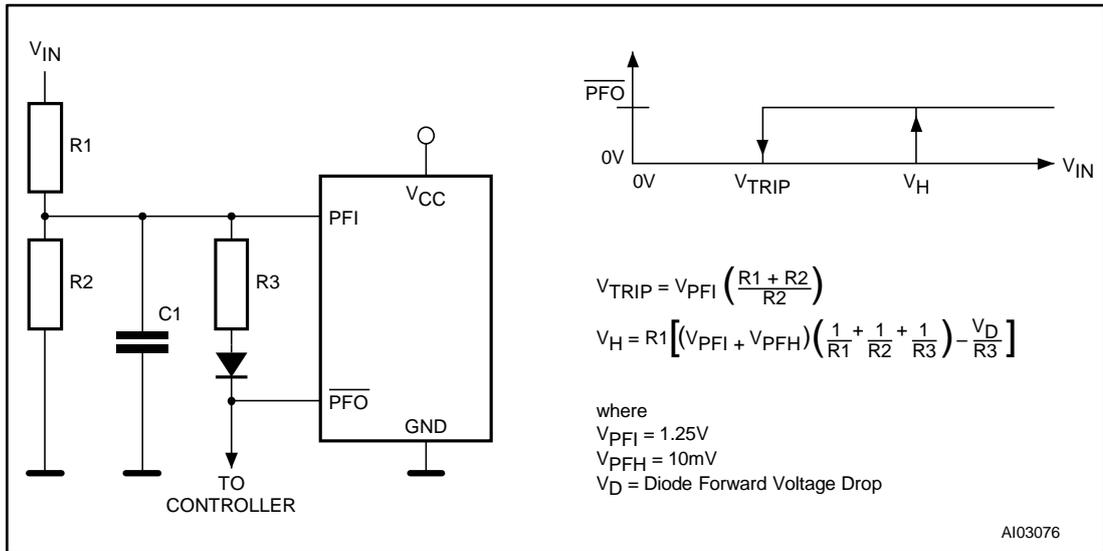
Hysteresis may be added to PFI for additional noise margin if desired (see [Figure 7: "Adding hysteresis"](#)). The ratio of R1 and R2 should be selected such that PFI sees V_{PFI} when V_{UNREG} falls to its trip point (V_{TRIP}). Connecting R3 between PFI and \overline{PFO} provides the hysteresis and should typically be more than 10 times the value of R1 or R2. The hysteresis window will extend both above (V_H) and below (V_L) the original trip point.

Figure 7: Adding hysteresis



Connecting an ordinary signal diode in series with R3 (see [Figure 8: "Hysteresis on rising \$V_{IN}\$ "](#)) so the lower trip point (V_L) coincides with the trip point without hysteresis, causing the entire hysteresis window to occur above V_{TRIP} . This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. The current through R1 and R2 should be at least $1 \mu A$ to ensure that the 25 nA PFI input current does not shift the trip point. The capacitor C1 is added for noise rejection and should be quite small (e.g. $\sim 100 \text{ nF}$), but is optional.

Figure 8: Hysteresis on rising V_{IN}



5 Revision history

Table 2: Revision history

Date	Revision	Changes
02-Jul-2001	1	Initial release
21-Mar-2014	2	Revised document presentation Updated <i>Figure 5: "PFI/PFO in a typical system"</i> Removed table entitled "Supervisory ZEROPOWER/TIMEKEEPER® products with power-fail comparator"

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