Introduction

For the PFC (power factor correction) converter, sepic topology can be used when an output voltage lower than the maximum input voltage is required. This is instead of boost topology, which is unsuitable because it must have an output voltage higher than the maximum input voltage. Sepic topology is advantageous because it allows the use of the ripple steering technique in order to reduce the switching frequency components of the input current without additional costs. This application note presents the basic equation of the sepic converter, in addition to design guidelines for a sepic PFC operating in transition mode and using the ripple steering technique. An application example with some tests results and waveforms is also provided in the document.
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1 Sepic topology for PFC converter

The most widely used topology in PFC applications is boost topology. It has two main advantages:

1. The power switch is a low sided one, unlike buck and buck-boost topology where it is an hide side one and needs a floating driving circuit.
2. The inductor is on the input side of the converter, limiting the slope of the input current.

The main disadvantage is that output voltage must always be higher than maximum input voltage, which may limit some applications and may be a problem when a lower output voltage is required.

Sepic topology has the above advantages and does not have the output voltage constraint. As in buck-boost topology, output voltage can be higher or lower than the input voltage. An additional advantage of sepic topology is that there are two inductors instead of one which can be wounded in the same magnetic core. Using the proper turn ratio the input current ripple can be reduced theoretically to zero and the input filter for the conducted electromagnetic interference strongly reduced (theoretically eliminated).

However, sepic topology, compared to boost topology, has the following disadvantages:

1. The MOSFET and the output diode break-down voltages are higher as they are the maximum reverse voltage when input and output voltages are summed (only output voltage for boost converter).
2. The current through the MOSFET is generally higher for the same output power.

1.1 Operation of the sepic converter

The basic schematic of the sepic converter is given in Figure 1.

Assuming that the average voltage across each inductor during one switching cycle, in steady state operation, is zero, it can also be assumed than the average voltage over one switching cycle across capacitor C1 equals the input voltage of the converter.

If capacitor C1 is not too small, the voltage ripple across C1 (V_{C1}) is negligible, and it can be assumed that over one switching cycle, this voltage stays constant and equals the input voltage (V_{IN}). This hypothesis (V_{C1} = V_{IN}) is the starting point for sepic converter analysis.

When the main switch (M1) of the sepic converter is on, input voltage is applied to inductor L2 (see Figure 2). In steady state condition, the same voltage is applied to inductor L1 which is in parallel with capacitor C1. The reverse voltage applied on diode D1 is the sum of the input and output voltage (V_{IN} + V_{OUT}) and the current through M1 is the sum of the currents through inductor L1 and inductor L2 (I_{L1} + I_{L2}).

Across inductor L1 and inductor L2 we have the same voltages and the currents through them rise linearly with slopes inversely proportional to their inductances values.

When M1 is switched off (Figure 3), diode D1 starts to conduct and the energy previously stored in inductor L1 and inductor L2 is released to restore the energy used up by capacitor C1 and capacitor C2 when M1 was on. This energy also supplies the load. The voltage across the MOSFET is the sum of the voltage across capacitor C1, which is equal to the sum of the input and the output voltage.
The current through diode D1 is the sum of the currents running through inductor L1 and inductor L2. The voltage across both inductors is equal to $V_{OUT}$, and the current slope is negative and inversely proportional to inductor L1 and inductor L2 respectively.

*Figure 4* shows the theoretical waveforms of the inductors’ currents. *Equation 1* and *Equation 2* give the waveform expressions during turn-on ($T_{ON}$), whilst *Equation 3* and *Equation 4* give the waveform expressions during turn-off ($T_{OFF}$).

**Equation 1**

$$I_{L1}(t) = I_{L10} + \frac{V_{IN}}{L_1} \cdot t$$

**Equation 2**

$$I_{L2}(t) = I_{L20} + \frac{V_{IN}}{L_2} \cdot t$$

**Equation 3**

$$I_{L1}(t) = I_{L10} + \frac{V_{IN}}{L_1} \cdot T_{ON} - \frac{V_{OUT}}{L_1} \cdot t$$

**Equation 4**

$$I_{L2}(t) = I_{L20} + \frac{V_{IN}}{L_2} \cdot T_{ON} - \frac{V_{OUT}}{L_2} \cdot t$$

*Figure 1. Basic circuit of the sepic converter*

*Figure 2. Sepic converter when the main switch is on*
1.2 Sepic converter as a PFC circuit operating in transition mode

In PFC applications, input voltage is the rectified main and it changes according to the equation:

\[
V_{IN}(\vartheta) = \sqrt{2} \cdot V_{ac} \cdot |\sin(\vartheta)|
\]

where \(\vartheta\) is \(2\pi f_L\), \(f_L\) is the line frequency, and \(V_{ac}\) is the rms value of the line voltage.

As switching frequency is in the range of some tenth of kHz, and thus much higher than the line frequency, we can assume \(\vartheta\) is constant over each switching cycle.

The L6562 (see [2]) is a current mode controller dedicated to PFC applications. It is used in this instance. It senses the MOSFET current and the input voltage of the converter (rectified main), through a sense resistor and a resistor divider respectively. Cycle by cycle the MOSFET is switched-off as the sensed current reaches a limit set by the controller. This limit is proportional to the sensed input voltage so, the MOSFET peak current \((I_{PK}(t))\) follows a sinusoidal reference:

\[
I_{PK}(t) = I_{PK} \cdot |\sin(\vartheta)|
\]
Taking into account that input voltage is now the rectified main, *Equation 1* and *Equation 2* can be rewritten as follows:

**Equation 7**

\[ I_{L1}(t, \theta) = I_{L10} + \frac{V_{IN}(\theta)}{L_1} \cdot t, \quad I_{L2}(t, \theta) = I_{L20} + \frac{V_{IN}(\theta)}{L_2} \cdot t \]

Due to transition mode operation, the MOSFET is switched on as soon as the diode current falls to zero. This means that:

**Equation 8**

\[ I_{L10} - I_{L20} = 0 \]

From *Equation 8*, the MOSFET peak current equation may be derived:

**Equation 9**

\[ I_{PK}(\theta) = \left( \frac{1}{L_1} + \frac{1}{L_2} \right) \cdot t_{ON}(\theta) \cdot \sqrt{2} \cdot V_{ac} \cdot \sin(\theta) \]

Combining *Equation 9* and *Equation 6* an expression for \(T_{ON}\) may be obtained:

**Equation 10**

\[ t_{ON}(\theta) = \frac{I_{PK} \cdot \sin(\theta)}{\left( \frac{1}{L_1} + \frac{1}{L_2} \right) \cdot \sqrt{2} \cdot V_{ac} \cdot \sin(\theta)} = \frac{L_e \cdot I_{PK}}{\sqrt{2} \cdot V_{ac}} \cdot T_{ON} \]

where \(L_e\) is the parallel between inductor \(L_1\) and inductor \(L_2\). *Equation 10* indicates that, as in TM (Transition Mode) boost converter \(T_{ON}\) is independent from \(\theta\).

The expression for \(T_{OFF}\) is obtained in a similar way to above:

**Equation 11**

\[ T_{OFF}(\theta) = \frac{T_{ON} \cdot \sqrt{2} \cdot V_{ac} \cdot \sin(\theta)}{V_O} \]

where \(V_O\) is the output voltage. The off time is dependent on \(\theta\), as in TM boost converter.

Once \(T_{ON}\) and \(T_{OFF}\) are known, switching frequency \(f_{SW}\) may be easily calculated as it is a function of \(\theta\):

**Equation 12**

\[ f_{SW}(\theta) = \frac{1}{T_{ON} + T_{OFF}(\theta)} = \frac{1}{T_{ON} \cdot \left( 1 + \frac{\sqrt{2} \cdot V_{ac} \cdot |\sin(\theta)|}{V_O} \right)} \]

*Figure 5* shows the switching frequency versus \(\theta\) for two different input voltages. To calculate input current averaged over one switching cycle, *Equation 13*, the charge balance on capacitor \(C_1\), is used:

**Equation 13**

\[
\left( I_{L10}(\theta) + \frac{1}{2} \cdot \frac{V_{IN}(\theta)}{L_1} \cdot T_{ON} \right) \cdot T_{ON} = \left( I_{L20}(\theta) + \frac{1}{2} \cdot \frac{V_{IN}(\theta)}{L_2} \cdot T_{ON} \right) \cdot T_{OFF}(\theta) = Q(\theta)
\]
where $Q(\vartheta)$ indicates the quantity of electrical charge that flows through capacitor $C_1$, cycle by cycle.

Combining Equation 8 and Equation 13, $I_{L20}(\vartheta)$ may be calculated as follows:

**Equation 14**

$$I_{L20}(\vartheta) = \frac{f_{SW}(\vartheta) \cdot V_{IN}(\vartheta) \cdot T_{ON}}{2} \cdot \left[ \frac{T_{ON}}{L_1} - \frac{T_{OFF}(\vartheta)}{L_2} \right]$$

Using equation 14, $I_{L2avg}$ may then be calculated using **Equation 15**:

**Equation 15**

$$I_{L2avg}(\vartheta) = \frac{1}{2} \cdot \frac{V_{IN}(\vartheta)}{L_2} \cdot T_{ON} + I_{L20}(\vartheta) = \frac{1}{2} \cdot I_{PK} \cdot \frac{|\sin(\vartheta)|}{1 + \sqrt{2} \cdot \frac{V_{AC}}{V_O} |\sin(\vartheta)|}$$

**Equation 15** shows that the input current is not exactly sinusoidal. A certain amount of distortion is related to the quantity $K_v$, which is defined as follows:

$$K_{v} = \sqrt{2} \cdot \frac{V_{AC}}{V_O}$$

**Figure 6** shows the input currents (before the bridge diodes) for different values of $V_{AC}$. The first input current, $I_0(\vartheta)$, is calculated for $K_v = 0$. It is used only as a reference, because it is completely sinusoidal. In this instance, $V_O$ is considered to be 200 V. The second input current, $I_1(\vartheta)$, is at $V_{AC} = 265$ V and the third, $I_2(\vartheta)$, is the input current at $V_{AC} = 175$ V. All currents are normalized in accordance with their respective RMS values. In figure 6, the distortion of the current with respect to a perfect sinusoid is obvious. Even though such distortion is present, quite high values for the power factor are obtained. The voltage across capacitor $C_1$ averaged over one switching cycle is the same as the input voltage. There is an additional voltage ripple due to the currents of the inductors across capacitor $C_1$. Its amplitude ($\Delta V_{C1}(\vartheta)$) is calculated below:

**Equation 16**

$$\Delta V_{C1}(\vartheta) = \frac{V_{IN}(\vartheta) \cdot T_{ON}^2}{C_1 \cdot L_e} \cdot \frac{T_{OFF}(\vartheta)}{T_{ON} + T_{OFF}(\vartheta)}$$
Substituting the values of $T_{ON}$ (Equation 10), $T_{OFF}$ (Equation 11), and $V_{IN}(\theta)$ (Equation 5), $\Delta V_{C1}(\theta)$ may be expressed as follows:

**Equation 17**

$$
\Delta V_{C1}(\theta) = \frac{L_{e}}{C_{1}} \cdot \frac{l_{PK}}{2} \cdot \frac{\sin(\theta)}{(V_{O} + \sqrt{2} \cdot V_{ac} \cdot \frac{\sin(\theta)}{\sin(\theta)})^{2}}
$$

It is useful to rewrite some quantities calculated earlier, in terms of converter output power, RMS input voltage ($V_{AC}$), and expected efficiency ($\eta$), because these quantities are generally known at the beginning of a design. Input power may be expressed as follows:

**Equation 18**

$$
P_{in} = \int_{0}^{\frac{1}{f_{L}}} \left[ \frac{l_{PK}}{2} \cdot \frac{\sin(2\pi f_{L} \cdot t)}{1 + K_{v} \cdot \frac{\sin(2\pi f_{L} \cdot t)}} \cdot \sqrt{2} \cdot V_{ac} \cdot \frac{\sin(2\pi f_{L} \cdot t)}{\sin(\theta)}} \right] \cdot dt
$$

$(F(Kv))$ may be calculated as follows:

**Equation 19**

$$
F(k_{v}) = \frac{1}{f_{L}} \cdot \int_{0}^{\frac{1}{f_{L}}} \sin^{2}(2\pi f_{L} \cdot t) \cdot \left[ \frac{1}{1 + K_{v} \cdot \frac{\sin(2\pi f_{L} \cdot t)}} \right] \cdot dt
$$

$I_{PK}$ may be expressed as follows:

**Equation 20**

$$
l_{PK} = \frac{2 \cdot P_{O}}{\eta \cdot \sqrt{2} \cdot V_{ac} \cdot F(k_{v})}
$$

The switching frequency can be expressed as:

**Equation 21**

$$
f_{sw}(\theta) = \frac{\eta \cdot V_{ac} \cdot F(k_{v})}{P_{O} \cdot L_{e} \cdot (1 + K_{v} \cdot \frac{\sin(\theta)}{\sin(\theta)})}
$$

**Figure 5.** Switching frequency variation vs $\theta$ for two different input voltages

1. Where $V_{acmin} = 175$ V, $V_{acmax} = 265$ V, $L_{e} = 1$ mH, $h = 0.9$, and $P_{O} = 65$W.
1.3 Coupled inductor sepic converter and ripple steering

If the two inductors are wounded in the same magnetic core, it is possible to reuse the equations used in Section 1.2. Moreover, the current ripple in the input inductor $L_2$ can theoretically be reduced to zero, simply by selecting the correct turn ratio. A model of two coupled inductors is shown in Figure 8. $L_{lk1}$ and $L_{lk2}$ are the leakage inductances, $L_M$ is the magnetizing inductance and $n$ is the turn ratio.

The equations that describe the coupled inductor model of Figure 8 are given below.

**Equation 22**

$$
\begin{align*}
  v_1(t) &= L_{L1} \frac{dl_1(t)}{dt} + L_M \frac{dl_M(t)}{dt} \\
  v_2(t) &= L_{L2} \frac{dl_2(t)}{dt} + n \cdot L_M \frac{dl_M(t)}{dt} \\
  \frac{dl_M}{dt} &= \frac{dl_1}{dt} + n \cdot \frac{dl_2(t)}{dt}
\end{align*}
$$

In the first two sub equations of **Equation 22**, the derivative of the magnetizing current ($l_M$) can be substituted with the value given in sub-equation 3.

Considering that the same voltage is applied to both inductors we have:

**Equation 23**

$$
\begin{align*}
  v_1(t) &= L_{EQ1} \frac{dl_1(t)}{dt} \\
  v_2(t) &= L_{EQ2} \frac{dl_2(t)}{dt}
\end{align*}
$$

**Equation 24**

$$
\begin{align*}
  L_{EQ1} &= \frac{L_{L1} \cdot L_{L2} + L_M \cdot L_{L2} + n^2 \cdot L_M \cdot L_{L1}}{L_{L2} + n \cdot (n - 1) \cdot L_M} \\
  L_{EQ2} &= \frac{L_{L1} \cdot L_{L2} + L_M \cdot L_{L2} + n^2 \cdot L_M \cdot L_{L1}}{L_{L1} - (n - 1) \cdot L_m}
\end{align*}
$$
The main conclusion of Equation 23 and Equation 24, is that the same equations can be used for coupled and uncoupled inductors. If no current flows on the secondary side, voltage $V_2$ is the same as voltage $V_2^1$ (see Figure 8) and may be written as follows:

**Equation 25**

$$V_2 = V_2^1 = n \cdot V_1^1 = n \cdot \frac{L_M}{L_M + L_{LK1}} \cdot V_1$$

As the same voltage is applied, simultaneously, to both inductors in a sepic converter, **Equation 25** may be simplified below as:

**Equation 26**

$$n \cdot \frac{L_M}{L_M + L_{LK1}} = 1$$

When the above 'ripple steering' condition is verified theoretically, the voltage across $L_{LK2}$ is zero and no current flows on the secondary side. In the actual circuit only the high frequency components of the inductor $L_2$ current are attenuated. Once **Equation 26** is verified, **Equation 24** may be simplified as:

**Equation 27**

$$\begin{align*}
L_{EQ1} &= L_M + L_{LK1} \\
L_{EQ2} &= \infty
\end{align*}$$

Therefore, for a sepic converter with coupled inductors, infinite inductance at the input may be seen theoretically once **Equation 26** is satisfied. In the actual circuit, due to imperfect matching with **Equation 26** and due to the fact that the voltages applied to the two inductors are not exactly the same (because of the voltage ripple on capacitor C1), a large input inductance may be seen at the converter input. This input inductance helps the line filter in eliminating the switching frequency component of the input current.
1.4 Small signal model for a TM sepic converter

It is possible to model the output stage of the sepic converter as a current source. The sourced current is a function of the input voltage RMS value, the output voltage, and the MOSFET peak current. To obtain the necessary function, the output diode current may first by averaged over each switching cycle, to give the following equation:

**Equation 28**

\[
I_{D1}(\theta) = \frac{k_{\text{vmin}}}{2} \cdot I_{PK} \cdot (\sin(\theta))^2 \quad \frac{1}{1 + K_v \cdot |\sin(\theta)|}
\]

Assuming that the control loop reaction must be very slow to remain constant over a single line cycle, then to ensure high PFC, **Equation 28** may be averaged with respect to \( \theta \) as follows:

**Equation 29**

\[
I_{DIAVG}(V_{ACRMS}, V_O, I_{PK}) = \frac{1}{2} \cdot \sqrt{2} \cdot \frac{V_{ACRMS}}{V_O} \cdot I_{PK} \cdot \mathcal{F} \left( \sqrt{2} \cdot \frac{V_{ACRMS}}{V_O} \right)
\]

For small variations of its argument, the \( I_{D1AVG} \) function may be approximated with a linear function, and the output stage of the sepic converter may be represented by the circuit in Figure 10. Bearing in mind that \( \mathcal{F}(K_v) \) was defined in **Equation 19**, expressions for \( g_2 \) (see Figure 10), \( e_2 \) (see Figure 10) and \( r_2 \) (see Figure 10) are given below:

**Equation 30**

\[
\begin{align*}
g_2 &= \frac{\partial I_{D1AVG}}{\partial I_{ACRMS}} \\
e_2 &= \frac{\partial I_{D1AVG}}{\partial I_{PK}} \cdot \frac{1}{2} \cdot K_v \cdot \mathcal{F}(K_v) \\
r_2 &= -\left[ \frac{\partial I_{D1AVG}}{\partial V_O} \right]^{-1} = \left[ I_{PK} \cdot \frac{K_v}{2 \cdot V_O} \cdot \mathcal{F}(K_v) + K_v \cdot \frac{\partial \mathcal{F}(K_v)}{\partial K_v} \right]^{-1}
\end{align*}
\]

It should be remembered that \( K_v \) was defined as:

\[
K_v = \frac{\sqrt{2} \cdot V_{AC}}{V_O}
\]

Also, note that \( g_2 \) is not calculated here because is not used in the control Loop design. Then, using Figure 10 and the sub-equations of **Equation 30**, it is possible to deduce the small signal transfer function (control to output) \( G(s) = V_{COMP}(s)/V_O(s) \).

**Equation 31**

\[
G(s) = \frac{\partial \dot{V}_O}{\partial V_{COMP}} = \frac{G_O}{1 + \frac{s}{\omega_p}}
\]

where the gain \( (G_O) \) and the pole frequency \( (\omega_p) \) are defined below:

**Equation 32**

\[
G_O = K_P \cdot K_M \cdot e_2 \cdot \frac{\sqrt{2} \cdot V_{ACRMS}}{R_{\text{SENSE}}} \cdot \frac{r_2 \cdot R_O}{r_2 + R_O} \quad \omega_p = \frac{r_2 - R_O}{C_2 \cdot r_2 \cdot R_O}
\]

where \( (R_O) \) is the assumed resistive load.
2 Practical design example of a sepic converter

A practical example of a sepic converter is described below.

2.1 Design specifications

For the input data, the design specifications are needed.

Table 1. Design specification

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mains voltage range: $V_{INMIN} (RMS) - V_{INMAX} (RMS)$</td>
<td>$175 , V_{ACRMS} - 265 , V_{ACRMS}$</td>
</tr>
<tr>
<td>Regulated DC output voltage</td>
<td>200 V</td>
</tr>
<tr>
<td>Rated Output Power: $P_O$</td>
<td>65 W</td>
</tr>
<tr>
<td>Minimum switching frequency: $f_{swmin}$</td>
<td>45 kHz</td>
</tr>
<tr>
<td>Maximum over-voltage admitted: $\Delta V_{OVP}$</td>
<td>40 V</td>
</tr>
<tr>
<td>Maximum output voltage ripple $\Delta V_O$</td>
<td>20 V</td>
</tr>
<tr>
<td>Expected efficiency: $\eta$</td>
<td>90 %</td>
</tr>
<tr>
<td>Maximum mains RMS current $I_{INRMSMAX}$</td>
<td>$\frac{P_O}{\eta \cdot V_{ACMIN}} = 420 mA$</td>
</tr>
</tbody>
</table>
The complete schematic of the circuit is given in Figure 13.

### 2.2 MOSFET (M₁) selection

The MOSFET peak current value \( I_{PK} \) is calculated using Equation 18. Substituting the quantities given in the electrical specifications, the MOSFET peak current value is \( I_{PK} = 2.36 \text{ A} \). The RMS value of the current flowing through the MOSFET may be calculated using Equation 33:

**Equation 33**

\[
I_{M1RMS} = I_{PK} \left( \frac{F(K_{vmin})}{3} \right) = 0.678 \text{ A}
\]

where:

**Equation 34**

\[
K_{vmin} = \sqrt{2} \frac{V_{ACMIN(RMS)}}{V_O}
\]

Under the worst case scenario, the MOSFET and the output diode have to sustain a voltage that is the sum of the maximum peak input voltage and the maximum output voltage. Considering the electrical specifications above and a safety margin of 10%, the minimum breakdown voltage \( B_{DVSSMin} \) for M1 is:

**Equation 35**

\[
B_{DVSSMin} = (\sqrt{2} \cdot V_{ACmax} + V_O + \Delta V_{OP}) \cdot 1.1 = (375 \text{ V} + 200 \text{ V} + 40 \text{ V}) \cdot 1.1 = 777 \text{ V}
\]

To avoid large heat sink, the RMS value of the through current suggests using a MOSFET with an \( R_{DSON} \) not greater than 1.5 Ohm. The selected MOSFET, the STP9NK70, has a maximum \( R_{DSON} \) of 1.2 Ohm at 25 °C and a breakdown voltage of 700 V.

### 2.3 Diode D1 selection

The average value of the diode D1 current is the output current. The RMS value of the current flowing through diode D1 can be calculated using the following formula:

**Equation 36**

\[
I_{D1RMS} = I_{PK} \left[ \frac{1}{3} \cdot \frac{1}{\pi} \int_{0}^{\pi} K_{vmin} \cdot |\sin(\theta)|^3 \right] = 0.687 \text{ A}
\]
The minimum breakdown voltage of diode D1 is the same as for the MOSFET. The selected diode D1, STTH208, has a breakdown voltage of 800 V. When it is forward biased, the voltage drop, \(V_d\), is 1.05 V and the dynamic resistance \(r_d\) is 100 m\(\Omega\). The power dissipation on D1 may easily be calculated as follows:

\[
Equation 37
P_{D1\text{Loss}} = V_d \cdot I_O + r_d \cdot I_{D1\text{RMS}}^2 = 0.388W
\]

### 2.4 Capacitor C1 selection

The equivalent inductance \(L_e\) must be calculated, using \(Equation 38\) and knowing the minimum switching frequency, the output power, and the efficiency from previous electrical specifications:

\[
Equation 38
L_e = \frac{\eta \cdot V_{ACMIN(RMS)}^2 \cdot F(k_{vmin})}{P_O \cdot f_{sw\text{min}} \cdot (1 + k_{vmin})} = 1041mH \equiv 1mH
\]

The value of capacitor C1 may be selected by imposing the maximum voltage ripple across it. Considering a maximum voltage ripple of 15 V

\[\Delta V_{C1\text{MAX}} = 15V\]

and using \(Equation 21\), the following formula may be calculated:

\[
Equation 39
C_1 = \frac{L_e \cdot I_{PK}^2}{\Delta V_{C1\text{MAX}}} \cdot \frac{1}{2} \cdot \frac{1}{(V_O + \sqrt{2} \cdot V_{ac\text{min}})} = 416nF
\]

A 470 nF capacitor was selected.

It is important to note that the voltage ripple on capacitor C1 will affect the ripple steering effect.

The difference between the voltages across the two inductors, either when the MOSFET is on or off, is the difference between the voltage on capacitor C1 and the input voltage, which effectively is the switching frequency voltage ripple, across capacitor C1.

Because of this ripple, the two inductors do not have exactly the same voltage. Even when \(Equation 26\) is perfectly satisfied, the current ripple on the input inductor L2 is not zero.

### 2.5 Output capacitor C2 selection

The output diode current, averaged over each switching cycle, is given in \(Equation 29\). The graph of this waveform is shown in \(Figure 11\). The quantity of electrical charge that goes into capacitor C2 is the same as the integral of the diode current:

\[
Equation 40
C_2 \cdot V_O(\dot{\theta}) = X(\dot{\theta}) = \int_0^\theta I_{D1}(\alpha) \cdot d\alpha
\]
Under steady state conditions, the output voltage is maximum and minimum at the two points where $I_{D1}(\theta)$ equals the output current $I_O$. Letting these angles be $\theta_1$ and $\theta_2$, the minimum output capacitor value that guarantees an output voltage ripple lower than the specified $\Delta V_O$ is:

**Equation 41**

$$C_2 = \frac{|X(\theta_1) - X(\theta_2)|}{2 \cdot \pi \cdot f_L \cdot \Delta V_O}$$

### 2.6 Transformer design

The selected magnetic core is an ETD29 made with N67 material. The effective area ($A_e$) of this core is 0.76 cm$^2$. Once the core is selected, the minimum turn number, which prevents the transformer from saturation or overheating, may be calculated using the formula:

**Equation 42**

$$N_{2 \text{min}} = \frac{V_{in} \cdot T_{ON}}{A_e \cdot \Delta B}$$

The maximum magnetic swing ($\Delta B$) selected is 0.25 T. In the current design the number of turns for the inductor $L_2$ is 125.

If the ripple steering condition is satisfied, **Equation 43** (below) may be calculated using **Equation 24**:

**Equation 43**

$$L_e = \left( \frac{1}{L_{EQ1}} + \frac{1}{L_{EQ2}} \right)^{-1} = L_{LK1} + L_M = L_{OP1}$$

It may be used to select the proper air gap, where $L_{OP1}$ is the inductance measured at the primary side with the secondary side open. Selecting the correct turn ratio to meet the ripple steering condition for an actual transformer (rather than a theoretical one) is not easy, as the internal parameters of the transformer ($L_M$ and $L_{LK1}$) are unknown. **Equation 44** is equivalent to **Equation 26** but is based on measurable quantities. $L_{SH1}$ and $L_{OP1}$ are the primary inductances, measured when the secondary side is shorted and when the secondary side is open, respectively.

**Equation 44**

$$n = \frac{L_{OP1}}{\sqrt{L_{OP1} - L_{SH1}}}$$

**Equation 44** is obtained using the hypothesis expressed in **Equation 45**:

**Equation 45**

$$L_{LK1} = \frac{1}{n^2} \cdot L_{LK2}$$

**Equation 45** is generally true if the transformer has a ‘symmetrical structure’. **Figure 12** shows two examples of transformers with a symmetrical structure. A slotted transformer (**Figure 12** b) is used in the board for the current document. The selected turn ratio ($n$) is 1.28, which gives a value of 98 turns for the inductor $L_1$. 
2.7 Selection of other components

Selection of the other components of the circuit may be made using the guidelines for a boost converter which are given in [2]. Capacitor C1 must be considered in parallel with the input capacitor, which means that a small capacitor of 10 nF is adequate for the current design.

For the control loop design the procedure used for a boost converter in [4] may be followed. The small signal model developed in this document must be considered.

The charge pump which supplies the IC, while respecting the calculated steady state values, needs to be a little over-sized. During start-up, capacitor C2 is not pre-charged by the inrush current as in a boost converter, and therefore, the charge pump provides less current. In order not to have too big a charge pump, the capacitor on the \(V_{CC}\) pin of the L6562 has to be increased during start up phase to supply the IC, even if the charge pump is not able to provide enough current.

Figure 11. Output diode current averaged over the switching cycles

![Figure 11](image)

Figure 12. Transformers with symmetrical structures

![Figure 12](image)
3 Conclusion

This document presented the sepic converter operating in transition mode for power factor correction applications. The ripple steering technique was also presented. The basic theory behind the sepic converter and the ripple steering technique was discussed and design equations were outlined. An example of a design was proposed.

3.1 References

2. L6561, enhanced transition mode power factor corrector (AN966).
3. Minimize filtering with ripple steering. Published in Analog Zone.
4. Control loop modeling of L6561-based TM PFC (AN1089)
5. Transition-mode PFC controller (L6562 datasheet)

4 Board description and bench evaluation results

4.1 Board description

This section gives the bill of material and the schematic of the board according to the electrical specifications given in Section 2.

Table 2. Bill of material

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>470 nF</td>
<td>630 V capacitor</td>
</tr>
<tr>
<td>C2</td>
<td>68 µF</td>
<td>250 V electrolytic capacitor</td>
</tr>
<tr>
<td>C3</td>
<td>10 nF</td>
<td>X2 type capacitor</td>
</tr>
<tr>
<td>C4</td>
<td>47 µF</td>
<td>25V electrolytic capacitor</td>
</tr>
<tr>
<td>C5</td>
<td>56 nF</td>
<td>100 V capacitor</td>
</tr>
<tr>
<td>C6</td>
<td>47 nF</td>
<td>Small signal capacitor</td>
</tr>
<tr>
<td>C7</td>
<td>10 nF</td>
<td>Small signal capacitor</td>
</tr>
<tr>
<td>C8</td>
<td>1.5 µF</td>
<td>Small signal capacitor</td>
</tr>
<tr>
<td>D1</td>
<td>STTH208</td>
<td>STMicroelectronics high voltage ultrafast rectifier</td>
</tr>
<tr>
<td>D2</td>
<td>BRIDGE</td>
<td>600 V, 1 A standard bridge diode</td>
</tr>
<tr>
<td>D3</td>
<td>1N4148</td>
<td>Standard diode</td>
</tr>
<tr>
<td>D4</td>
<td>15 Vz</td>
<td>15 V zener diode</td>
</tr>
<tr>
<td>F1</td>
<td>1 A</td>
<td>1 A fuse</td>
</tr>
</tbody>
</table>
Table 2. Bill of material (continued)

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTC1</td>
<td>1</td>
<td>1 Ohm NTC</td>
</tr>
<tr>
<td>Q1</td>
<td>STP9NK70</td>
<td>STMicroelectronics N-Channel 700 V supermesh™ power MOSFET</td>
</tr>
<tr>
<td>R1a, R1b</td>
<td>1 Ohm</td>
<td>1 % precision resistor</td>
</tr>
<tr>
<td>R2, R3</td>
<td>470 Kohm</td>
<td>1 % precision resistor</td>
</tr>
<tr>
<td>R4</td>
<td>12 Kohm</td>
<td>1 % precision resistor</td>
</tr>
<tr>
<td>R5</td>
<td>22 Ohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>R6</td>
<td>12 Kohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>R7, R8</td>
<td>1.2 Megaohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>R9</td>
<td>8.2 Kohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>R10</td>
<td>18 Kohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>R11</td>
<td>82 Ohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>R13, R12</td>
<td>270 Kohm</td>
<td>Resistor</td>
</tr>
<tr>
<td>T1</td>
<td>Coupled inductors</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>L6562</td>
<td>Transition mode PFC controller</td>
</tr>
</tbody>
</table>
Figure 13. Schematic of the sepic converter
4.2 Bench results

The diagrams in this section summarize the results of certain bench evaluations. They also show waveforms under different load and line conditions.

*Figure 14* illustrates the measured efficiency for different loads (65 W, 38 W and 22 W of output power) versus the input ac voltage.

*Figure 15* demonstrates the MOSFET drain voltage (Ch4), the output voltage (Ch3) and the input voltage.

The quantities that indicate the quality of the input current as power factor, THD (Total Harmonic Distortion) and crest factor, where measured at full load and for different input voltages. They are reported in *Table 3*.

*Figure 16 to Figure 19* show the currents flowing in the two inductors (Ch1: L1 current; Ch2: L2 current) for different load conditions. Letting the input voltage of the converter (the rectified main) be a perfect rectified sinusoid, it may be used as a reference and is shown as Ch4 in the above figures.

*Figure 20* illustrates the input current (Ch1) measured before the input bridge diodes. The voltage at the input of the bridge diodes (Ch4) is also shown as a reference.

*Figure 20* is input current at full load (65 W) with 230 V<sub>ac</sub> as input voltage. *Figure 21* is input current at half load (32 W) with 230 V<sub>ac</sub> as input voltage.

**Table 3. Input current quality measurements**

<table>
<thead>
<tr>
<th>Input voltage (V&lt;sub&gt;RMS&lt;/sub&gt;)</th>
<th>PFC</th>
<th>THD %</th>
<th>Crest factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>175</td>
<td>0.992</td>
<td>10.3</td>
<td>1.35</td>
</tr>
<tr>
<td>220</td>
<td>0.986</td>
<td>12.3</td>
<td>1.36</td>
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<tr>
<td>230</td>
<td>0.984</td>
<td>12.6</td>
<td>1.37</td>
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<tr>
<td>265</td>
<td>0.975</td>
<td>14.2</td>
<td>1.46</td>
</tr>
</tbody>
</table>

*Figure 14. Efficiency chart*
Figure 15. Main waveform of the circuit

1. Test conditions include $P_{out} = 65$ W and $V_{in} = 230$ VAC RMS.
Figure 16. Current of the inductors over one line cycle: $V_{in} = 230 \text{ V}_{\text{ACRMS}}$, $P_{out} = 65 \text{ W}$

Figure 17. Current of the inductors over switching cycles: $V_{in} = 230 \text{ V}_{\text{ACRMS}}$, $P_{out} = 65 \text{ W}$

Figure 18. Current of the inductors over one line cycle: $V_{in} = 230 \text{ V}_{\text{ACRMS}}$, $P_{out} = 65 \text{ W}$

Figure 19. Currents of the inductors over switching cycles: $V_{in} = 230 \text{ V}_{\text{ACRMS}}$, $P_{out} = 65 \text{ W}$
5 Revision history

Table 4. Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>05-Mar-2007</td>
<td>1</td>
<td>First issue</td>
</tr>
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</table>
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