Introduction

The STEVAL-ISV019V1 is an evaluation board based on the SPV1050 ultralow power energy harvester and battery charger. For any detail related to the SPV1050 features and performances please refer to the SPV1050 datasheet.

The evaluation board implements the boost configuration of the DC-DC converter and has the purpose of enhancing the SPV1050 based applications development by testing the silicon performance thanks to many jumpers and test points, and by helping to find out the best system configuration to make the SPV1050 working at the most of efficiency.

The STEVAL-ISV019V1 is configured to harvest energy from PV panels supplying $0.5 \text{ V} \leq V_{\text{MP}} \leq 2.5 \text{ V}$ and $30 \mu\text{A} \leq I_{\text{MP}} \leq 20 \text{ mA}$ and charge a battery with the $3.7 \text{ V}$ undervoltage protection threshold ($V_{\text{UVP}}$) and $4.2 \text{ V}$ end of charge voltage threshold ($V_{\text{EOC}}$).

Nevertheless, few easy changes on the application components (input and output resistor partitioning, $C_{\text{IN}}$ capacitor) allow to use a different PV panel and source (like TEG), and a battery, by setting the $V_{\text{MPP\_SET}}$, the $V_{\text{UVP}}$ and the $V_{\text{EOC}}$ thresholds according to the new requirements. More in detail, operating ranges can be extended as follows: $V_{\text{MP}}$ from $150 \text{ mV}$ up to $5 \text{ V}$, $I_{\text{MP}}$ up to $100 \text{ mA}$, $V_{\text{UVP}}$ down to $2.2 \text{ V}$ and $V_{\text{EOC}}$ up to $5.3 \text{ V}$.

The STEVAL-ISV019V1 evaluation board is shown in Figure 1.

Figure 1. STEVAL-ISV019V1 evaluation board
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1 Schematic and bill of material

The schematic, bill of material and gerber files can be downloaded from the Design resources tab of the STEVAL-ISV019V1 product folder on www.st.com.
Figure 2. STEVAL-ISV019V1 schematic
Figure 3. STEVAL-ISV019V1 application diagram
<table>
<thead>
<tr>
<th>Sect.</th>
<th>Item</th>
<th>Quantity</th>
<th>Reference</th>
<th>Part / value</th>
<th>Tolerance %</th>
<th>Voltage current</th>
<th>Watt</th>
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<th>Package</th>
<th>Manufacturer</th>
<th>Manufacturer code</th>
<th>More information</th>
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<td>C1</td>
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<td>15%</td>
<td>16 V</td>
<td></td>
<td>0805</td>
<td>Murata</td>
<td>GCM21BR71C4 75KA73L</td>
<td>Input capacitance</td>
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<td>Murata</td>
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<td>J1, J2, J3</td>
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<td>0805</td>
<td>VISHAY</td>
<td>CRCW08052M70FKEA</td>
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<td>Murata</td>
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Table 1. Bill of material
### Table 1. Bill of material (continued)

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<tr>
<th>Sect.</th>
<th>Item</th>
<th>Quantity</th>
<th>Reference</th>
<th>Part / value</th>
<th>Tolerance %</th>
<th>Voltage current</th>
<th>Watt</th>
<th>Technol. info.</th>
<th>Package</th>
<th>Manufacturer</th>
<th>Manufacturer code</th>
<th>More information</th>
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<td>1</td>
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<td></td>
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<td>5%</td>
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<td>17</td>
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</table>

| LDOs section | | | | | | | | | | | | |
| 19 | 2 | C6, C7 | 100 nF | 10% | X7R | 0603 | | KEMET | C0603C104K4R AC | | Tank capacitor for LDOs |
| 21 | 2 | SW1, SW2 | 5-pin male Stripline | Pitch 2.54 mm | TH | | | | | | | |
| 23 | 1 | CN3 | | 4-way screw connector | | | | | | | | |

- **Battery section**
  - 14 1 C9 47 µF 20% 10 V 0805 TDK C2012X5R1A47 6M125AC Connector for external supply of pin STORE
  - 15 1 R4 6.2 MΩ 5% 0805 RS RS-0805-6m2-5%-0.125W Resistor partitioning for UVP, EOC, protection setting
  - 16 1 R5 499 kΩ 1% 0805 VISHAY CRCW0805499 KFKEA
  - 17 1 R6 2.7 MΩ 1% 0805 VISHAY CRCW08052M70FKEA
  - 18 1 CN2 8-way screw connector TE Connectivity 282836-8 Connector for battery and battery status signals

- **LDOs section**
  - 19 2 C6, C7 100 nF 10% X7R 0603 KEMET C0603C104K4R AC Tank capacitor for LDOs
  - 21 2 SW1, SW2 5-pin male Stripline Pitch 2.54 mm TH Close 2 - 3: LDO disabled Close 1 - 2: LDO enabled Floating: external control through CN3
  - 23 1 CN3 4-way screw connector TE Connectivity 282836-4 Connector for LDOs enable connection
### List of test points

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<tr>
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<th>Quantity</th>
<th>Reference</th>
<th>Part / value</th>
<th>Tolerance %</th>
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<td>STORE pin sensing and soldering</td>
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<td>GND pin sensing (for probe scope)</td>
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</table>
2 System setup

The system setup that can be used for the evaluation of the SPV1050 device is shown in Figure 4:

![Figure 4. Measurement system setup](image)

The supply system emulates the I-V characteristic of a PV panel and it is composed by a power supply $V_{GEN}$, to determine $V_{OC}$, and a resistor $R_{IN}$, to determine $I_{MP}$ and $V_{MP}$.

Considering the typical electrical parameters of a PV panel ($V_{OC}$, $V_{MP}$, $I_{MP}$, $I_{SC}$), the supply system has to be set as following:

- $V_{GEN} = V_{OC}$
- $R_{IN} = (V_{OC} - V_{MP})/I_{MP}$

At the output stage a real battery can be connected to the BATT pin. The battery can be emulated by a power supply with a resistor ($R_{BATT}$) in series.
From *Figure 5* to *Figure 7* show the component placement and the layout (top and bottom views) of the STEVAL-ISV019V1.

*Figure 5. Layout - silkscreen view*

*Figure 6. Layout - top view*  
*Figure 7. Layout - bottom view*
The following indications must be followed in the PCB routing:

The same ground plane has to connect the exposed pad and the pins PGND and GND.

The capacitor on the STORE pin must be placed as close as possible to the pin.

The capacitors on the LDO1 and LDO2 pins must be placed as close as possible to the respective pins.

Details on the recommended layout solution are shown in Figure 8 and Figure 9.

Figure 8. Ground plane detail
Figure 9. Component placement detail
4 Component selection

This section describes the application rules to be followed for properly selecting the components around the SPV1050 device.

4.1 MPPT setting

The “Maximum Power Point” (MPP) is set through the input resistor partitioning R1, R2 and R3.

As a preliminary rule, the voltage on the MPP pin (V_{MPP}), which depends on the voltage supplied by the selected source (V_{IN}), must be \( \leq V_{UVP} \) (which is set by the output resistor partitioning R3, R4, R5).

So, the following equation:

**Equation 1**

\[
V_{MPP} = V_{IN} \frac{R_2 + R_3}{R_1 + R_2 + R_3} \leq V_{UVP}
\]

can be rewritten as follows:

**Equation 2**

\[
V_{UVP} \geq V_{OC(MAX)} \frac{R_2 + R_3}{R_1 + R_2 + R_3}
\]

\( V_{OC(MAX)} \) stands for the maximum voltage that the source can supply (open circuit voltage).

Further, the MPP_{RATIO} = \( V_{MPP \_SET}/V_{OC} \) is set by the following equation:

**Equation 3**

\[
V_{MPP \_SET} = V_{IN} \frac{R_3}{R_1 + R_2 + R_3}
\]

\[
MPP_{RATIO} \cdot V_{OC} = \frac{R_3}{R_1 + R_2 + R_3}
\]

Finally, the leakage on the input resistor partitioning must be negligible, hence typically it must be:

**Equation 4**

\[
10 \, \text{M} \Omega \leq R_1 + R_2 + R_3 \leq 20 \, \text{M} \Omega
\]

If the electrical characteristics of the selected source and battery are such that \( V_{OC(MAX)} \leq V_{UVP} \), the resistor R1 can be simply replaced by a short-circuit. Consequently, only R2 and R3 have to be selected for a proper setting of MPP_{RATIO}.

For the PV panels the \( V_{MP} \) is typically in the range between 70% and 80% of \( V_{OC} \).

For the TEG the \( V_{MPP \_SET} \) is equals to 50% of \( V_{OC} \), so the selection is \( R_1 = 0 \) and \( R_2 = R_3 \).
4.2 Input capacitance

Every 16 seconds (typical) the SPV1050 device stops switching for 400 ms. During this time frame the input capacitor C1 is charged up to $V_{OC}$ by the source: the voltage will rise according to the time constant ($T_1$), which depends both on its capacitance and on the equivalent resistance $R_{EQ}$ of the source.

In case of the PV panel source, assuming $I_{MP(min)}$ as the minimum current at which the MPP must be guaranteed, the $R_{EQ}$ can be calculated as follows:

**Equation 5**

$$R_{EQ} = \frac{V_{OC} - V_{MPP}}{I_{MP(min)}} = \frac{V_{OC} \cdot (1 - MP\text{P\textsc{Ratio}})}{I_{MP(min)}}$$

Consequently

**Equation 6**

$$C_1 \leq \frac{T_1}{R_{EQ}}$$

*Figure 10* and *Figure 11* show the effect of different value of the C1 on the time constant: too high capacitance might be not charged within the 400 ms time window affecting the MPPT precision.

![Figure 10. Input stage equivalent circuit](image1.png)

![Figure 11. Effect of C1 on sampled voltage](image2.png)

The default $C_1 = 4.7 \mu F$ capacitance covers the most typical application cases. The energy extracted from the harvested source, and stored in the input capacitance, is transferred to the load by the DC-DC converter though the inductor. The energy extracted by the inductor depends by the sink current: the higher input currents cause higher voltage drop on the input capacitance and this may result a problem for low voltage (< 1 V) and high energy (> 20 mA) sources. In such application cases the input capacitance has to be increased or, alternatively the L1 inductance has to be reduced.

The SPV1050 performances might be further improved by reducing the time constant (e.g. reducing input capacitance) at very low input power.
4.3 Capacitance on MPP-REF pin

It's recommended to use $C_8 = 10 \, \text{nF}$ in most of the application cases.

4.3.1 Inductor selection

The SPV1050 device controls the switching of the integrated DC-DC by limiting the peak current flowing through the inductor $L_1$.

$L_1 = 22 \, \mu\text{H}$ covers the most typical application range: the lower is the series resistance of the selected inductor, the lower is its DC loss. The current capability of the selected inductor must be $\geq 200 \, \text{mA}$.

4.3.2 Output voltage ripple

In case of battery with high series resistance and a fast load transient, the capacitor on the STORE pin may momentarily discharge and cause the undesired triggering of the $V_{\text{UVP}}$ threshold, implying the battery disconnection.

Although the fast transient might be masked by a proper capacitance between the UVP and GND pins, if the battery has a low peak current capability, the voltage on the STORE pin may further drop down lower than $V_{\text{UVP}}$.

The drawback of a $C_{\text{UVP}}$ between UVP and GND pins is the related delay in the intervention of the end of charge protection. The consequent voltage overshoot on $V_{\text{STORE}}$ must be always lower than the AMR of the STORE pin (5.5 V); the worst case to be considered is at maximum input power and the STORE pin in the open load.

Increasing the capacitance on the STORE pin has the drawback of affecting the output time constant and consequently delays the startup time. The same capacitor might be placed in parallel to the battery, on the BATT pin.

The selection of the battery and of the output capacitance on the STORE pin ($C_9$) is strictly related to the following application parameters:

- The series resistance of the battery ($R_{\text{BATT}}$)
- The EOC threshold ($V_{\text{EOC}}$) and the UVP threshold ($V_{\text{UVP}}$)
- The maximum load current ($I_{\text{LOAD(MAX)}}$)
- The $T_{\text{LOAD(ON)}\text{,}}$ how long the load sink $I_{\text{LOAD(MAX)}}$
- The maximum allowed voltage drop on LDOs outputs ($V_{\text{DROP(MAX)}}$)

The maximum current that can be supplied to the load is the sum of the currents that can be supplied by the battery ($I_{\text{BATT(MAX)}}$) and by the $C_9$ ($I_{\text{STORE}}$):

Equation 7

\[
I_{\text{LOAD(MAX)}} = I_{\text{BATT(MAX)}} + I_{\text{STORE}}
\]

The maximum current that the battery can supply without triggering the UVP threshold is:

Equation 8

\[
I_{\text{BATT(MAX)}} = \frac{V_{\text{BATT}} - V_{\text{UVP}}}{R_{\text{BATT}}}
\]
The amount of charge that the C9 can supply is:

**Equation 9**

\[ Q_9 = C_9 \cdot V_{DROP(MAX)} \]

Considering that \( I = C \cdot \frac{dV}{dt} \), it follows:

**Equation 10**

\[ I_{BATT(MAX)} = I_{LOAD(MAX)} - \frac{C_{STORE} \cdot V_{DROP(MAX)}}{T_{LOAD(ON)}} \]

Thus:

**Equation 11**

\[ C_{STORE} \geq T_{LOAD(ON)} \cdot \frac{I_{LOAD(MAX)} - I_{BATT(MAX)}}{V_{DROP(MAX)}} \]

### 4.3.3 UVP and EOC setting

The pins UVP and EOC have to be connected to the STORE pin by the resistor partitioning R4, R5 and R6 to setup the related thresholds by scaling down those voltage values and by comparing them with the internal voltage reference set at 1.23 V.

The design rules to setup the R4, R5 and R6 are the following:

**Equation 12**

\[ V_{BG} = V_{UVP} \cdot \frac{R_5 + R_6}{R_4 + R_5 + R_6} \]

**Equation 13**

\[ V_{BG} = V_{EOC} \cdot \frac{R_6}{R_4 + R_5 + R_6} \]

Further, in order to minimize the leakage due to the output resistor partitioning it has to be typically:

**Equation 14**

\[ 10 \, \text{M} \Omega \leq R_4 + R_5 + R_6 \leq 20 \, \text{M} \Omega \]
# 5 Board description

The STEVAL-ISV019V1 has a full set of connectors, jumpers and switches as described below:

## Table 2. CN1 connector

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## Table 3. CN2 connector

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<th>6</th>
<th>7</th>
<th>8</th>
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</thead>
<tbody>
<tr>
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<td>VBATT</td>
<td>GND</td>
<td>LDO2</td>
<td>GND</td>
<td>LDO1</td>
<td>GND</td>
<td>BATT-CON</td>
<td>BATT-CHG</td>
</tr>
</tbody>
</table>

- **V_BATT**: connect this pin to the positive of the battery.
- **LDO2**: connect this pin to the load to be supplied at 3.3 V.
- **LDO1**: connect this pin to the load to be supplied at 1.8 V.
- **BATT-CON**: output logic pin for battery connection monitoring. Please notice that this is an open drain pin, which has to be pulled up by a resistor (typically 10 MΩ) to a voltage rail lower than \( V_{\text{STORE}} \).
- **BATT-CHG**: output logic pin for battery charging status monitoring. Please notice that this is an open drain pin, which has to be pulled up by a resistor (typically 10 MΩ) to a voltage rail lower than \( V_{\text{STORE}} \).

## Table 4. CN3 connector

<table>
<thead>
<tr>
<th>CN3 pin number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPV1050 pin signal</td>
<td>LDO1_EN</td>
<td>GND</td>
<td>GND</td>
<td>LDO2_EN</td>
</tr>
</tbody>
</table>

- **LDO1_EN**: input logic pin to enable/disable the LDO1. Connect this pin to the control signal from the microcontroller.
- **LDO2_EN**: input logic pin to enable/disable the LDO2. Connect this pin to the control signal from the microcontroller.
- STORE: connect this pin to the tank capacitor $C_{\text{STORE}}$.
- GND: system ground.

The MPPT function can be disabled by pulling up the pin MPP-SET and unsoldering the resistor R2. In this case the duty cycle of the switching converter will be regulated according to the fixed end of charge voltage connected to the J3.

### Table 5. CN4 connector

<table>
<thead>
<tr>
<th>CN4 pin number</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPV1050 pin signal</td>
<td>STORE</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Table 6. J1, J2, J3: enable/disable MPPT

<table>
<thead>
<tr>
<th>J1</th>
<th>J2</th>
<th>J3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>LEAVE IT OPEN (signal monitoring)</td>
<td>OPEN: MPPT ENABLED</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLOSE: MPPT DISABLED$^{(1)}$</td>
</tr>
</tbody>
</table>

1. The R2 must be unsoldered.

### Table 7. SW1, SW2: enable/disable LDOs

<table>
<thead>
<tr>
<th>SW1</th>
<th>SW2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>CLOSE 3 - 4: LDO1 DISABLED</td>
</tr>
<tr>
<td></td>
<td>CLOSE 2 - 3: LDO1 ENABLED</td>
</tr>
<tr>
<td></td>
<td>FLOATING: EXTERNAL CONTROL BY CN3</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 6 Revision history

Table 8. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-May-2014</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>16-Jun-2016</td>
<td>2</td>
<td>Updated Section 4.3.2: Output voltage ripple on page 14 (added test).</td>
</tr>
</tbody>
</table>
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