Introduction

The STEVAL-CCA053V1 is a four-layer demonstration board designed for the evaluation of the STA333IS two-channel, high-efficiency Sound Terminal® device.

The purpose of this application note is to show:
- how to connect the STA333IS demonstration board
- the performance of the STA333IS device
- how to avoid critical board and layout issues

All the results and characterization data included in this application note have been measured using Audio Precision equipment. Reference documents consist of the STA333IS datasheet, schematic diagrams and PCB layout.

Figure 1. STEVAL-CCA053V1
Contents

1 Test conditions and connections of demonstration board .......... 4
   1.1 Power supply signal and interface connection ................... 4
   1.2 Output configuration ........................................... 4
   1.3 Required equipment ............................................. 4
   1.4 Board connections .............................................. 5

2 Schematic diagram and PCB layout ................................. 6
   2.1 Schematic ....................................................... 6
   2.2 PCB layout ..................................................... 7
   2.3 Bill of material ................................................ 8

3 APWorkbench settings ................................................ 9

4 Test results .......................................................... 10

5 Thermal test - $V_{CC} = 12.5\,\text{V}, 1\,\text{kHz},\text{ load} = 8\,\text{W (stereo)}$ ................................. 14
   5.1 Test conditions .................................................. 14
   5.2 Test results ..................................................... 14

6 Design guidelines for schematic and PCB layout ..................... 15
   6.1 General .......................................................... 15
   6.2 Decoupling capacitors ........................................... 15
   6.3 Snubber network ................................................ 15
   6.4 PCB layout ....................................................... 16
      6.4.1 Snubber layout .............................................. 16
      6.4.2 $V_{CC}$ traces ............................................... 16
      6.4.3 Ground plane and heatsink ................................ 17
      6.4.4 Output filter ............................................... 18
      6.4.5 $V_{CC}$ filter for high frequency ......................... 18

7 Revision history ...................................................... 19
### List of figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STEVAL-CCA053V1.</td>
</tr>
<tr>
<td>2</td>
<td>Demonstration board (four-layer) - connectors.</td>
</tr>
<tr>
<td>3</td>
<td>Schematic diagram - part 1.</td>
</tr>
<tr>
<td>4</td>
<td>Schematic diagram - part 2 (connectors)</td>
</tr>
<tr>
<td>5</td>
<td>STA333IS demonstration board - four-layer PCB.</td>
</tr>
<tr>
<td>6</td>
<td>APWorkbench - device selection.</td>
</tr>
<tr>
<td>7</td>
<td>APWorkbench - control panel.</td>
</tr>
<tr>
<td>8</td>
<td>THD+N vs. power - $V_{CC} = 12.5$ V, load = 8 W, 1 kHz.</td>
</tr>
<tr>
<td>9</td>
<td>THD+N vs. frequency - $V_{CC} = 12.5$ V, load = 8 W, $P_{out} = 1$ W at 1 kHz</td>
</tr>
<tr>
<td>10</td>
<td>Frequency response - $V_{CC} = 12.5$ V, load = 8 W, $P_{out} = 1$ W at 1 kHz</td>
</tr>
<tr>
<td>11</td>
<td>Crosstalk - $V_{CC} = 12.5$ V, load = 8 W, $P_{out} = 1$ W at 1 kHz</td>
</tr>
<tr>
<td>12</td>
<td>FFT - $V_{CC} = 12.5$ V, load = 8 W, $P_{out} = 1$ W at 1 kHz.</td>
</tr>
<tr>
<td>13</td>
<td>Output power vs. supply voltage - load = 8 W, 1 kHz.</td>
</tr>
<tr>
<td>14</td>
<td>Efficiency - $V_{CC} = 12.5$ V, 1 kHz, load = 8 W (stereo)</td>
</tr>
<tr>
<td>15</td>
<td>Thermal analysis - $V_{CC} = 12.5$ V - 2 x 10 W at 1 kHz.</td>
</tr>
<tr>
<td>16</td>
<td>Snubber network.</td>
</tr>
<tr>
<td>17</td>
<td>PCB layout recommendations - star routing $V_{CC}$ traces.</td>
</tr>
<tr>
<td>18</td>
<td>PCB layout recommendation - large ground plane on the top side</td>
</tr>
<tr>
<td>19</td>
<td>PCB layout recommendation - large ground plane on the inner layer 2</td>
</tr>
<tr>
<td>20</td>
<td>PCB layout recommendation - large ground plane on the inner layer 3</td>
</tr>
<tr>
<td>21</td>
<td>PCB layout recommendation - large ground plane on the bottom side</td>
</tr>
<tr>
<td>22</td>
<td>Output filter.</td>
</tr>
<tr>
<td>23</td>
<td>$V_{CC}$ filter.</td>
</tr>
</tbody>
</table>
1 Test conditions and connections of demonstration board

1.1 Power supply signal and interface connection

1. Connect the power supply to the +V_{CC} and GND terminal blocks (J2)
2. Connect the STEVAL-CCA053V1 interface board to the J4 connector
3. Connect the S/PDIF signal cable to the RCA jack on the STEVAL-CCA035V1 board. The signal source should be the Audio Precision equipment or a DVD player.
4. Adjust the voltage level of the power supply. The voltage range of the DC power supply is 4.5 V to 18 V.
5. Connect the load to the connectors J1 and J3

1.2 Output configuration

The STA333IS demonstration board can be only configured for 2.0 channels and BTL outputs.

1.3 Required equipment

- Audio Precision (System 2700)
  - Audio Analyzer: Mod. SYS2722 -192K
  - Class-D filter: AUX-0025 filter
  - Multifunction module: DCX-127
- DC power supply (4.5 V to 18 V)
  - Lambda Genesys Gen 80-19
  - HP 6038A
- Digital oscilloscope: Tektronix TDS5054B
- Digital multimeter: AGILENT Mod. 34410A
- PC with APWorkbench control software installed
1.4 Board connections

Figure 2. Demonstration board (four-layer) - connectors

- J2 DC supply
- J1 OUT1
- J3 OUT2
- J4 Connect to STEVAL-CCA035V board

Connect to STEVAL-CCA035V board.
2 Schematic diagram and PCB layout

2.1 Schematic
Figure 4. Schematic diagram - part 2 (connectors)

2.2 PCB layout

Figure 5. STEVAL-CCA053V1 board - four-layer PCB

Note: Please refer to Figure 18 through Figure 21 on page 17 for the top, inner layer 2, inner layer 3, and bottom views, respectively.
## 2.3 Bill of material

<table>
<thead>
<tr>
<th>No.</th>
<th>Type</th>
<th>Footprint</th>
<th>Description</th>
<th>Qty</th>
<th>Reference</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Connector</td>
<td>Through-hole</td>
<td>2P pitch: 5 mm connector terminal</td>
<td>3</td>
<td>J1, J2, J3</td>
<td>Any source</td>
</tr>
<tr>
<td>2</td>
<td>Header</td>
<td>Through-hole</td>
<td>16P (8 x 2 row) 2.5 mm header</td>
<td>1</td>
<td>J4</td>
<td>Any source</td>
</tr>
<tr>
<td>3</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>50 Volt NPO 330 pF ±10%</td>
<td>2</td>
<td>C12, C13</td>
<td>Murata</td>
</tr>
<tr>
<td>4</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>50 Volt 1nF ±10%</td>
<td>6</td>
<td>C1, C2, C3, C4, C5, C6</td>
<td>Murata</td>
</tr>
<tr>
<td>5</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>50 Volt 100 nF ±10%</td>
<td>6</td>
<td>C20, C21, C22, C23, C24, C27</td>
<td>Murata</td>
</tr>
<tr>
<td>6</td>
<td>CCAP</td>
<td>CAP1206</td>
<td>50 Volt 1U ±10%</td>
<td>2</td>
<td>C16, C17</td>
<td>Murata</td>
</tr>
<tr>
<td>7</td>
<td>ECAP</td>
<td>CAP1206</td>
<td>10 µF / 16 V</td>
<td>5</td>
<td>C7, C8, C10, C11, C30</td>
<td>Samsung</td>
</tr>
<tr>
<td>8</td>
<td>RES</td>
<td>R1206</td>
<td>6R2, ±5% 1/8W</td>
<td>4</td>
<td>R1, R2, R5, R6</td>
<td>Murata</td>
</tr>
<tr>
<td>9</td>
<td>RES</td>
<td>R1206</td>
<td>20 ±5% 1/8W</td>
<td>2</td>
<td>R3, R4</td>
<td>Murata</td>
</tr>
<tr>
<td>10</td>
<td>RES</td>
<td>R0603</td>
<td>2R2 ±5% 1/16W</td>
<td>1</td>
<td>R7</td>
<td>Murata</td>
</tr>
<tr>
<td>11</td>
<td>RES</td>
<td>R0603</td>
<td>NS</td>
<td>2</td>
<td>R8, R12</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Plastic</td>
<td>Hexagonal</td>
<td>Hexagonal rod 15 mm length, male type</td>
<td>4</td>
<td>Four corners</td>
<td>Any source</td>
</tr>
<tr>
<td>13</td>
<td>Plastic</td>
<td>Hexagonal</td>
<td>Hexagonal rod 8 mm length, female type</td>
<td>4</td>
<td>Four corners</td>
<td>Any source</td>
</tr>
<tr>
<td>14</td>
<td>IC</td>
<td>CSP 5x6 array</td>
<td>STA333IS</td>
<td>1</td>
<td>IC1</td>
<td>STMicroelectronics</td>
</tr>
<tr>
<td>15</td>
<td>Coil</td>
<td>SMD</td>
<td>DPM02, MARUWA</td>
<td>2</td>
<td>L5, L6</td>
<td>Maruwa</td>
</tr>
<tr>
<td>16</td>
<td>PCB</td>
<td></td>
<td>STA333IS 4-layer 1V0</td>
<td>1</td>
<td></td>
<td>Fastprint</td>
</tr>
</tbody>
</table>
3 APWorkbench settings

Figure 6. APWorkbench - device selection

Figure 7. APWorkbench - control panel
4 Test results

Figure 8. THD+N vs. power - $V_{CC} = 12.5$ V, load $= 8 \, \Omega$, 1 kHz

Figure 9. THD+N vs. frequency - $V_{CC} = 12.5$ V, load $= 8 \, \Omega$, $P_{out} = 1$ W at 1 kHz
Figure 10. Frequency response - $V_{CC} = 12.5\,\text{V}$, load = $8\,\Omega$, $P_{out} = 1\,\text{W}$ at 1 kHz

Figure 11. Crosstalk - $V_{CC} = 12.5\,\text{V}$, load = $8\,\Omega$, $P_{out} = 1\,\text{W}$ at 1 kHz
Figure 12. FFT - $V_{CC} = 12.5$ V, load = 8 $\Omega$, $P_{out} = 1$ W at 1 kHz

Figure 13. Output power vs. supply voltage - load = 8 $\Omega$, 1 kHz
Figure 14. Efficiency - $V_{CC} = 12.5$ V, 1 kHz, load = 8 $\Omega$ (stereo)
5 Thermal test - $V_{CC} = 12.5$ V, 1 kHz, load= 8 $\Omega$ (stereo)

5.1 Test conditions

$V_{CC} = 12.5$ VDC
Load= 8 $\Omega$ (resistive dummy load)
Gain= +3 dB (both L&R channels)
All channels ON
AP filter= 22 Hz ÷ 22 kHz
Output power: 2 x 10 W (adj. using post-scale)
$T_{amb} = 31$ °C

5.2 Test results

$T_{max} = 88.6$ °C
$T_{amb} = 31$ °C
$\Delta T = 57.6$ °C

Figure 15. Thermal analysis - $V_{CC} = 12.5$ V - 2 x 10 W at 1 kHz
6 Design guidelines for schematic and PCB layout

6.1 General

- Absolute maximum rating: 20 V
- Bypass capacitor 100 nF in parallel to 1 μF and 10 μF for each power VCC branch. Preferable dielectric is X7R.
- Vdd and ground for the digital section should be separated from the other power supply.
- Coil saturation current compatible with the peak current of the application

6.2 Decoupling capacitors

The decoupling capacitors can be shared for each VCC branch. The decoupling capacitors must be placed as close as possible to the IC pins.

The capacitor and the decoupling capacitor must be on the same layer as well as the track used to connect the capacitors and the positive VCC device pins.

6.3 Snubber network

The snubber circuit must be optimized for the specific application. Starting values are 330 pF in series to 22 Ω.

The power dissipation in this network can be defined by the following formula which considers the power supply, frequency and capacitor value:

\[ P = C \cdot \text{Freq}_{PWM} \cdot (2 \cdot V_{OUT})^2 \]

This power is dissipated on the series resistance.
6.4 PCB layout

6.4.1 Snubber layout

Solder the snubber network as close as possible to the related IC pin.

**Figure 16. Snubber network**

6.4.2 V\textsubscript{CC} traces

Design the PCB tracks to implement a star routing for the V\textsubscript{CC} traces.

**Figure 17. PCB layout recommendations - star routing V\textsubscript{CC} traces**
6.4.3 **Ground plane and heatsink**

To dissipate the power not delivered to the loads, a large ground plane should be implemented. This solution allows removing the heat from the device without adding an external heatsink.

*Note:* It is mandatory to have a large ground plane on the top layer, inner layer 2, inner layer 3, and the bottom layer and solder the slug on the PCB.

---

Figure 18. PCB layout recommendation - large ground plane on the top side

Figure 19. PCB layout recommendation - large ground plane on the inner layer 2

Figure 20. PCB layout recommendation - large ground plane on the inner layer 3

Figure 21. PCB layout recommendation - large ground plane on the bottom side
6.4.4 Output filter

It is recommended to design the PCB using symmetrical paths and tracks.

Figure 22. Output filter

6.4.5 $V_{CC}$ filter for high frequency

The $V_{CC}$ filter capacitors must be placed as close as possible to the supply pins. The ceramic capacitors must be positioned on the same layer of the device (in this demonstration board, on the top layer of the PCB) and the distance from the IC must be short and compatible with the minimum SMB mounting limitation.

Figure 23. $V_{CC}$ filter

The PWM frequency is 384 kHz (with $F_s = 48$ kHz) with very fast transition time. In order to compensate the inductive effect of the copper track, the ceramic capacitors must be placed as close as possible to the supply pins. The recommended distance between the capacitors and the supply pins is less than 5 mm.
7 Revision history

Table 2. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>01-Jul-2013</td>
<td>1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>