Introduction

The board shown in Figure 1 is a two-layer demonstration board designed for the evaluation of the STA333IS two-channel, high-efficiency Sound Terminal® device.

The purpose of this application note is to show:
- how to connect the STA333IS demonstration board
- the performance of the STA333IS device
- how to avoid critical board and layout issues

All the results and characterization data included in this application note have been measured using Audio Precision equipment. Reference documents consist of the STA333IS datasheet, schematic diagrams and PCB layout.

Figure 1. STA333IS 2 layer demo board
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1 Test conditions and connections of demonstration board

1.1 Power supply signal and interface connection

1. Connect the power supply to the +V_{CC} and GND terminal blocks (J2)
2. Connect the STEVAL-CCA035V1 interface board to the J4 connector
3. Connect the S/PDIF signal cable to the RCA jack on the STEVAL-CCA035V1 board. The signal source should be the Audio Precision equipment or a DVD player.
4. Adjust the voltage level of the power supply. The voltage range of the DC power supply is 4.5 V to 18 V.
5. Connect the load to the connectors J1 and J3

1.2 Output configuration

The STA333IS demonstration board can be only configured for 2.0 channels and BTL outputs.

1.3 Required equipment

- Audio Precision (System 2700)
  - Audio Analyzer: Mod. SYS2722 -192K
  - Class-D filter: AUX-0025 filter
  - Multifunction module: DCX-127
- DC power supply (4.5 V to 18 V)
  - Lambda Genesys Gen 80-19
  - HP 6038A
- Digital oscilloscope: Tektronix TDS5054B
- Digital multimeter: AGILENT Mod. 34410A
- PC with APWorkbench control software installed
1.4 Board connections

Figure 2. Demonstration board (two-layer) - connectors
2 Schematic diagram and PCB layout

2.1 Schematic

Figure 3. Schematic diagram - part 1
Figure 4. Schematic diagram - part 2 (connectors)

2.2 PCB layout

Figure 5. STA333IS demonstration board - two-layer PCB (top view)
Figure 6. STA333IS demonstration board - two-layer PCB (bottom view)
2.3 Bill of material

<table>
<thead>
<tr>
<th>N°</th>
<th>Type</th>
<th>Footprint</th>
<th>Description</th>
<th>Q.ty</th>
<th>Reference</th>
<th>Manufacturer</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>Connector</td>
<td>Through-hole</td>
<td>2P pitch: 5 mm connector terminal</td>
<td>3</td>
<td>J1, J2, J3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Header</td>
<td>Through-hole</td>
<td>16P (8x2 row) 2.5 mm header</td>
<td>1</td>
<td>J4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>50 Volt NPO 330 pF ±10%</td>
<td>2</td>
<td>C12, C13</td>
<td>Murata</td>
</tr>
<tr>
<td>4</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>50 Volt 1 nF ±10%</td>
<td>4</td>
<td>C1, C2, C3, C4</td>
<td>Murata</td>
</tr>
<tr>
<td>5</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>50 Volt 100 nF ±10%</td>
<td>6</td>
<td>C20, C21, C22, C23, C24, C27</td>
<td>Murata</td>
</tr>
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<td>6</td>
<td>CCAP</td>
<td>CAP0603</td>
<td>NS</td>
<td>8</td>
<td>C5, C6, C7, C8, C14, C15, C16, C19</td>
<td>Murata</td>
</tr>
<tr>
<td>7</td>
<td>CCAP</td>
<td>CAP1206</td>
<td>50 Volt 220 nF ±10%</td>
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<td>C10, C11, C31, C32, C33, C34</td>
<td>Murata</td>
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<tr>
<td>8</td>
<td>CCAP</td>
<td>CAP1206</td>
<td>50 Volt 1U ±10%</td>
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<td>C16, C17</td>
<td>Murata</td>
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<tr>
<td>9</td>
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<td>CAP1206</td>
<td>10 µF / 16 V</td>
<td>1</td>
<td>C30</td>
<td>Panasonic</td>
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<td>10</td>
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<td>C9</td>
<td>Panasonic</td>
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<td>11</td>
<td>RES</td>
<td>R1206</td>
<td>NS</td>
<td>4</td>
<td>R1, R2, R5, R6</td>
<td>Murata</td>
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<td>12</td>
<td>RES</td>
<td>R1206</td>
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<td>R3, R4</td>
<td>Murata</td>
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<td>13</td>
<td>RES</td>
<td>R0603</td>
<td>2R2 ±5% 1/16W</td>
<td>1</td>
<td>R7</td>
<td>Murata</td>
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<tr>
<td>14</td>
<td>RES</td>
<td>R0603</td>
<td>NS</td>
<td>2</td>
<td>R8, R12</td>
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<tr>
<td>15</td>
<td>Plastic rod</td>
<td>Hexagonal rod 15 mm length, male type</td>
<td>4</td>
<td>Four corners</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Plastic rod</td>
<td>Hexagonal rod 8 mm length, female type</td>
<td>4</td>
<td>Four corners</td>
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<td></td>
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<tr>
<td>17</td>
<td>IC</td>
<td>BGA30</td>
<td>STA333IS</td>
<td>1</td>
<td>IC1</td>
<td>STMicroelectronics</td>
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<td>18</td>
<td>Coil</td>
<td>SMD</td>
<td>SWPA6045SS4R7MT, 4.7 µH</td>
<td>4</td>
<td>L1, L2, L3, L4</td>
<td>Sunlord</td>
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<td>19</td>
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<td>STA333IS CSP 2-layer 1V1</td>
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</table>
3 APWorkbench settings

Figure 7. APWorkbench - device selection

Figure 8. APWorkbench - control panel
4 Test results

Figure 9. THD+N vs. power - $V_{CC} = 12$ V, load = 8 $\Omega$, 1 kHz

Figure 10. THD+N vs. frequency - $V_{CC} = 12$ V, load = 8 $\Omega$, $P_{out} = 1$ W at 1 kHz
Figure 11. Frequency response - $V_{CC} = 12$ V, load = 8 $\Omega$, $P_{out} = 1$ W at 1 kHz

Figure 12. Crosstalk - $V_{CC} = 12$ V, load = 8 $\Omega$, $P_{out} = 1$ W at 1 kHz
Figure 13. FFT - $V_{CC} = 12$ V, load = 8 $\Omega$, $P_{out} = 1$ W at 1 kHz

Figure 14. Output power vs. supply voltage - load = 8 $\Omega$, 1 kHz
Figure 15. Efficiency - $V_{CC} = 12$ V, 1 kHz, load = 8 $\Omega$ (stereo)
5 Thermal performance

Test conditions:
- $V_{CC} = 12 \text{ V}$
- 1 kHz sine wave
- Load = 2 x 8 $\Omega$
- Output power: 2 x 10 W

![Figure 16. Thermal performance](image)

<table>
<thead>
<tr>
<th>IC temp</th>
<th>$T_{amb} = 25 \degree C$</th>
<th>$T_{amb} = 40 \degree C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC temp</td>
<td>78$\degree$C</td>
<td>93$\degree$C</td>
</tr>
</tbody>
</table>
6 Design guidelines for schematic and PCB layout

6.1 General

- Absolute maximum rating: 20 V
- Bypass capacitor 100 nF in parallel to 1 µF and 10 µF for each power VCC branch. Preferable dielectric is X7R.
- Vdd and ground for the digital section should be separated from the other power supply.
- Coil saturation current compatible with the peak current of the application

6.2 Decoupling capacitors

The decoupling capacitors can be shared for each VCC branch. The decoupling capacitors must be placed as close as possible to the IC pins.

6.3 Output filter

![Output filter diagram](image)

**Figure 17. Output filter**

6.3.1 Snubber network

The snubber circuit must be optimized for the specific application. Starting values are 330 pF in series to 22 Ω.

The power dissipation in this network can be defined by the following formula which considers the power supply, frequency and capacitor value:

\[ P = C \cdot \text{Freq}_\text{PWM} \cdot (2 \cdot \text{Vout})^2 \]

This power is dissipated on the series resistance.
6.3.2 Main filter

The main filter is an L and C based Butterworth filter. The cut-off frequency must be chosen between the upper limit of the audio band (~20 kHz) and the carrier frequency (384 kHz).

![Figure 18. Main filter](image)

\[
C_{load} = \frac{1}{2 \pi \cdot f_{cutoff} \cdot R_{load}}
\]

\[
L_{load} = \frac{R_{load}}{2 \pi \cdot \sqrt{2} \cdot f_{cutoff}}
\]

\[
f_{cutoff} = \frac{1}{2 \pi \cdot \sqrt{2} \cdot C_{load} \cdot L_{load}}
\]

6.3.3 Damping network

The C-R-C is a damping network. It is mainly intended for high inductive loads where the speaker load could be disconnected.

![Figure 19. Damping network](image)

Table 2. Recommended values for main filter and damping network

<table>
<thead>
<tr>
<th>R_{load}</th>
<th>16 Ω</th>
<th>12 Ω</th>
<th>8 Ω</th>
<th>6 Ω</th>
<th>4 Ω</th>
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</thead>
<tbody>
<tr>
<td><strong>Main filter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L_{load}</td>
<td>47 µH</td>
<td>33 µH</td>
<td>22 µH</td>
<td>15 µH</td>
<td>10 µH</td>
</tr>
<tr>
<td>C_{load}</td>
<td>220 nF</td>
<td>330 nF</td>
<td>470 nF</td>
<td>680 nF</td>
<td>1 µF</td>
</tr>
<tr>
<td><strong>Damping network</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C damp-S</td>
<td>100 nF</td>
<td>100 nF</td>
<td>100 nF</td>
<td>100 nF</td>
<td>220 nF</td>
</tr>
<tr>
<td>C damp-P</td>
<td>100 nF</td>
<td>100 nF</td>
<td>100 nF</td>
<td>100 nF</td>
<td>220 nF</td>
</tr>
<tr>
<td>R damp</td>
<td>10 Ω</td>
<td>8.2 Ω</td>
<td>6.2 Ω</td>
<td>4.7 Ω</td>
<td>2.7 Ω</td>
</tr>
</tbody>
</table>
6.4 PCB layout

6.4.1 Snubber network
Solder the snubber network as close as possible to the related IC pin.

Figure 20. Snubber network

6.4.2 Electrolytic capacitor
Place the electrolytic capacitor first to separate the Vcc branches.

Figure 21. Electrolytic capacitor
6.4.3 Ground plane and heatsink

In order to dissipate the heat, a large ground plane is used. It is mandatory to have a large ground plane on the top and bottom layers and solder the slug on the PCB.

Figure 22. Ground plane

Large ground plane on the top side
Large ground plane on the bottom side
6.4.4 PCB symmetrical paths

For differential applications, creating symmetrical paths for the output stage is recommended.

Figure 23. Output path

Output path: the copper tracks should be placed to have symmetrical paths.
The coils must be separated to avoid crosstalk. Shielded parts must be used.

**Figure 24. Coils**

6.4.5 $V_{CC}$ filter for high frequency

The $V_{CC}$ filter capacitors must be placed as close as possible to the supply pins as well as the ceramic capacitors.

**Figure 25. $V_{CC}$ filter capacitors**

The PWM frequency is 384 kHz. In order to compensate the inductive effect of the copper track, the ceramic capacitors must be placed as close as possible to the supply pins. The recommended distance between the capacitors and the supply pins is less than 5 mm.
7 Revision history

Table 3. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tbody>
<tr>
<td>01-Jul-2013</td>
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<td>Initial release.</td>
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