Introduction

The EVLHVLED815W8CV demonstration board shows how to implement a high power factor LED driver with a constant voltage regulation, using the single-stage primary side HVLED815PF controller.

The HVLED815PF device is an integrated power controller with primary side control to achieve the LED current regulation within ± 5%.

It also has a primary side voltage regulation and this AN shows how to reach the high power factor with the constant voltage (CV) regulation.

The device incorporates an 800 V avalanche rated FET and fits in a standard SO-16 package. An internal start-up circuit eliminates the need for an external start circuitry reducing the component counts/space and increases system efficiency.

Figure 1. Demonstration board - top side view
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The main features of the demonstration board are:

- Output constant voltage (CV regulation)
- High power factor - PF > 0.98
- High efficiency - up to 88%
- Primary side regulation - no optocoupler
- Fully isolated output (flyback topology)
- Tight output voltage regulation < ± 3%
- Low total harmonic distortion - THD < 30%
- Automatic self-supply (internal high voltage startup)
- Minimum component count (internal Power MOSFET)

The main electrical specification requirements of the driver are summarized in the list:

- Input voltage \( (V_{IN}) \) 230 Vrms (200 - 265 Vac)
- Output voltage \( (V_{OUT}) \) 25 V
- Output voltage ripple \( (\Delta V_{OUT}^{pk-pk}) \) < 3%
- Maximum output current \( (I_{OUT}^{MAX}) \) 310 mA
- Overcurrent protection \( (I_{OUT}^{CC}) \) 375 mA
- Maximum output power \( (P_{OUT}^{MAX}) \) 7.8 W
- LED driver efficiency \( (\eta) \) > 0.85%
- Minimum switching frequency \( (F_{sw}^{MIN}) \) 100 kHz
- Reflected voltage \( (V_R) \) 100 V
2 Circuit description and design guidelines

2.1 Preliminary consideration

The HVLED815PF controller is specifically designed to work as a constant current (CC) LED driver with a primary side regulation (PSR) and a high power factor (HPF) capability.

As shown on the left side of Figure 2, the HVLED815PF device incorporates two control loops: the current control loop (constant current - CC) through the ILED pin regulates the LED output current \( (I_{OUT}^{CC}) \) and the voltage control loop (constant voltage - CV) through the COMP pin regulates the output voltage during the open-LED fault condition.

The voltage control loops can then be used to regulate the output voltage when the output current is lower than the maximum deliverable current \( (I_{OUT}^{CC}) \) resulting in an output characteristic showed on the right side of Figure 2.

![Figure 2. Voltage and current control principle (left side) and output characteristic (right side)](image)

Starting from the standard application schematic (see Figure 1: “Application circuit for high power factor LED driver - single range input” in the HVLED815PF datasheet for the details) the constant current LED driver can be easily “converted” into a constant voltage LED driver (CV) still keeping the high power factor and low total harmonic distortion (THD).

The high power factor is implemented adding through the \( R_{PF} \) resistor a contribution proportional to the \( V_{IN} \) input voltage on the CS pin: as a consequence the input current is proportional to the input voltage during the line period, implementing the high power factor correction.

In the CC LED driver the \( R_{OS} \) resistor has been mainly used to add on the CS pin a positive contribution proportional to the average value of the input voltage \( (V_{IN}) \) in order to keep a good line regulation. The second advantage of the contribution through the \( R_{OS} \) resistor is to keep a good total harmonic distortion (THD) over the line range, because adding a small offset on the CS pin the input current can go to zero when the input voltage is close to zero.

When implementing a CV LED driver the voltage control loop works to keep the output voltage constant and independent from the input voltage, so the contribution proportional to the average value of the input voltage is no more needed.
A small offset on the CS is still useful to keep a good THD and so it can be added using a resistor from the VCC pin instead of a partitioning from the input voltage resulting in a reduction of the dissipated power and the component count/size.

The $V_{OUT}$ output voltage is regulated through the CV loops and it has to be designed in order to have system bandwidth much lower than current loop bandwidth (voltage loop BW $\ll 100$ Hz - 120 Hz); the current loop is instead used to set the maximum deliverable current $I_{OUT}^{CC}$.

The design can be set defining an equivalent current sense resistor according to the standard HVLED815PF equation for the output current setting:

Equation 1

$$R_{SENSE,\, EQ} = \frac{n}{2} \cdot \frac{V_{CLED}}{I_{OUT}^{CC}}$$

where $n$ is the transformer ratio between the primary ($N_P$) and secondary side ($N_S$). $V_{CLED}$ is the internal equivalent reference voltage ($V_{CLED} = 0.2$ V). See the HVLED815PF datasheet for more details.

2.2 Transformer selection

The main parameters of the flyback transformer ($L_P, N_P, N_S, N_{AUX}, L_{UK}$) have to be designed in order to sustain the desired output voltage ($V_{OUT}$), the maximum output power ($P_{OUT}$), the device supply ($V_{CC}$) and the desired reflected voltage on the primary side ($V_R$).

The transformer magnetization inductance ($L_P$) is selected as a trade-off between the maximum switching frequency (internally limited up to 166 kHz) and the maximum output power, according to Equation 2:

Equation 2

$$L_{P,\, MAX} = \frac{V_{INMIN}}{\left(1 + \frac{V_{INMIN}}{V_R}\right)} \cdot \frac{1}{F_{SWMIN}} \cdot \frac{1}{I_p \cdot \sqrt{2}}$$

where $I_p$ is the primary peak current and it can be estimated using Equation 3:

Equation 3

$$I_p(V_{IN}, I_{OUT}) = I_{OUT,\, MAX} \cdot \left(2 \cdot \frac{N_P}{N_S} \cdot \left(1 + \frac{V_R}{\eta \cdot V_{INMIN}}\right)\right)$$

The ratio between the primary ($N_P$) and secondary ($N_S$) winding can be selected to reach the desired reflected voltage ($V_R$), using Equation 4:

Equation 4

$$\frac{N_P}{N_S} = \frac{V_R}{V_{OUT} + V_D} \approx \frac{V_R}{V_{OUT}}$$

where $V_R$ is the desired reflected voltage, $V_D$ the forward voltage of the output diode.
The $V_R$ reflected voltage is selected as a trade-off between efficiency (higher $V_R$ means lower switching losses on the flyback Power MOSFET) and the absolute voltage on the primary side switching node (higher $V_R$ means higher spike voltage on the Power MOSFET’s drain). Typical range of this parameter is between 70 V and 140 V.

Assuming a desired reflected voltage of 100 V the ratio becomes:

**Equation 5**

\[
\frac{N_P}{N_S} = \frac{V_R}{V_{OUT} + V_D} = \frac{100V}{25V + 0.8V} = 3.87
\]

The ratio between the auxiliary ($N_{AUX}$) and primary ($N_P$) winding has to be selected to guarantee the supply voltage for the IC when the output voltage is regulated (during the startup the IC supply voltage is generated by the internal high voltage startup).

**Equation 6**

\[
\frac{N_S}{N_{AUX}} = \frac{V_{OUT} + V_D}{V_{CC(IC)}}
\]

where typically the IC voltage is designed in the range of 17 V - 18 V (typ.).

In this design the IC voltage has been selected 15 V resulting in a higher secondary-auxiliary transformer turns ratio:

**Equation 7**

\[
\frac{N_S}{N_{AUX}} = \frac{25V + 0.8V}{15V} = 1.72
\]

Assuming a transformer with $N_P = 125$ T, the secondary and auxiliary winding turn results $N_S = 33$ T, $N_{AUX} = 19$ T.

Putting the value of **Equation 7** into **Equation 3** and resolving the **Equation 2**, the maximum transformer magnetization inductance can be estimated:

**Equation 8**

\[
L_{PMAX} = \frac{200V}{(1 + \frac{200V}{100V})} \cdot \frac{1}{100kHz} \cdot \frac{1}{310mA \cdot (2 \cdot 3.87) \cdot \left(1 + \frac{100V}{0.85 \cdot 200V}\right) \cdot \frac{1}{\sqrt{2}}} = 1.73mH
\]

The selected magnetization inductance is $L_P = 1.4$ mH.

The leakage inductor of the transformer should be minimized to reduce the voltage spike on the drain node when the MOSFET is turned OFF - the maximum leakage inductor value is typically selected < 3% of the primary magnetizing value ($L_{LK} < 3% \cdot L_P$).
2.3 Output voltage control - primary side regulation

The IC is specifically designed to work in a primary side regulation (PSR) and the output voltage is sensed through a voltage partition of the auxiliary winding, as shown in Figure 3.

The signal on the DMG pin is sampled-and-held at the end of transformer demagnetization to get an accurate image of the output voltage (V\textsubscript{OUT}) and it is compared with the internal error amplifier reference voltage V\textsubscript{REF} (2.51 V typ.).

During the MOSFET’s OFF-time the leakage inductance resonates with the drain capacitance and a damped oscillation is superimposed on the reflected voltage. The internal S/H logic is able to discriminate such oscillations from the real transformer demagnetization.

When the DMG logic detects the transformer demagnetization, the sampling process stops, the information is frozen and compared with the error amplifier internal reference.

The internal error amplifier is a transconductance type and delivers on the COMP pin a current proportional to the voltage unbalance of the two inputs: the COMP pin generates the control voltage that is compared with the voltage across the sense resistor, thus modulating the cycle-by-cycle peak drain current to regulate the desired output voltage.

Figure 3. Voltage control principle: internal schematic

The COMP pin is used for the frequency compensation: typically an R\textsubscript{C} - C\textsubscript{C} network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

When implementing the high power factor (HPF - see Section 2.4: High power factor implementation), the output voltage control loop must have frequency bandwidth much lower than the “control current loop” (100/120 Hz, that is the double of line input frequency). As a consequence the output voltage control loop has to be designed in order to have bandwidth much lower than 100/120 Hz (i.e. BW\textsubscript{CV} < 5 - 10 Hz).
Referring to the HVLED815PF datasheet, the average output voltage can be easily programmed through the $R_{FB}$ resistor, using **Equation 9**:

**Equation 9**

$$R_{FB} = R_{DMG} \cdot \frac{V_{REF}}{\left(\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT}^2 - V_{REF}\right)}$$

where $N_{AUX}$ and $N_{SEC}$ are the auxiliary and secondary turn numbers respectively and $V_{REF}$ is the internal reference voltage (2.51 V typ.).

The $R_{DMG}$ resistor is designed to keep the line feed-forward and it can still be calculated as shown in the HVLED815PF datasheet, considering the equivalent $R_{SENSE\_EQ}$ resistor defined in **Equation 1**:

**Equation 10**

$$R_{DMG} = \frac{N_{AUX} \cdot L_{P} \cdot R_{FF}}{N_{P}} \cdot \frac{T_{D} \cdot R_{SENSE\_EQ}}{125 \cdot 100 \cdot 1.08} = 82k\Omega$$

where $R_{FF}$ and $T_{D}$ - the internal feed-forward resistor and the MOSFET turns OFF delay time respectively. For more details see section 4.7: “Voltage feed-forward block” in the HVLED815PF datasheet.

Using the calculated $R_{DMG}$ resistor, the $R_{FB}$ resistor can be calculated using **Equation 9**.

**Equation 11**

$$R_{FB} = 82k\Omega \cdot \frac{2.51V}{\left(\frac{19T}{33T} \cdot 25V\right) - 2.51V} = 17.3k\Omega$$

### 2.4 High power factor implementation

Referring to **Figure 4**, the $R_{PF}$ resistor (R6 on the application schematic) gives a contribution proportional to the input voltage on the CS pin: as a consequence the input current is proportional to the input voltage during the line period, implementing a high power factor correction.

In particular, the contribution proportional to the input voltage is generated using the auxiliary winding - diode in series to the $R_{PF}$ resistor is needed to avoid any injection on the CS pin when the auxiliary winding is positive.

As mentioned in **Section 2.3**, through the $R_{OS}$ resistor (the R14 resistor on the schematic between the CS pin and VCC pin) a positive offset on the CS pin is added, in order to keep a good THD. This offset can be designed using **Equation 12**:

**Equation 12**

$$V_{OS} = V_{CC} \cdot \frac{[(R_{CS} + R_{SENSE}) / / R_{PF}]}{[(R_{CS} + R_{SENSE}) / / R_{PF}] + R_{OS}} = K \cdot V_{CS}^{CV}$$

where $V_{CS}^{CV}$ is the voltage on the CS pin that is imposed by the voltage control loop and $K$ is a constant that by experience is selected in the range of 2/3 - 3/4.
The voltage on the CS pin depends on the ratio between the delivered output current ($I_{OUT}$) and the maximum deliverable current ($I_{OUT-CC}$) and so it can be estimated using *Equation 13*:

$$V_{CS}^{CV}(I_{OUT}) = \left[V_{CLED} \cdot \left(1 + \frac{\eta \cdot V_{inRMS}}{VR} \right) \right] \cdot \frac{I_{OUT}}{I_{OUT-CC}}$$

where $V_R$ is the reflect voltage ($V_R = V_{OUT} \cdot N_P/N_S$), $V_{inRMS}$ is the RMS value of the input voltage, $\eta$ is system efficiency and $I_{OUT-CC}$ is the maximum delivered current that can be programmed through the current control loop.

Assuming then $R_{PF} << R_{CS}$ and $R_{SENSE} << R_{CS}$, *Equation 13* can be simplified and the $R_{OS}$ resistor results:

$$R_{OS} = \frac{V_{CC} - [K \cdot V_{CS}^{CV}]}{[K \cdot V_{CS}^{CV}]} \cdot R_{CS}$$

where $V_{CC}$ is the IC supply voltage and it has been designed according to the secondary-to-auxiliary winding ratio (see *Equation 7*).

The $R_{CS}$ resistor (R1 on the schematic in *Figure 7*) between the CS pin and SOURCE pin is needed to add on the CS pin also the contribution proportional the output current through the $R_{SENSE}$ resistor.

The R1 resistor is typically selected in the range of 0.5 - 1.0 kΩ in order to minimize the internal feed-forward effect and to minimize the power dissipation on the $R_{PF}$ resistor.

Using the previous formulas the $R_{OS}$ resistor can be estimated:

$$R_{OS} = \frac{V_{CC} - [K \cdot V_{CS}^{CV}]}{[K \cdot V_{CS}^{CV}]} \cdot R_{CS} = \frac{15V - \left\{ \left[ \frac{3}{4} \cdot (0.2V \cdot (1 + \frac{100V}{0.85} \cdot 200V)) \right] \cdot \left[ \frac{310mA}{375mA} \right] \right\}}$$

$$\cdot \left\{ \left[ \frac{3}{4} \cdot (0.2V \cdot (1 + \frac{100V}{0.85} \cdot 200V)) \right] \cdot \left[ \frac{310mA}{375mA} \right] \right\}$$

$$\cdot 1k\Omega = 76.8k\Omega$$

The capacitor between the CS pin and ground could be useful when the transformer leakage inductor cannot be minimized (voltage spike on the drain pin could be coupled from the CS net).

The $R_{PF}$ resistor gives a contribution proportional to the input voltage and it can be estimated using *Equation 16*, considering the maximum input voltage:

$$R_{PF} = R_{CS} \cdot \left[ \frac{(V_{inMAX} \cdot \sqrt{2} \cdot R_{OS} \cdot N_{AUX}) - (V_{CC} \cdot R_{CS} \cdot N_P)}{N_P \cdot (0.75 \cdot R_{OS} + V_{CC} \cdot R_{CS})} \right]$$
Using the calculated value of $N_{AUX}$, $N_{P}$, $R_{OS}$ and $R_{CS}$ the $R_{PF}$ resistor results:

**Equation 17**

\[
R_{PF} = 1\, k\Omega \cdot \left[ \frac{265V \cdot \sqrt{2} \cdot 76.8k\Omega \cdot 19T} {125T \cdot (0.75 \times 76.8k\Omega \cdot 15V \cdot 1k\Omega)} \right] = 59k\Omega
\]

**Figure 4. HPF connections**

The voltage loop changes the voltage on the CS pin to keep the output voltage regulated. Respect to the standard circuit (no high power factor implementation through $R_{PF}$ and $R_{OS}$), the contributions proportional to $V_{IN}$ trough the $R_{PF}$ resistor and the offset through the $R_{OS}$ resistor give of course a modification of the voltage across the $R_{SENSE}$ resistor generating a different gain between the $R_{SENSE}$ and CS pin.

The $V_{OS}$ offset voltage is basically selected to have no input current when the input voltage is close to zero at the minimum line condition: as a consequence the voltage across the $R_{SENSE}$ resistor is basically equal to the voltage generated by the $R_{PF}$ resistor.

The $R_{SENSE}$ can be estimated imposing the equality between the two ratios, in the worst-case condition (minimum line and maximum deliverable current $I_{OUT}^{CC}$):

**Equation 18**

\[
\frac{V_{CS}^{CV}}{R_{SENSE, EQ}} = \left[ \frac{R_{CS} \cdot \frac{V_{AUX}}{R_{PF} \cdot \sqrt{2}}} {R_{SENSE}} \right]
\]

where $V_{AUX}$ is the voltage present at the auxiliary winding when the MOSFET is ON:
Equation 19
\[ V_{\text{AUX}} = V_{\text{IN}} \cdot \frac{N_{\text{AUX}}}{N_p} \]

Replacing Equation 1, Equation 13, and Equation 18 in Equation 17, the \( R_{\text{SENSE}} \) resistor results:

Equation 20
\[ R_{\text{SENSE}} = \frac{1}{2} \cdot \frac{N_{\text{AUX}} \cdot R_{\text{CS}}}{N_s \cdot R_{\text{PF}}} \cdot \frac{1}{I_{\text{OUT,CC}}} \cdot V_{\text{inRMS,MIN}} \left( \frac{V_R}{1 + \eta \cdot V_{\text{inRMS,MIN}}} \right) \]

The resistors \( R_{\text{SENSE}}, R_{\text{FB}}, R_{\text{DMG}}, R_{\text{OS}}, R_{\text{CS}}, R_{\text{PF}} \) determine the output voltage and the maximum deliverable current setting - suggested accuracy of these parameters is 1%.

2.5 Output filter

The output filter has to be designed to respect the output voltage ripple specification \( \Delta V_{\text{OUT,PK-PK}} \). In this kind of application, the single-stage high power factor, the high frequency ripple at the switching frequency can be neglected respect to the low frequency ripple at double line frequency (100/120 Hz).

The output capacitor value can then be estimated using Equation 21:

Equation 21
\[ C_{\text{outMIN}} = \frac{0.4}{\pi} \cdot \frac{I_{\text{OUT,MAX}}}{f_{\text{line}}} \cdot \Delta V_{\text{OUT,PK-PK}} = \frac{0.4}{\pi} \cdot \frac{310 \text{mA}}{50 \text{Hz} \cdot 0.75 \text{V}} = 1005 \mu\text{F} \]

For this design, three output capacitors of 330 \( \mu\text{F}/64 \text{ m\Omega}/35 \text{ V} \) have been selected.

2.6 Voltage control loop compensation

As mentioned in Section 2.3 the voltage control loop must have frequency bandwidth much lower than the "control current loop" to avoid any interaction between the two loops. The current loop "works" at the double of line input frequency (100 - 120 Hz), resulting in suggested voltage loop bandwidth in the range of 5 - 10 Hz (\( BW_{\text{CV}} < 1/10 \) of current loop bandwidth).

The small signal system voltage loop gain can be estimated considering the equivalent schematic in Figure 5.

Equation 22
\[ G_{\text{loop,CV}}(s) = G_{p}(s) \cdot G_{c}(s) = [G_{\text{pwm}} \cdot G_{\text{ps}}(s)] \cdot [G_{\text{ea}} \cdot G_{\text{sh}}(s) \cdot G_{\text{fb}}] \]
where the previous transfer functions are:
- \( G_{PWM} \) is the internal PWM modulator gain (\( G_{PWM} = 0.5 \))
- \( G_{PS}(s) \) is the power stage transfer function (transformer and output filter)
- \( G_{Fp} \) is the feedback gain between the \( V_{OUT} \) and DMG pin
- \( G_{Sh}(s) \) is the internal sample and hold transfer function
- \( G_{EA}(s) \) is the error amplifier transfer function (COMP pin network)

**Figure 5. Equivalent small signal voltage control loop schematic**

The power stage transfer function is calculated considering the transfer function of a standard flyback converter:

**Equation 23**

\[
G_{PS}(s) = G_{0 PS} \cdot \frac{\left(1 + \frac{s}{\omega z_{1 PS}}\right) \cdot \left(1 - \frac{s}{\omega z_{2 PS}}\right)}{\left(1 + \frac{s}{\omega p_{PS}}\right)}
\]

**Equation 24**

\[
G_{0 PS} = \frac{1}{2} \cdot N_P \cdot \frac{R_{OUT}}{R_{SENSE}} \cdot \frac{1 - d_P}{1 + d_P}
\]

**Equation 25**

\[
\omega z_{1 PS} = \frac{1}{ESR \cdot C_{OUT}}
\]
Equation 26
\[ \omega z_{2\,ps} = \frac{N_P^2 \cdot R_{\text{OUT}} \cdot (1 - d_p)^2}{L_p \cdot d_p} \]

Equation 27
\[ \omega p_{\,ps} = \frac{1 + d_p}{R_{\text{OUT}} \cdot C_{\text{OUT}}} \]

where ESR is the equivalent output capacitor resistance and \( d_p \) is the primary duty-cycle that depends on the input and output voltage and it can be estimated with Equation 28:

Equation 28
\[ d_p = \frac{V}{V_R + \eta \cdot V_{\text{inRMS}}} \]

The power stage presents one pole at low frequency (this pole is basically related to the output filter time constant), and two zeros. Note that one zero is positive, resulting in a negative contribution on the phase margin.

Replacing the component value on Equation 25, Equation 26, Equation 27 and considering the \( V_{\text{inRMS},\,\text{typ}} \) and \( I_{\text{OUT},\,\text{MAX}} \), the frequency singularities of the power stage result:

\[ f_{p,\,ps} = 2.6 \, \text{Hz} \quad f_{z1,\,ps} = 2.5 \, \text{kHz} \quad f_{z2,\,ps} = 183 \, \text{kHz}. \]

The feedback gain transfer function is the ration between the output voltage and the DMG pin, and it is calculated using Equation 29:

Equation 29
\[ G_{\text{fb}} = \frac{N_{\text{AUX}} \cdot R_{\text{FB}}}{N_S \cdot R_{\text{FB}} + R_{\text{DMG}}} \]

The sample and hold transfer function can be neglected because system voltage loop bandwidth is much lower than the system switching frequency (the pole of the sample and hold circuitry is at higher frequency than system bandwidth \( BW_{\text{CV}} \ll F_{pS&H} \)):

Equation 30
\[ G_{\text{sh}}(s) \cong 1 \]

Typically an \( R_C - C_C \) series network is connected between the COMP pin and ground to compensate the system loops, resulting in the following error amplifier transfer function:

Equation 31
\[ G_{\text{ea}}(s) = G_{\text{ea0}} \cdot \frac{1 + \frac{s}{\omega z_{\,\text{ea}}}}{s} \]

Equation 32
\[ G_{\text{ea0}} = \frac{g_{m}}{C_C} \]
Equation 33
\[
\omega z_{ea} = \frac{1}{R_C \cdot C_C}
\]
where \( g_m \) is the transconductance gain of the internal operational transconductance amplifier (\( g_m = 2.2 \text{ mS typ} \)). For more details, see the HVLED815PF datasheet - Table 5: “Electrical characteristics”.

Inserting the Equation 22 to Equation 33 in Equation 21, the small signal system control loop transfer function results:

Equation 34
\[
G_{\text{loop CV}}(s) = G_{\text{loop0}} \cdot \frac{(1 + \frac{s}{\omega p \cdot p}) \cdot (1 - \frac{s}{\omega z \cdot p}) \cdot (1 + \frac{s}{\omega z_{ea}})}{1 + \frac{s}{\omega p \cdot p}}
\]

Equation 35
\[
G_{\text{loop0}} = \frac{1}{2} \cdot \left( \frac{N_P}{N_S} \cdot \frac{R_{\text{OUT}}}{R_{\text{SENSE}}} \right) \cdot \frac{1 - d_P}{1 + d_P} \cdot \left( \frac{N_{\text{AUX}}}{N_S} \cdot \frac{R_{\text{FB}}}{R_{\text{FB}} + R_{\text{DMG}}} \right) \cdot \left( \frac{g_m}{C_C} \right)
\]

As mentioned in Section 2.3 control voltage loop bandwidth (BWCV) has to be designed at very low frequency (i.e. 5 - 10 Hz) to avoid the interaction with the “current loop”: as a consequence the zeros of the power stage can be typically “neglected” because they are at much higher frequency than system bandwidth resulting in a simplified loop gain calculation:

Equation 36
\[
G_{\text{loop CV}}(s) \approx G_{\text{loop0}} \cdot \frac{1}{s} \cdot \left( \frac{1 + \frac{s}{\omega z_{ea}}}{1 + \frac{s}{\omega p \cdot p}} \right)
\]

Equation 35 shows the simplified voltage control loop gain formula having two pole and one zero in the frequencies range of interest.

The external compensation network (\( R_C, C_C \)) introduces a pole in the origin and one zero that can be selected to both stabilize the system voltage control loop and to obtain desiderated system bandwidth BWCV.

Considering the control loop gain estimated in Equation 36, the \( R_C \) resistor and the \( C_C \) capacitor can be programmed using the following relationships:

Equation 37
\[
R_C = \text{BWCV} \cdot \left( \frac{4 \cdot \pi \cdot C_{\text{OUT}} \cdot R_{\text{SENSE}}}{g_m} \right) \cdot \left( \frac{N_S^2}{N_{\text{AUX}} \cdot N_P} \right) \cdot \left( \frac{R_{\text{FB}} + R_{\text{DMG}}}{R_{\text{FB}}} \right) \cdot \left( 1 + \frac{V_R}{\eta \cdot V_{\text{in RMS}}} \right)
\]

\[
= 5 \cdot \left( \frac{4 \cdot \pi \cdot 3 \cdot 330 \mu \text{F}}{2.2 \text{mS}} \right) \cdot \left( \frac{337^2}{191 \cdot 125} \right) \cdot \left( \frac{17.3 \text{k}\Omega + 82k\Omega}{17.3 \text{k}\Omega} \right) \cdot \left( 1 + \frac{100V}{0.85 \cdot 230V} \right) = 215\Omega
\]
Equation 38

\[ C_C \approx \frac{1}{R_C \cdot (4 \cdot \pi \cdot B W_{CV})} = \frac{1}{220 \Omega \cdot (4 \cdot \pi \cdot 5 \text{Hz})} = 74 \mu \text{F} \]

A capacitor between the COMP pin and ground can be also added to remove the high frequency voltage ripple without impacting on the transfer function (i.e. adding a small capacitor in the range of few nF).

**Figure 6. Transfer function**

2.7 System design tips

Starting from the estimated value using *Equation 11, Equation 15, Equation 17, Equation 20, Equation 37* and *Equation 38*, further fine tuning on the real LED driver board could be necessary and it can be easily done considering that:

- Decreasing the \( R_{PF} \) resistor value, the power factor effect increases
- Decreasing the \( R_{OS} \) resistor value, the input current close to zero decreases
- Decreasing the \( R_{SENSE} \) resistor value, the maximum deliverable output current increases
- Increasing the \( C_C \) compensation capacitor, the system phase margin increases and voltage loop bandwidth decreases.
- Decreasing the \( R_C \) compensation resistor, the voltage loop gain/bandwidth decreases and also the ripples on the COMP pin.
3  Schematic and bill of materials

Figure 7. Demonstration board schematic
<table>
<thead>
<tr>
<th>Ref.</th>
<th>Value</th>
<th>Part number</th>
<th>Vendor</th>
<th>Package</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD1</td>
<td>600 V-0.8 A</td>
<td>HD06-T</td>
<td>DIODES® INC.</td>
<td>Mini DIP</td>
<td>Bridge rectifier</td>
</tr>
<tr>
<td>C1</td>
<td>47 nF</td>
<td>B32921C3473</td>
<td>EPCOS</td>
<td>DIP 5 x 11 x 13</td>
<td>Input filter capacitor</td>
</tr>
<tr>
<td>C2</td>
<td>68 nF</td>
<td>B32921C3683</td>
<td>EPCOS</td>
<td>DIP 5 x 11 x 13</td>
<td>Input filter capacitor</td>
</tr>
<tr>
<td>C3</td>
<td>1 nF</td>
<td>C3216X7R2J102K</td>
<td>TDK</td>
<td>SMD 1206</td>
<td>Snubber capacitor</td>
</tr>
<tr>
<td>C4</td>
<td>22 μF/50 V</td>
<td>EUFR1H220</td>
<td>Panasonic</td>
<td>RADIAL 5 x 11.5</td>
<td>( V_{CC} ) filter capacitor</td>
</tr>
<tr>
<td>C5</td>
<td>1 μF</td>
<td>C2012X5R1E105K</td>
<td>TDK</td>
<td>SMD 0805</td>
<td>ILED pin filtering</td>
</tr>
<tr>
<td>C6</td>
<td>10 μF</td>
<td>C2012X5R0J106M</td>
<td>TDK</td>
<td>SMD 0805</td>
<td>( C_{C} ) - compensation network</td>
</tr>
<tr>
<td>C7</td>
<td>1 nF</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( C_{P} ) - compensation network</td>
</tr>
<tr>
<td>C8</td>
<td>100 nF/25 V</td>
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<td></td>
<td>SMD 0805</td>
<td>( V_{CC} ) filter capacitor</td>
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<tr>
<td>C9</td>
<td>NC</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>CS pin filtering</td>
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<tr>
<td>C10</td>
<td>1500 pF</td>
<td>DE1E3KX152MN5A</td>
<td>Murata</td>
<td></td>
<td>Y2 capacitor</td>
</tr>
<tr>
<td>C12A</td>
<td>330 μF/35 V</td>
<td>B41888C7337M</td>
<td>EPCOS</td>
<td>RADIAL 10 x 16</td>
<td>Output capacitor</td>
</tr>
<tr>
<td>C13</td>
<td>NC</td>
<td></td>
<td></td>
<td>SMD 1206</td>
<td>Output MLCC capacitor</td>
</tr>
<tr>
<td>C14</td>
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<td></td>
<td></td>
<td>SMD 1206</td>
<td>Output MLCC capacitor</td>
</tr>
<tr>
<td>C15</td>
<td>330 μF/35 V</td>
<td>B41888C7337M</td>
<td>EPCOS</td>
<td>RADIAL 10 x 16</td>
<td>Output capacitor</td>
</tr>
<tr>
<td>C16</td>
<td>330 μF/35 V</td>
<td>B41888C7337M</td>
<td>EPCOS</td>
<td>RADIAL 10 x 16</td>
<td>Output capacitor</td>
</tr>
<tr>
<td>C17</td>
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<td></td>
<td>SMD 1206</td>
<td>Output MLCC capacitor</td>
</tr>
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<td>C18</td>
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<td></td>
<td>SMD 1206</td>
<td>Output MLCC capacitor</td>
</tr>
<tr>
<td>D1</td>
<td>1 A/600 V</td>
<td>STTH1L06</td>
<td>STMicroelectronics®</td>
<td>SMB FLAT</td>
<td>Snubber diode</td>
</tr>
<tr>
<td>D2</td>
<td>1 N4148</td>
<td></td>
<td></td>
<td>SOD-123</td>
<td>Self-supply diode</td>
</tr>
<tr>
<td>D3</td>
<td>3 A/150 V</td>
<td>STPS3150UF</td>
<td>STMicroelectronics</td>
<td>SMB FLAT</td>
<td>Output filter diode</td>
</tr>
<tr>
<td>D4</td>
<td>1 N4148</td>
<td></td>
<td></td>
<td>SOD-123</td>
<td>PF network diode</td>
</tr>
<tr>
<td>F1</td>
<td>1 A -250 V</td>
<td>MCMSF 1 A 250 V</td>
<td>MULTICOMP</td>
<td>DIP 4 x 8</td>
<td>Input fuse</td>
</tr>
<tr>
<td>L1</td>
<td>1.5 mH</td>
<td>B82145A1155J000</td>
<td>EPCOS</td>
<td>DIP 6.5 x 12</td>
<td>Input inductor</td>
</tr>
<tr>
<td>R1</td>
<td>330 kΩ</td>
<td></td>
<td></td>
<td>SMD 1206</td>
<td>Snubber resistor</td>
</tr>
<tr>
<td>R2</td>
<td>2.2 Ω - 1%</td>
<td></td>
<td></td>
<td>SMD 1206</td>
<td>( R_{SENSE} ) resistor</td>
</tr>
<tr>
<td>R3</td>
<td>15 Ω - 1%</td>
<td></td>
<td></td>
<td>SMD 1206</td>
<td>( R_{SENSE} ) resistor</td>
</tr>
<tr>
<td>R4</td>
<td>1 kΩ - 1 %</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( R_{CS} ) resistor</td>
</tr>
<tr>
<td>R5</td>
<td>17.3 kΩ - 1%</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( R_{FB} ) resistor</td>
</tr>
<tr>
<td>R6</td>
<td>56 kΩ - 1%</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( R_{DF} ) resistor</td>
</tr>
<tr>
<td>R7</td>
<td>220 Ω</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( R_{C} ) compensation network</td>
</tr>
<tr>
<td>R8</td>
<td>82 kΩ - 1%</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( R_{DMG} ) resistor</td>
</tr>
<tr>
<td>R9</td>
<td>2.2 Ω</td>
<td></td>
<td></td>
<td>SMD 0805</td>
<td>( V_{CC} ) filtering</td>
</tr>
<tr>
<td>R10</td>
<td>0 Ω</td>
<td></td>
<td></td>
<td>SMD 0603</td>
<td>Optional</td>
</tr>
<tr>
<td>R11</td>
<td>NC</td>
<td></td>
<td></td>
<td>SMD 0603</td>
<td>Optional</td>
</tr>
<tr>
<td>Ref.</td>
<td>Value</td>
<td>Part number</td>
<td>Vendor</td>
<td>Package</td>
<td>Description</td>
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<tr>
<td>------</td>
<td>-----------</td>
<td>--------------</td>
<td>--------------</td>
<td>-----------</td>
<td>------------------</td>
</tr>
<tr>
<td>R12</td>
<td>6.8 kΩ</td>
<td></td>
<td>SMD 0805</td>
<td>Minimum load</td>
<td></td>
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<tr>
<td>R13</td>
<td>6.8 kΩ</td>
<td></td>
<td>SMD 0805</td>
<td>Minimum load</td>
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</tr>
<tr>
<td>R14</td>
<td>62 kΩ - 1%</td>
<td></td>
<td>SMD 0805</td>
<td>ROS resistor</td>
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<tr>
<td>T1</td>
<td>SRW13EP-XxxH003</td>
<td>TDK</td>
<td>TROUGH HOLE 10-pin</td>
<td>Flyback transformer</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>HVLED815PF</td>
<td>STMicroelectronics</td>
<td>SO-16</td>
<td>IC with integrated MOS</td>
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</table>
4 Transformer specifications

Figure 8. Transformer specifications

<table>
<thead>
<tr>
<th>[1] 外観及び寸法</th>
<th>APPEARANCE &amp; DIMENSIONS</th>
<th>(UNIT: mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A: 17.5 mm MAX</td>
<td>B: 17.0 mm MAX</td>
<td>C: 15.5 mm MAX</td>
</tr>
<tr>
<td>D: 3.3±0.5 mm</td>
<td>E: 3.0±0.5 mm</td>
<td>F: 11.0±0.5 mm</td>
</tr>
<tr>
<td>d: 0.6±0.1 mm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All products are fixed with the adhesive.

Safety standards

Over Surface & Air Spaces

Minimum 2.5mm

Minimum 2.5mm

Winding specification

PIN 2, 7, 8, 9 should be pulled off

AL-Value=00dc/#2 (Z=4) (GAP: R20)

<table>
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<tr>
<th>No.</th>
<th>COIL</th>
<th>TERMINAL</th>
<th>TURNS</th>
<th>WIRE</th>
<th>method</th>
<th>25Ux8.0</th>
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<tr>
<td>1</td>
<td>N P1</td>
<td>1-3</td>
<td>125</td>
<td>TPEW 0.14</td>
<td>FIT-SPACE</td>
<td>1.27TS</td>
</tr>
<tr>
<td>2</td>
<td>N S</td>
<td>6-10</td>
<td>35</td>
<td>TPEW 0.30</td>
<td>FIT-SPACE</td>
<td>1.2TS</td>
</tr>
<tr>
<td>3</td>
<td>N aux</td>
<td>4-5</td>
<td>19</td>
<td>TPEW 0.14</td>
<td>SPACE</td>
<td>2.2TS</td>
</tr>
</tbody>
</table>

Lp 1-3 = (1 MHz Ref)±10% at10kHz/IV, Le 5-3 = ---μH MAX (Sec shorted) at10kHz/IV

Planar

P-S: 150, 60Vrms 1s 2mA
P-CORE: 150, 60Vrms 1s 2mA
S-CORE: 150, 60Vrms 1s 2mA

IR: P-S, P-S-CORE 100 IMD MIN at DC 50V

Approved | Checked | Designed | Customer | ST |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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<tr>
<td>周小波</td>
<td>MODEL</td>
<td>SRW13EP-XxxH003</td>
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<td>2013/6/4</td>
<td>DWG. No.</td>
<td>X11725</td>
<td>ISSUE</td>
<td>6</td>
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</tbody>
</table>
5 PCB layout

Figure 9. PCB layout - top side

Figure 10. PCB layout - bottom side
6 Test results

From Figure 11 to Figure 18 are shown the main results of the demonstration boards at nominal line input voltage (230 Vac).

6.1 Efficiency

System efficiency is higher than 80% starting from 20% of the rated maximum load (about 70 mA) and it increases up to 88% at the maximum load.

![Figure 11. System efficiency](image)

6.2 Power factor

The power factor is higher than 0.75 starting from 20% of the rated maximum load (about 70 mA) and increases up to 0.95 at maximum load.
6.3 Standby power dissipation

The power consumption of the demonstration board in standby condition (no load) is below 300 mW.
6.4 Line regulation

The average output voltage is regulated within ± 0.8% from no load to full load.

Figure 14. Line regulation

6.5 Harmonic distortion

The demonstration board respects the EC61000-3-2 Class D specification.

Figure 15. Harmonic distortion at 310 mA
Figure 16. Harmonic distortion at 275 mA

Figure 17. Harmonic distortion at 200 mA

Figure 18. Harmonic distortion at 135 mA
6.6 Thermal measurement

All component temperatures are below 50 °C - a thermal test has been performed at ambient temperature (25 °C).

![Figure 19. Thermal test - top side](image)

<table>
<thead>
<tr>
<th>Label</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Input capacitor (C1)</td>
</tr>
<tr>
<td>B</td>
<td>Input inductor</td>
</tr>
<tr>
<td>C</td>
<td>Input capacitor (C2)</td>
</tr>
<tr>
<td>D</td>
<td>Transformer</td>
</tr>
<tr>
<td>E</td>
<td>Output capacitor</td>
</tr>
</tbody>
</table>
Figure 20. Thermal test - bottom side

Table 3. Thermal test - bottom side

<table>
<thead>
<tr>
<th>Label</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Bridge diode</td>
</tr>
<tr>
<td>B</td>
<td>IC (HVLED815PF)</td>
</tr>
<tr>
<td>C</td>
<td>Snubber</td>
</tr>
<tr>
<td>D</td>
<td>Output diode</td>
</tr>
</tbody>
</table>
6.7 Waveforms

Figure 21. MOSFET current at $I_{\text{OUT}}^{\text{max}}$

CH1 (brown): rectified input voltage
CH2 (purple): MOSFET drain
CH3 (blue): MOSFET source

Figure 22. MOSFET current at $I_{\text{OUT}}^{\text{max}/2}$

CH1 (brown): rectified input voltage
CH2 (purple): MOSFET drain
CH3 (blue): MOSFET source
Figure 23. Steady-state condition

CH3 (blue): output voltage
CH4 (green): input current

Figure 24. Startup at $I_{\text{OUT}}^{\text{max}}$

CH1 (brown): rectified input voltage
CH3 (blue): MOSFET source
CH4 (green): output voltage
Figure 25.Shutdown at $I_{\text{OUT}}^{\text{max}}$

CH1 (brown): rectified input voltage
CH3 (blue): MOSFET source
CH4 (green): output voltage

Figure 26. COMP pin at $I_{\text{OUT}}^{\text{max}}$

CH1 (brown): COMP pin
CH2 (purple): CS pin
CH3 (blue): VCC pin
Figure 27. Switching frequency at $I_{OUT}^{max}$

CH1 (brown): rectified input voltage (on the peak)
CH2 (purple: MOSFET source
CH3 (blue): MOSFET drain
7 Electromagnetic compatibility

The demonstration board meets the EN55015 - average limits.

Figure 28. EMI
8 Supporting material

Documentation

- ST HVLED815PF datasheet, “Offline LED driver with primary-sensing and high power factor up to 15 W”
- ST AN1059, “Design equations of high-power-factor flyback converters based on the L6561”
- ST AN1262, “Offline flyback converters design methodology with the L6590 family”.

9 Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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</thead>
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<tr>
<td>10-Feb-2014</td>
<td>1</td>
<td>Initial release.</td>
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