Introduction

This application note is intended to provide additional information and suggestions for the correct use of the LNBH23 device. All waveforms shown are based on the demonstration board (order code STEVAL-CBL003V1) described in Section 5.

The LNBH23 is an integrated solution for supplying/interfacing satellite LNB modules. It provides good performance in a simply and cheaply way, with minimum external components necessary. It includes all functions needed for LNB supply and interfacing, in accordance with international standards. Moreover, it includes an I²C bus interface and, thanks to a fully integrated step-up DC-DC converter, it functions with a single input voltage supply ranging from 8 V to 15 V.

Figure 1. LNBH23 internal block diagram
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<td>38</td>
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</tbody>
</table>
1 **Block diagram description**

The internal blocks of the LNBH23 are described in the paragraphs that follow.

1.1 **Step-up controller**

The LNBH23 features a built-in step-up DC-DC converter that, from a single supply source ranging from 8 V to 15 V, generates the voltages that allow the linear post-regulator to work with minimum power dissipation. The external components of the DC-DC converter are connected to the Lx and VUP pins (see Figure 5). No external power MOSFET is needed.

1.2 **Pre-regulator block**

This block includes a voltage reference connected to the BYP pin, an undervoltage lockout circuit, intended to disable the whole circuit when the supplied Vcc drops below a fixed threshold (6.7 V typ) and a power-on reset that sets all the I²C registers to zero when the Vcc is turned on and rises from zero above the on threshold (7.3 V typ).

1.3 **I²C interface and diagnostics**

The main functions of the device are controlled via I²C bus by writing 5 bits on the system register (SR bits in write mode). In the same register there are 5 bits that can be read back (SR bits in read mode) and provide 5 diagnostic functions.

Five bits report the diagnostic status of five internal monitoring functions:
- VMON: output voltage diagnostic. If the output voltage level is below the guaranteed limit (refer to the device datasheet) the VMON I²C bit is set to “1”.
- TMON: 22 kHz tone diagnostic. If the 22 kHz tone amplitude and/or the tone frequency is outside of the guaranteed limits (refer to the device datasheet.), the TMON I²C bit is set to “1”.
- IMON: minimum output current diagnostic to detect if no LNB is connected on the bus or a cable not connected to the IRD. The LNBH23 is provided with a minimum output current flag by the IMON I²C bit in read mode, which is set to “1” if the output current is lower than 12 mA (typ) with ITEST=1 and 6 mA with ITEST=0.
- OTF: overtemperature flag. If overheating occurs (junction temperature exceeds 150 °C), the OTF I²C bit is set to “1”.
- OLF: overload flag. If the output current required exceeds the current limit threshold or a short-circuit occurs, the OLF I²C bit is set to “1”.

Moreover, three bits will report the last output voltage register status (EN, VSEL, LLC) received by the IC. The LNBH23 I²C interface address can be selected among two different addresses by setting the voltage level of the dedicated ADDR pin.
1.4 22 kHz oscillator and EXTM function

The internal 22 kHz tone generator is factory-trimmed in accordance with current standards and can be controlled by the DSQIN pin (TTL-compatible), which allows immediate DiSEqC™ data encoding. The rising and falling edges are kept within the 5 µs to 15 µs range, 8 µs (typ) for 22 kHz. The duty cycle is 50% (typ), and modulates the DC output with a 0.650 Vpp (typ) amplitude as well as the DSQIN pin.

The EXTM is a logic input to allow the activation of the 22 kHz tone output, on the $V_{oT_x}$ pin, by using the device's integrated tone generator. If the EXTM pin is used, the internal 22 kHz generator must be kept ON (TTX pin or TTX bit set HIGH). When a TTL-compatible 22 kHz signal is applied (for example, a 22 kHz square wave from the demodulator), the EXTM internal circuit detects the 22 kHz TTL signal code and activates the internal 22 kHz tone on the $V_{oT_x}$ output. The 22 kHz tone on the output is activated after a delay from the TTL signal presence on the EXTM pin. The tone output starts with about a 1.5 T delay after the 1st cycle of the TTL signal and stops after about a 2 T delay after the TTL signal on the EXTM has expired (see Figure 2 below). The tone output can also be activated via the DSQIN pin. It starts with a 1.5 T ± 25 µs maximum delay and stops after 2 T ± 25 µs maximum delay with 20–24 kHz tolerance for EXTM input pin.

Figure 2. EXTM timing control

1.5 Tone detector

This block provides a complete circuit to decode the 22 kHz burst code present on the DETIN pin in a digital signal by the DSQOUT pin where an open drain MOSFET is connected. The tone is also monitored and a dedicated bit (TMON) provides the diagnostic function described in the Section 1.3.
1.6 DiSEqC communication

The following steps must be taken to ensure the correct implementation of the DiSEqC 2.0 communication:

- **T0**: before starting the DiSEqC transmission, the TTX function must be activated (through the TTX pin or TTX I²C bit).
- **T1**: after a 500 µs minimum, the IC is ready to receive the DiSEqC code through the DSQIN pin (or, alternatively, the TEN I²C bit can be set to HIGH to activate the 22 kHz burst).
- **T2**: when the transmission has elapsed, the TTX function must be set to LOW (through the TTX pin or TTX I²C bit) not earlier than 200 µs after the last falling edge of the DiSEqC code.

![DiSEqC timing control](image)

1.7 Linear post-regulator, modulator and protection

The output voltage selection and the current selection commands join this block, which manages all the LNB output function. This block gives feedback to the I²C interface, from the diagnostic block, regarding the status of the thermal protection, overcurrent protection and output settings.
# Pin description

The LNBH23 is available in exposed pad PowerSSO-24 or QFN32 packages for surface mount assembly. Figure 4 shows the device pinouts for each package. Table 1 briefly summarizes the pin functionality.

**Figure 4.** LNBH23 pin configuration

![LNBH23 pin configuration](image)

**Table 1.** LNBH23 pin description

<table>
<thead>
<tr>
<th>Pin n° QFN32</th>
<th>Pin n° PSSO-24</th>
<th>Symbol</th>
<th>Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>17</td>
<td>VCC</td>
<td>Supply input</td>
<td>8 to 15 V IC DC-DC power supply</td>
</tr>
<tr>
<td>18</td>
<td>16</td>
<td>VCC–L</td>
<td>Supply input</td>
<td>8 to 15 V analog power supply</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>Lx</td>
<td>NMOS drain</td>
<td>Integrated N-channel power MOSFET drain</td>
</tr>
<tr>
<td>27</td>
<td>22</td>
<td>V_UP</td>
<td>Step-up voltage</td>
<td>Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor</td>
</tr>
<tr>
<td>21</td>
<td>19</td>
<td>V_oRX</td>
<td>LDO output port</td>
<td>Output of the integrated linear post-regulator</td>
</tr>
<tr>
<td>22</td>
<td>20</td>
<td>V_sTX</td>
<td>Output port for 22 kHz tone TX</td>
<td>TX output to the LNB</td>
</tr>
<tr>
<td>6</td>
<td>8</td>
<td>SDA</td>
<td>Serial data</td>
<td>Bi-directional data from/to I²C bus</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>SCL</td>
<td>Serial clock</td>
<td>Clock from I²C bus</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>DSQIN</td>
<td>DiSEqC input</td>
<td>This pin accepts the DiSEqC code from the main microcontroller. The LNBH23 uses this code to modulate the internally-generated 22 kHz carrier. Set this pin to ground if not used</td>
</tr>
</tbody>
</table>
### Table 1. LNBH23 pin description (continued)

<table>
<thead>
<tr>
<th>Pin n°</th>
<th>Pin n°</th>
<th>Symbol</th>
<th>Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>14</td>
<td>TTX</td>
<td>TTX enable</td>
<td>This pin, as well as the TTX I2C bit of the system register, is used to control the TTX function enable before starting the 22 kHz tone transmission. Set this pin to ground if not used</td>
</tr>
<tr>
<td>29</td>
<td>1</td>
<td>DETIN</td>
<td>Tone decoder input</td>
<td>22 kHz tone decoder input, must be AC coupled to the DiSEqC 2.0 bus</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>DSQOUT</td>
<td>DiSEqC output</td>
<td>Open drain output of the tone detector to the main microcontroller for DiSEqC 2.0 data decoding. It is low when a tone is detected on the DETIN pin</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>EXTM</td>
<td>External modulation</td>
<td>External modulation logic input pin which activates the 22 kHz tone output on the VoTX pin. Set to ground if not used</td>
</tr>
<tr>
<td>5</td>
<td>7</td>
<td>P-GND</td>
<td>Power ground</td>
<td>DC-DC converter power ground</td>
</tr>
<tr>
<td>20</td>
<td>18</td>
<td>A-GND</td>
<td>Analog ground</td>
<td>Analog circuits ground</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>BYP</td>
<td>Bypass capacitor</td>
<td>Needed for internal preregulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>ADDR</td>
<td>Address setting</td>
<td>Two I2C bus addresses available by setting the address pin level voltage</td>
</tr>
<tr>
<td>28</td>
<td>23</td>
<td>ISEL</td>
<td>Current selection</td>
<td>The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold with the equation: Imax(typ.)=10000/RSEL</td>
</tr>
<tr>
<td>30</td>
<td>2</td>
<td>VCTRL</td>
<td>Output voltage control</td>
<td>13 V - 18 V linear regulator VoRX switch control. To be used only with VSEL=1. If VCTRL=1 or floating Vout=18.5 V (or 19.5 V if LLC=1). If VCTRL=0 then Vout=13.4 V (LLC=either 0 or 1)</td>
</tr>
<tr>
<td>ePad</td>
<td>ePad</td>
<td>ePad</td>
<td>ePad</td>
<td>On the bottom side of the PowerSSO-24 package. Must be connected with power ground and to the ground layer through vias to dissipate heat</td>
</tr>
</tbody>
</table>
3 Component selection guidelines

The LNBH23 application schematic in Figure 5 shows the typical configuration for a single LNB power supply.

Figure 5. LNB power supply schematic using the LNBH23

Note: TVS diode to be used if surge protection is required (see Section 3.9).

Table 2. LNBH23 demonstration board BOM list

<table>
<thead>
<tr>
<th>Component</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>LNBH23 PSSO-24 ePad for STEVAL-CBL003V1</td>
</tr>
<tr>
<td></td>
<td>LNBH23 QFN32 ePad for STEVAL-CBL005V1</td>
</tr>
<tr>
<td>C1</td>
<td>100 µF 35 V electrolytic capacitor, higher value is suitable</td>
</tr>
<tr>
<td>C3, C5</td>
<td>100 µF 25 V electrolytic capacitor, ESR in the 150 mΩ to 350 mΩ range (see Section 3.3)</td>
</tr>
<tr>
<td>C9</td>
<td>10 µF 35 V electrolytic capacitor</td>
</tr>
<tr>
<td>C2, C7</td>
<td>0.1 µF 35 V ceramic capacitors</td>
</tr>
<tr>
<td>C4, C6</td>
<td>0.47 µF 35 V ceramic capacitors</td>
</tr>
</tbody>
</table>
### 3.1 Input capacitors

An electrolytic bypass capacitor (C1 in *Figure 5*) between 100 µF and 470 µF located close to the LNBH23 is needed for stable operation. In any case, a ceramic capacitor between 100 nF and 470 nF is recommended to reduce the switching noise at the input voltage pin.

### 3.2 Ferrite bead

The most important parameter when selecting the ferrite bead is the rated current. Ensure that the ferrite has a current rating of at least 2 A and impedance higher than 60 Ω at 100 MHz.

### 3.3 DC-DC converter output capacitors

Two low-cost electrolytic capacitors are needed on the DC-DC converter output stage (C3 and C5 in *Figure 5*). Moreover, two ceramic capacitors are recommended to reduce high frequency switching noise. The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To minimize these voltage spikes, special low-inductance ceramic capacitors can be used, and their lead lengths must be kept short and as close as possible to the IC pins (C4 and C6 in *Figure 5*). To further reduce switching noise, a ferrite bead is recommended between the capacitors (see *Section 3.2* for required rating and impedance).
The most important parameter for the output capacitors is the effective series resistance (ESR). The DC-DC converter control loop circuit has been designed to work properly with low-cost electrolytic capacitors which have ESR in the range of 200 mΩ. A 100 µF output filter capacitor with ESR between 150 mΩ and 350 mΩ is a good choice in most application conditions. It is also possible to use electrolytic capacitors up to 220 µF with ESR between 100 mΩ and 300 mΩ. The capacitor voltage rating must be at least 25 V, but if the highest voltage selection condition is used (AUX=1), 35 V or higher voltage capacitors are suggested.

### 3.4 DC-DC converter Schottky diode

In typical application conditions it is beneficial to use a 1 A Schottky diode which is suitable for the LNBH23 DC-DC converter. Taking into consideration that the DC-DC converter Schottky diode must be selected depending on the application conditions ($V_{RRM} > 25$ V), an N-channel Schottky diode like the STPS130A is recommended.

The average current flowing through the Schottky diode is lower than $I_{PEAK}$ and can be calculated using **Equation 1**. In worst-case conditions, such as low input voltage and higher output current, a Schottky diode capable of supporting the $I_{PEAK}$ should be selected. $I_{PEAK}$ can be calculated using **Equation 2**.

**Equation 1**

$$I_d = I_{out} \cdot \frac{V_{out}}{V_{in}}$$

**Table 3. Recommended Schottky diode**

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part number</th>
<th>$I_{F(av)}$</th>
<th>$V_{F(max)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>STMicroelectronics</td>
<td>1N5818</td>
<td>1 A</td>
<td>0.50 V</td>
</tr>
<tr>
<td></td>
<td>1N5819</td>
<td>1 A</td>
<td>0.55 V</td>
</tr>
<tr>
<td></td>
<td>STPS130A</td>
<td>1 A</td>
<td>0.46 V</td>
</tr>
<tr>
<td></td>
<td>STPS1L30A</td>
<td>1 A</td>
<td>0.30 V</td>
</tr>
<tr>
<td></td>
<td>STPS2L30A</td>
<td>2 A</td>
<td>0.45 V</td>
</tr>
<tr>
<td></td>
<td>1N5822</td>
<td>3 A</td>
<td>0.52 V</td>
</tr>
<tr>
<td></td>
<td>STPS340</td>
<td>3 A</td>
<td>0.63 V</td>
</tr>
<tr>
<td></td>
<td>STPS3L40A</td>
<td>3 A</td>
<td>0.5 V</td>
</tr>
</tbody>
</table>

### 3.5 DC-DC converter inductor

The LNBH23 operates with a standard 22 µH inductor for the entire range of supply voltages and load current. The inductor saturation current rating (where inductance is approximately 70% of zero current inductance) must be greater than the switch peak current ($I_{PEAK}$) calculated at:

- maximum load ($I_{out_{max}}$)
- minimum input voltage ($V_{in_{min}}$)
- maximum DC-DC output voltage ($V_{UP_{max}} = V_{out_{max}} + 0.75$ V)
In this condition the switch peak current is calculated using the formula in \textit{Equation 2}.

\textbf{Equation 2}

\[
I_{\text{peak}} = \frac{V_{\text{UP max}} \cdot I_{\text{out max}}}{\text{Eff} \cdot V_{\text{in min}}} + \frac{V_{\text{in min}}}{2LF \left( 1 - \frac{V_{\text{in min}}}{V_{\text{UP max}}} \right)}
\]

where

- Eff is the efficiency of the DC-DC converter (93\% typ. at highest load)
- L is the inductance (22 \(\mu\)H typ.)
- F is the PWM frequency (220 kHz typ.).

\textbf{Example}:

Application conditions:

- \(V_{\text{out max}}= 19.2\) V (supposing EN=VSEL=1, LLC=0)
- \(V_{\text{in min}}= 11\) V
- \(V_{\text{UP max}}=V_{\text{out max}}+V_{\text{drop}}= 19.2\) V+0.75 V= 19.95 V
- \(I_{\text{out max}}= 500\) mA
- Eff=90\%

Based on \textit{Equation 2} and the preceding application conditions, \(I_{\text{PEAK}}\) is:

\textbf{Equation 3}

\[
I_{\text{peak}} = \frac{19.95 \cdot 0.5}{0.9 \cdot 11} + \frac{11}{2 \cdot 22 \cdot 10^{-6} \cdot 220 \cdot 10^{3} \left( 1 - \frac{11}{19.95} \right)} = 1.52 \text{ A}
\]

Several inductors suitable for the LNBH23 are listed in the \textit{Table 4}, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, since many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the \(I_{\text{PEAK}}\) current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize power losses and, consequently, to maximize total efficiency.

\textbf{Table 4. Recommended inductors}

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part number</th>
<th>Isat(A)</th>
<th>DRC (m(\Omega))</th>
<th>Mounting type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sumida</td>
<td>CD104-220MC</td>
<td>1.6</td>
<td>67</td>
<td>SMD</td>
</tr>
<tr>
<td></td>
<td>RHC110-220M</td>
<td>2.4</td>
<td>88</td>
<td>Through-hole</td>
</tr>
<tr>
<td>Toko</td>
<td>822LY-220K</td>
<td>1.3</td>
<td>70</td>
<td>Through-hole</td>
</tr>
<tr>
<td></td>
<td>824LY-220K</td>
<td>1.72</td>
<td>76</td>
<td>Through-hole</td>
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<tr>
<td></td>
<td>A671HN-220L</td>
<td>2.44</td>
<td>21</td>
<td>Through-hole</td>
</tr>
<tr>
<td></td>
<td>A814LY-220M</td>
<td>2.0</td>
<td>75</td>
<td>SMD</td>
</tr>
</tbody>
</table>
3.6 Output current limit-$R_{SEL}$ selection

The linear regulator current limit threshold can be set through an external resistor connected to ISEL pin. The resistor value defines the output current limit using the equation:

\[ I_{\text{max}}(A) = \frac{10000}{R_{\text{SEL}}} \]

where $R_{\text{SEL}}$ is the resistor connected between the ISEL pin and GND. The highest selectable current limit threshold is 1.0 A (typ) with $R_{\text{SEL}}=10 \text{ k}\Omega$.

3.7 Undervoltage diode protection

During a short-circuit removal on the LNB output, negative voltage spikes may occur on the $V_{\text{OTX}}$ and $V_{\text{ORX}}$ pins. To prevent reliability problems, two low-cost Schottky diodes are used between those pins and GND (see D2 and D4 in Figure 5).

3.8 DiSEqC implementation and inductor selection

To comply with DiSEqC 2.x requirements, an output R-L filter is needed. The 22 kHz tone transmission occurs through the $V_{\text{OTX}}$ pin, whereas the DC voltage is provided from the $V_{\text{ORX}}$ pin. The $V_{\text{OTX}}$ function must be activated only during the tone transmission while the $V_{\text{ORX}}$ provides the 13/18 V output voltage. This solution allows the 22 kHz tone to pass without any losses due to the R-L filter impedance. But to respect the minimum DC voltage requirement, it is recommended to use an inductor with a current rating higher than the rated output current and a low DRC to minimize the voltage drop.

For example, supposing:
- $I_{\text{out}} = 500 \text{ mA}$
- $DRC=51 \text{ m}\Omega$ (Panasonic inductor ELC08D221E)

\[ V_{\text{drop}}(V) = DCR(\Omega) \cdot I_{\text{out}}(A) = 0.051 \cdot 0.5 = 0.025 \text{ V} \]

Several inductors suitable for the LNBH23 are listed in the Table 5.
3.9 **TVS diode**

The LNBH23 device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. LNBH23 devices are not able to withstand such high energy discharges, so transient voltage suppressor (TVS) devices are used to protect the LNBH23 and other devices electrically connected to the antenna cable.

The LNBTVS developed by STMicroelectronics is a dedicated lightning and electrical overstress surge protection device for LNB voltage regulators. These protection devices are designed to comply with the stringent IEC 61000-4-5 standards and to withstand surges of up to 500 A. ST offers a broad selection of these products for cost/performance optimization.

The selection of the TVS diode must be made based on the maximum peak power dissipation that the diode is capable of supporting.

### Table 6. **Recommended LNBTVS**

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part number</th>
<th>VBR&lt;sub&gt;TYP&lt;/sub&gt;(V)</th>
<th>Ppp(W)10/100µs</th>
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<tr>
<td>STMicroelectronics</td>
<td>LNBTVS4-220</td>
<td>23.1</td>
<td>1800</td>
</tr>
<tr>
<td></td>
<td>LNBTVS4-221</td>
<td>23.1</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>LNBTVS4-222S</td>
<td>23.1</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>LNBTVS6-221S</td>
<td>21.3</td>
<td>3000</td>
</tr>
</tbody>
</table>

Select the TVS diode which is capable of supporting the required Ppp(W) value indicated in **Table 6**.
4 Other application circuits

The following paragraphs present two particular application solutions: the first can be used to reduce the 18 V to 13 V transition time, while the second is designed to improve lightning surge protection.

4.1 18 V to 13 V fast transition with high bus capacitance

In cases of very high bus capacitance (Cbus>10 µF) and very low output current, an external circuit (with a 4.7 V Zener diode and a 100 Ω series resistor) can be added to reduce 18 V to 13 V transition fall time, as shown in Figure 6.

The TTX bit (or pin) must be set high only during the transition from 18 V to 13 V. The TTX function activates only the push-pull circuit, but not the tone output. The 22 kHz tone is activated only when the TEN bit (or DSQIN pin) is also set high and injected into the LNB bus through the 10 µF capacitor.

When the TTX function is activated, the V_{o\text{TX}} voltage is internally set at 5 V (typ), below the Vout (for example, if Vout=18 V then V_{o\text{TX}}=18-5=13 V) and, at the same time, the P-channel is enabled to sink current (note: the P-channel is internally current-limited).

With a 4.7 V Zener diode, when TTX=high, the current through the Zener is: I_z=(5-4.7)/100=3 mA. If TTX=low, the current through the Zener is negligible.

If there is a high output capacitance present, during the transition from 18 V to 13 V (with TTX=high), the voltage drop (Vout-V_{o\text{TX}}) is increased because the V_{o\text{TX}} goes quickly to low level (at 13 V-5 V=8 V) and, consequently, the Zener current is also increased until the output capacitance is discharged to 13 V. For example, with 100 µF on the output, the 18 V to 13 V fall time is about 25 ms.
The following steps must be taken to ensure the correct implementation of 18 to 13 V transition with the $V_{\text{OTx}}$ addition circuit shown in Figure 6:

- **T0**: to start the 18 V to 13 V transition the TTX function must be activated at least 0.5 ms before setting the VSEL I\(^2\)C bit (set HIGH TTX I\(^2\)C bit or TTX pin).
- **T1**: set LOW VSEL I\(^2\)C bit.
- **T2**: after 30 ms, 18 V to 13 V LNB transition time is elapsed at T2. The 30 ms delay is valid to ensure 18 V to 13 V complete transition in case of $C_{\text{bus}}=100 \ \mu\text{F}$ and $I_{\text{out}}=0 \ \text{mA}$. The delay time can be modified with different $C_{\text{bus}}$ capacitance and output current value.

**Figure 7. Fast transition timing sequence**
If the internal 22 kHz tone generator is activated (TEN I²C bit or DSQIN pin is set high), at T1 set low the VSEL I²C bit or VCTRL pin and after 25 ms, 18 V to 13 V LNB transition time is elapsed at T2.

4.2 Reverse voltage and lightning surge protection

Figure 9 shows a suggested schematic to improve output circuit protection in applications where:

- TVS diode with Vclamp voltage of 25 V is required
- An external power supply source could force a reverse DC voltage of 25 V on the LNB bus
The Schottky diode prevents the reverse voltage from flowing into the $V_{\text{out}}$ pin (internally connected to the linear regulator). In applications where a reverse DC voltage (up to 60 V) is forced and low $V_{\text{out}}$ tolerance is required, the recommended part number is STPS3L60U. In any case, it is possible to use a different part based to the DC reverse voltage. $D_3$ shields the $V_{\text{out}}$ pin because it discharges the reverse voltage into the $V_{\text{up}}$ capacitor and $D_{4c}$ (suggested part number SM2T18A) is mandatory for DC reverse voltage $\geq 25$ V.
5 Layout guidelines

Due to high current levels and fast switching waveforms, which radiate noise, a proper printed circuit board (PCB) layout is essential. Sensitive analog grounds can be protected by using a star ground configuration. Also, lead lengths should be minimized to reduce stray capacitance, trace resistance, and radiated noise. Ground noise can be minimized by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Place input bypass capacitors (C1, C2, C7 and C8) as close as possible to Vcc and GND, and the DC-DC output capacitors (C3, C4, C5 and C6) as close as possible to VUP. Excessive noise at the Vcc input may falsely trigger the undervoltage circuitry, resetting the I²C internal registers. If this occurs, the registers are set to zero and the LNBH23 is put into shutdown mode.

LNB power supply demonstration boards are available for each package option through order codes STEVAL-CBL003V1 (Figure 10) and STEVAL-CBL005V1 (Figure 11).

Figure 10. STEVAL-CBL003V1 demonstration board photo (PowerSSO-24 package)

Figure 11. STEVAL-CBL005V1 demonstration board photo (QFN32 package)
5.1 PCB layout

Any switch mode power supply requires a good PCB layout in order to achieve maximum performance. Component placement, and GND trace routing and width are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed.

All traces carrying current should be drawn on the PCB as short and as thick as possible. This should be done to minimize resistive and inductive parasitic effects, and increase system efficiency.

White arrows indicate the suggested PCB (ring) ground plane to avoid spikes on the output voltage (this is related to the switching side of the LNBH23). Good soldering of the ePad helps on this issue.

Figure 12. STEVAL-CBL003V1 PCB top layer

![PCB Top Layer](image1)

Figure 13. STEVAL-CBL003V1 PCB bottom layer

![PCB Bottom Layer](image2)
Figure 14. STEVAL-CBL003V1 component layout

Figure 15. STEVAL-CBL005V1 PCB top layer
5.2 Startup procedure

Testing the demonstration board requires a PC with a parallel port (ECP printer port), an \( ^2 \)C bus interface, software (LNBxxx control suite), a dual-output power supply (3 A clamp current or higher) and an electronic load.

- Step 1: Install the LNBXXX control suite software (see Section 6).
- Step 2: Plug the \( ^2 \)C connector into CN5.
- Step 3: Supply the demonstration board through CN2.
- Step 4: Refer to Section 6.1 of software installation guide to use the software.
Figure 18. STEVAL-CBL003V1 connectors

CN2
To supply the demonstration board (Typ. 12 VDC) Use a power supply with a 3 A clamp current or higher

CN3
To supply LNB VoTX=Vout test point

CN1
ADDR tip: Connect ADDR pin to ground to set I²C address = 02

CN5
I²C interface connections: For data transmissions from the I²C interface to the LNBH23 and vice-versa. Care should be taken to ensure proper connection of the I²C interface

Figure 19. STEVAL-CBL005V1 connectors

CN1
To supply the demo board (Typ. 12 VDC) Use a power supply with a 3 A clamp current or higher

CN6
To supply LNB VoTX=Vout test point

CN2
ADDR tip: Connect ADDR pin to ground to set I²C address = 02

CN3
I²C interface connections: For data transmissions from the I²C interface to the LNBH23 and vice-versa. Care should be taken to ensure proper connection of the I²C interface
Figure 20. STEVAL-CBL003V1 bench test

Figure 21. STEVAL-CBL005V1 bench test
6 Software installation

Unzip the compressed file and perform the installation by clicking on the SETUP.exe file. Click on: Windows® “start” menu -> Program -> STMicroelectronics -> LNBxxx control suite. The screen shown in Figure 22 appears, with a green light indicating that the hardware and software are ready to work.

Figure 22. PC to I²C main window

The red “I²C ERROR” indicator signals that the LPT port needs to be configured, and/or the I²C cable (swap the SCL and SDA, if needed) and power supply need to be checked.
The user can choose the device, printer port address for the PC and correct settings of the SCL and SDA bits to customize the I\(^2\)C hardware interface.

In the system setting menu, the device to be tested can be changed.
From the parallel port setting menu, the LPT parameters can be set.

Figure 25. Device selection window

Figure 26. Parallel port setting
At this point, the device address can be chosen. For the LNBH23, only $02= ADDR pin force to GND or $03= ADDR pin force to +5 V can be selected.
To obtain the status of the received bits in real-time, the "Auto read" checkbox must be checked.

Figure 30. Autoread setting
6.1 How to use the LNBH23 demonstration board with the LNBxxx control suite software

To power the IC, place a check in the EN checkbox and click the “Send I2C Pattern” button. If the device accepts the command string, the green indicator turns on. If there is no powerup after sending the command, it may be that the 12 V power supply is not sufficient to start the application, and more current capability is needed.

The screenshot in Figure 31 shows the following conditions:
- EN=1=ON
- Vout=13.4 V_{typ}

Figure 31. Power-on at 13.4 V

A status light “on” for OLF, OTF, TMON, VMON and IMON indicates that an error has occurred.
The screenshot in Figure 32 shows the following conditions:

- $EN=1$, $VSEl=1$
- $V_{out}=18.5\ V_{typ}$

**Figure 32.** Power-on at 18.5 V
The screenshot in Figure 33 shows the following conditions:

- EN=1, VSEL=1, LLC=1
- Vout=19.5 V_{typ}

Figure 33. LLC activation
The screenshot in Figure 34 shows the following conditions:

- EN=1, TEN=TTX=1
- Vout=13.4 \( V_{\text{typ}} \) + 22 kHz tone

**Figure 34. Tone activation**

For 22 kHz tone, TEN and TTX bits must be selected.
Overload condition

If the OLF (overload flag) indicator is on, a fault condition on the output has been detected and the status of this bit is changed. It turns off when the fault condition is removed.

- \( EN=1 \)
- \( V_{out}=\text{fault}, \ OLF=1 \)

**Figure 35. Overload detection**

The screenshot in **Figure 36** shows the following conditions:

- \( EN=1 \)
- \( V_{out}=\text{fault}, \ OTF=1 \)

**Figure 36. Overtemperature detection**
If the PCL checkbox is checked, a simple output short-circuit current clamp is set. If not, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for 90 ms (typ.), after which the output is set in shutdown for a time TOFF of 900 ms (typ). Simultaneously, the diagnostic OLF \( I^2C \) bit of the system register is set high. This feature allows the reduction of the total power dissipation during an overload or a short-circuit condition:

- EN=1, PCL=1
- Vout=13.4 V\(_{typ}\)

Figure 37. PCL deactivation
The AUX bit can be set high to force the LNBH23 output voltage to the highest voltage on the line (22 V typ.) during the minimum current diagnostic phase, in order to detect the output load and check the dish status or any optional devices inserted on the line.

The maximum current detected at ITEST=0 is 6 mA, while at ITEST=1 it is 12 mA.

During the minimum diagnostic current test, setting only EN=ITEST=AUX=1 is recommended. The screenshot in Figure 38 shows the following conditions:

- EN=1, AUX=1
- Vout=22 V (for testing multiswitch-box dish connection)

Figure 38. AUX activation
## 7 Revision history

Table 7. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
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<tbody>
<tr>
<td>13-Nov-2009</td>
<td>1</td>
<td>Initial release.</td>
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