Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use STM32L1xxx product families and describes the minimum hardware resources required to develop an STM32L1xxx application.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

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1 Glossary

- **Medium-density devices** are microcontrollers where the Flash memory ranges between 32 and 128 Kbytes.
- **Medium-density + devices** are microcontrollers where the Flash memory is 256 Kbytes.
- **High-density devices** are microcontrollers where the Flash memory is 384 Kbytes.
2 Power supplies

2.1 Introduction

Digital power voltage ($V_{\text{CORE}}$) is provided with an embedded linear voltage regulator with three different programmable ranges from 1.2 to 1.8 V.

To be fully functional at full speed, the device requires a 2.0 to 3.6 V operating voltage supply ($V_{\text{DD}}$), making possible to reach the digital power voltage $V_{\text{CORE}}$ of 1.8 V (product voltage range 1).

Product voltage range 2 ($V_{\text{CORE}} = 1.5$ V) and 3 ($V_{\text{CORE}} = 1.2$ V) can be selected when the $V_{\text{DD}}$ operates from 1.65 to 3.6 V. Therefore, frequency is limited to 16 MHz and 4 MHz respectively.

When the ADC and brownout reset (BOR) are not used, the device can operate at power voltages below 1.8 V down to 1.65 V.

Figure 1. Power supply overview

Note: $V_{\text{DDA}}$ and $V_{\text{SSA}}$ must be connected to $V_{\text{DD}}$ and $V_{SS}$, respectively.
2.1.1 Independent A/D converter supply and reference voltage

To improve conversion accuracy, the ADC and the DAC have an independent power supply that can be filtered separately, and shielded from noise on the PCB.

- The ADC voltage supply input is available on a separate $V_{DDA}$ pin
- An isolated supply ground connection is provided on the $V_{SSA}$ pin

$V_{DDA}$ and $V_{REF}$ require a stable voltage. The consumption on $V_{DDA}$ can reach several mA (see $I_{DD}(ADCx)$, $I_{DD}(DAC)$, $I_{DD}(COMPx)$, $I_{VDDA}$, and $I_{VREF}$ in the product datasheets for further information).

When available (depending on the package), $V_{REF}$ must be tied to $V_{SSA}$.

On BGA 64-pin and all 100-pin or more packages

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to $V_{REF+}$, a separate external reference voltage which is lower than $V_{DD}$. $V_{REF+}$ is the highest voltage, represented by the full scale value, for an analog input (ADC) or output (DAC) signal.

- For ADC
  - $2.4 \text{ V} \leq V_{REF+} = V_{DDA}$ for full speed ($ADCCLK = 16 \text{ MHz, 1 Msp} \text{s}$)
  - $1.8 \text{ V} \leq V_{REF+} = V_{DDA}$ for medium speed ($ADCCLK = 8 \text{ MHz, 500 Ksp} \text{s}$)
  - $2.4 \text{ V} \leq V_{REF+} \neq V_{DDA}$ for medium speed ($ADCCLK = 8 \text{ MHz, 500 Ksp} \text{s}$)
  - $1.8 \text{ V} \leq V_{REF+} < V_{DDA}$ for low speed ($ADCCLK = 4 \text{ MHz, 250 Ksp} \text{s}$)
  - When product voltage range 3 is selected ($V_{CORE} = 1.2 \text{ V}$), the ADC is low speed ($ADCCLK = 4 \text{ MHz, 250 Ksp} \text{s}$)

- For DAC
  - $1.8 \text{ V} \leq V_{REF+} < V_{DDA}$

On packages with 64 pins or less (except BGA package)

$V_{REF+}$ and $V_{REF}$ pins are not available. They are internally connected to the ADC voltage supply ($V_{DDA}$) and ground ($V_{SSA}$).
2.1.2 Independent LCD supply

The $V_{LCD}$ pin is provided to control the contrast of the glass LCD. This pin can be used in two ways:

- It can receive, from an external circuitry, the desired maximum voltage that is provided on the segment and common lines to the glass LCD by the microcontroller.
- It can also be used to connect an external capacitor that is used by the microcontroller for its voltage step-up converter. This step-up converter is controlled by software to provide the desired voltage to the segment and common lines of the glass LCD. Refer to the specific product datasheet for the capacitor value.

The voltage provided to the segment and common lines defines the contrast of the glass LCD pixels. This contrast can be reduced when the dead time between frames is configured.

2.1.3 Voltage regulator

The internal voltage regulator is always enabled after reset. It can be configured to provide the core with three different voltage ranges. Choosing a range with low $V_{core}$ reduces the consumption but lowers the maximum acceptable core speed. Consumption ranges in decreasing consumption order are as follows:

- Range 1, available only for $V_{DD}$ above 2.0 V, allows maximum speed
- Range 2 allows CPU frequency up to 16 MHz
- Range 3 allows CPU frequency up to 4 MHz

Voltage regulator works in three different modes depending on the application modes.

- In Run mode, the regulator supplies full power to the $V_{core}$ domain (core, memories and digital peripherals).
- In Stop mode, Low power run and Low power wait modes, the regulator supplies low power to the $V_{core}$ domain, preserving the contents of the registers and SRAM.
- In Standby mode, the regulator is powered off. The contents of the registers and SRAM are lost except for those concerned with the Standby circuitry.
2.2 Power supply schemes

The circuit is powered by a stabilized power supply, \( V_{DD} \).

- The \( V_{DD} \) pins must be connected to \( V_{DD} \) with external decoupling capacitors; one single Tantalum or Ceramic capacitor (minimum 4.7 \( \mu \)F typical 10 \( \mu \)F) for the package + one 100 \( n \)F Ceramic capacitor for each \( V_{DD} \) pin).
- The \( V_{DDA} \) pin must be connected to two external decoupling capacitors (100 \( n \)F Ceramic capacitor + 1 \( \mu \)F Tantalum or Ceramic capacitor).
- The \( V_{REF+} \) pin can be connected to the \( V_{DDA} \) external power supply. If a separate, external reference voltage is applied on \( V_{REF+} \), a 100 \( n \)F and a 1 \( \mu \)F capacitor must be connected on this pin. To compensate peak consumption on \( V_{ref} \), the 1 \( \mu \)F capacitor may be increased up to 10 \( \mu \)F when the sampling speed is high. When ADC or DAC is used, \( V_{REF+} \) must remain between 1.8 \( V \) and \( V_{DDA} \). \( V_{REF+} \) can be grounded when ADC and DAC are not active; this enables the user to power down an external voltage reference.
- Additional precautions can be taken to filter analog noise: \( V_{DDA} \) can be connected to \( V_{DD} \) through a ferrite bead.

**Figure 2. Power supply scheme**

1. \( V_{REF+} \) is either connected to \( V_{DDA} \) or to \( V_{REF} \).
2. \( N \) is the number of \( V_{DD} \) and \( V_{SS} \) inputs.
2.3 Reset and power supply supervisor

The input supply to the main and low power regulators is monitored by a power-on/power-down/brownout reset circuit. Power-on/power-down reset are a null power monitoring with fixed threshold voltages, whereas brownout reset gives the choice between several thresholds with a very low, but not null, power consumption.

In addition, the STM32L1xxx embeds a programmable voltage detector that compares the power supply with the programmable threshold. An interrupt can be generated when the power supply drops below the V_{PVD} threshold and/or when the power supply is higher than the V_{PVD} threshold. The interrupt service routine then generates a warning message and/or puts the MCU into a safe state.
1. The PVD is available on all STM32L devices and it is enabled or disabled by software.

2. The BOR is available only on devices operating from 1.8 to 3.6 V, and unless disabled by option byte it masks the POR/PDR threshold.

3. When the BOR is disabled by option byte, the reset is asserted when $V_{DD}$ goes below PDR level.

4. For devices operating from 1.65 to 3.6 V, there is no BOR and the reset is released when $V_{DD}$ goes above POR level and asserted when $V_{DD}$ goes below PDR level.
2.3.1 Power-on reset (POR)/power-down reset (PDR), brownout reset (BOR)

The monitoring voltage begins at 0.7 V.

During power-on, for devices operating between 1.8 and 3.6 V, the BOR keeps the device under reset until the supply voltages (V_{DD} and V_{DDIO}) come close to the lowest acceptable voltage (1.8 V). At power-up this internal reset is maintained during ~1 ms to wait for the supply to reach its final value and stabilize.

At power-down the reset is activated as soon as the power drops below the lowest limit (1.65 V).

At power-on, a defined reset should be maintained below 0.7 V. The upper threshold for a reset release is defined in the electrical characteristics section of the product datasheets.

![Figure 5. Power on reset/power down reset waveform](image)

If you want to run the CPU at full speed the threshold should be raised to 2.0 V. For a programmable threshold above the chip lowest limit, a brownout reset can be configured to the desired value. The BOR can also be used to detect a power voltage drop earlier. The threshold values of the BOR can be configured through the FLASH_OBR option byte.

2.3.2 Programmable voltage detector (PVD)

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. Seven different PVD levels can be selected by software between 1.85 V and 3.05 V, with a 200 mV step. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine then generates a warning message and/or puts the MCU into a safe state. The PVD is enabled by software configuration. As an example, the service routine can perform emergency shutdown tasks.
2.3.3 Brownout reset (BOR)

During power on, the brownout reset (BOR) keeps the device under reset until the supply voltage reaches the specified \(V_{\text{BOR}}\) threshold.

For devices operating from 1.65 to 3.6 V, the BOR option is not available and the power supply is monitored by the POR/PDR. As the POR/PDR thresholds are at 1.5 V, a “grey zone” exists between the \(V_{\text{POR}}/V_{\text{PDR}}\) thresholds and the minimum product operating voltage 1.65 V.

For devices operating from 1.8 to 3.6 V, the BOR is always active at power on and its threshold is 1.8 V.

When the system reset is released, the BOR level can be reconfigured or disabled by option byte loading.

If the BOR level is kept at the lowest level, 1.8 V at power-on and 1.65 V at power down, the system reset is fully managed by the BOR and the product operating voltages are within safe ranges.

When the BOR option is disabled by option byte, the power down reset is controlled by the PDR and a “grey zone” exists between the 1.65 V and \(V_{\text{PDR}}\).

\(V_{\text{BOR}}\) is configured through device option bytes. By default, level 4 threshold is activated. Five programmable \(V_{\text{BOR}}\) thresholds can be selected (see product datasheets for actual \(V_{\text{BOR0}}\) to \(V_{\text{BOR4}}\) thresholds).

When the supply voltage \((V_{\text{DD}})\) drops below the selected \(V_{\text{BOR}}\) threshold, a device reset is generated. When the \(V_{\text{DD}}\) is above the \(V_{\text{BOR}}\) upper limit the device reset is released and the system can start.

BOR can be disabled by programming the device option bytes. To disable the BOR function, \(V_{\text{DD}}\) must have been higher than \(V_{\text{BOR0}}\) to start the device option byte programming sequence. The power-on and power-down is then monitored by the POR and PDR (see power-on reset (POR)/power-down reset (PDR) section in the product datasheets).

The BOR threshold hysteresis is \(~100\) mV (between the rising and the falling edge of the supply voltage).
2.3.4 System reset

A system reset sets all registers to their reset values except for the RTC, backup registers and RCC control/status register, RCC_CSR.

A system reset is generated when one of the following events occurs:
1. A low level on the NRST pin (external reset)
2. Window watchdog end-of-count condition (WWDG reset)
3. Independent watchdog end-of-count condition (IWDG reset)
4. A reset bit set by software (SWreset)
5. Entering Standby or Stop mode configured to generate a reset (Low-power management reset)
6. Option byte loader reset
7. Exiting Standby mode

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

Figure 7. Reset circuit

The STM32L does not require an external reset circuit to power-up correctly. Only a pull-down capacitor is recommended to improve EMS performance by protecting the device against parasitic resets (see Figure 7).

Charging/discharging the pull-down capacitor thru the internal resistor adds to the device power consumption. The recommended value of 100 nF for the capacitor can be reduced to 10 nF to limit this power consumption.
3 Clocks

Four different clock sources can be used to drive the system clock (SYSCLK). They are:

- HSI ((high-speed internal) oscillator clock
- HSE (high-speed external) oscillator clock
- PLL clock
- MSI (multispeed internal) oscillator clock

The MSI is used as a system clock source after startup from reset, wake-up from Stop or Standby low power modes.

The devices have the following two secondary clock sources:

- 37 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for auto-wakeup from Stop/Standby mode.
- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Refer to the STM32L1xxx reference manual (RM0038) for a description of the clock tree.

3.1 MSI clock

The MSI clock signal is generated from an internal RC oscillator. Its frequency range can be adjusted by software through the RCC_ICSCR register. Seven frequency ranges are available: 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz (default value) and 4.2 MHz. Those frequencies are multiple values of 32.768 kHz.

The MSI clock is used as a system clock after a restart from reset.

The MSI RC oscillator has the advantage of providing a low-cost (no external components) low-power clock source. It is used as a wakeup clock in low power modes to reduce power consumption and wakeup time.

The MSIRDY flag in the RCC_CR register indicates whether the MSI RC is stable or not. At startup, the MSI RC output clock is not released until this bit is set by hardware.

The MSI RC can be switched on and off through the RCC_CR register (default is on).

If the application is subject to voltage or temperature variations, this may affect the RC oscillator speed. You can trim the MSI frequency in the application through the RCC_ICSCR register. Typically, this uses the HSE as reference (see RM0038 for details on clock measurement with TIM9/TIM10/TIM11). For more information refer to AN3300 “How to calibrate an STM32L1xx internal RC oscillator”.

3.2 HSE OSC clock

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE user external clock (see Figure 8)
- HSE external crystal/ceramic resonator (see Figure 9)

1. The value of \( R_{\text{EXT}} \) depends on the crystal characteristics. A typical value is in the range of 5 to 6 \( R_S \) (resonator series resistance).

2. Load capacitance, \( C_L \), has the following formula:
\[
C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{\text{stray}}
\]
where \( C_{\text{stray}} \) is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Please refer to Section 6: Recommendations on page 25 to minimize its value.

3.2.1 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 32 MHz.

The external clock signal (square, sine or triangle) with a duty cycle of about 50%, has to drive the OSC_IN pin while the OSC_OUT pin must be left in the high impedance state (see Figure 8 and Figure 9).

3.2.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 1 to 24 MHz.

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in Figure 9.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For \( C_{L1} \) and \( C_{L2} \) it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. \( C_{L1} \) and \( C_{L2} \) are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of \( C_{L1} \) and \( C_{L2} \). The PCB and MCU pin capacitances must be included when sizing \( C_{L1} \) and \( C_{L2} \) (10 pF can be used as a rough estimate of the combined pin and board capacitance).

Refer to the electrical characteristics sections in the datasheet of your product for more details.
3.3 LSE OSC clock

The low-speed external clock signal (LSE) can be generated from two possible clock sources:

- LSE user external clock (see Figure 10)
- LSE external crystal/ceramic resonator (see Figure 11)

### 3.3.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It must have a frequency of 32.768 kHz. The external clock signal (square, sine or triangle) with a duty cycle of about 50% has to drive the OSC32_IN pin while the OSC32_OUT pin must be left high impedance (see Figure 10).

### 3.3.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The oscillator can be switched on and off by software (default is off). When switched on, the oscillator is not stable immediately. A bit is set in the RCC_CSR register when the oscillator becomes stable and an interrupt can be generated if enabled in the RCC_CIR register.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator (see Figure 11).
3.4 **Clock security system (CSS)**

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped. If a failure is detected on the HSE oscillator clock, this oscillator is automatically disabled and an interrupt is generated to inform the software about the failure (clock security system interrupt, CSSI), allowing the MCU to perform rescue operations. The CSSI is linked to the Cortex™-M3 NMI (non-maskable interrupt) exception vector.

If the HSE oscillator is used directly or indirectly as the system clock (indirectly means: it is used as the PLL input clock, and the PLL clock is used as the system clock), a detected failure causes the system clock to switch to the MSI oscillator and the external HSE oscillator to be disabled. If the HSE oscillator clock is the clock entry of the PLL used as the system clock when the failure occurs, the PLL is also disabled.

For details, see the STM32L1xxx reference manual (RM0038).
4 Boot configuration

4.1 Boot mode selection

In the STM32L1xxx, three different boot modes can be selected by means of the BOOT[1:0] pins as shown in Table 2.

<table>
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<tr>
<th>BOOT mode selection pins</th>
<th>Boot mode</th>
<th>Aliasing</th>
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<tr>
<td>BOOT1</td>
<td>BOOT0</td>
<td>Main Flash memory</td>
</tr>
<tr>
<td>x</td>
<td>0</td>
<td>System memory</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Embedded SRAM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Embedded SRAM</td>
</tr>
</tbody>
</table>

The values on the BOOT pins are latched on the 4th rising edge of SYSCLK after a reset. It is up to the user to set the BOOT1 and BOOT0 pins after reset to select the required boot mode.

BOOT0 is a dedicated pin while BOOT1 is shared with a GPIO pin. Once BOOT1 has been sampled, the corresponding GPIO pin is free and can be used by the application.

The BOOT pins are also resampled when exiting Standby mode. Consequently, they must be kept in the required Boot mode configuration in Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, and starts code execution from the boot memory starting from 0x0000 0004.

4.2 Boot pin connection

Figure 12 shows the external connection required to select the boot memory of the STM32L1xxx.

Figure 12. Boot mode selection implementation example

1. Resistor values are given only as a typical example.
4.3 **Embedded boot loader mode**

The embedded boot loader is used to reprogram the Flash memory through one of the following interfaces: USART1, USART2 or USB for medium+ and high density devices. This program is located in the system memory and is programmed by ST during production (see the STM32L Flash programming manual for further details).
5 Debug management

5.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool.

Figure 13 shows the connection of the host to a development board. The evaluation board (STM32L152-EVAL and STM32L152D-EVAL) embeds the debug tools (ST-LINK) so it can be directly connected to the PC through an USB cable.

Figure 13. Host-to-board connection

5.2 SWJ debug port (serial wire and JTAG)

The STM32L1xxx core integrates the serial wire/JTAG debug port (SWJ-DP). It is an ARM® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.
5.3 Pinout and debug port pins

The STM32L1xxx MCU is offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

5.3.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as alternate functions of general-purpose I/Os (GPIOs). These pins, shown in Table 3, are available on all packages.

Table 3. Debug port pin assignment

<table>
<thead>
<tr>
<th>SWJ-DP pin name</th>
<th>JTAG debug port</th>
<th>SW debug port</th>
<th>Pin assignment</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Type</td>
<td>Description</td>
<td>Type</td>
</tr>
<tr>
<td>JTMS/SWDIO</td>
<td>I</td>
<td>JTAG test mode selection</td>
<td>I/O</td>
</tr>
<tr>
<td>JTCK/SWCLK</td>
<td>I</td>
<td>JTAG test clock</td>
<td>I</td>
</tr>
<tr>
<td>JTDI</td>
<td>I</td>
<td>JTAG test data input</td>
<td>-</td>
</tr>
<tr>
<td>JTDI/TRACESWO</td>
<td>O</td>
<td>JTAG test data output</td>
<td>-</td>
</tr>
<tr>
<td>JNTRST</td>
<td>I</td>
<td>JTAG test nReset</td>
<td>-</td>
</tr>
</tbody>
</table>

5.3.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins which are immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32L1xxx MCU implements a register to disable all or part of the SWJ-DP port, and so releases the associated pins for general-purpose I/O usage. This register is mapped on an APB bridge connected to the Cortex™-M3 system bus. It is programmed by the user software program and not by the debugger host.

Table 4 shows the different possibilities for releasing some pins. For more details, see the STM32L1xxx reference manual (RM0038).

Table 4. SWJ I/O pin availability

<table>
<thead>
<tr>
<th>Available debug ports</th>
<th>SWJ I/O pin assigned</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PA13 / JTMS/SWDIO</td>
</tr>
<tr>
<td>Full SWJ (JTAG-DP + SW-DP) - reset state</td>
<td>X</td>
</tr>
<tr>
<td>Full SWJ (JTAG-DP + SW-DP) but without JNTRST</td>
<td>X</td>
</tr>
<tr>
<td>JTAG-DP disabled and SW-DP enabled</td>
<td>X</td>
</tr>
<tr>
<td>JTAG-DP disabled and SW-DP disabled</td>
<td>Released</td>
</tr>
</tbody>
</table>
5.3.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must not be floating since they are directly connected to flip-flops which control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32L1xxx embeds internal pull-up and pull-down resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

The software can then use these I/Os as standard GPIOs.

*Note:* The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but, there is no special recommendation for TCK. However, for the STM32L1xxx, an integrated pull-down resistor is used for JTCK.

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

5.3.4 SWJ debug port connection with standard JTAG connector

*Figure 14* shows the connection between the STM32L1xxx and a standard JTAG connector.
6 Recommendations

6.1 Printed circuit board
For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (VSS) and another dedicated to the VDD supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

6.2 Component position
A preliminary layout of the PCB must make separate circuits:
- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution. This will reduce cross-coupling on the PCB that introduces noise.

6.3 Ground and power supply (VSS, VDD, VSSA, VDDA)
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually, and all ground returns should be to a single point. Loops must be avoided or have a minimum area. In order to improve analog performance, you must use separate supply sources for VDD and VDDA, and place the decoupling capacitors as close as possible to the device. The power supplies should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

6.4 Decoupling
All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors C (100 nF) and a Tantalum or Ceramic capacitor C of about 10 µF connected in parallel on the STM32L1xxx device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. Figure 15 shows the typical layout of such a VDD/VSS pair.
6.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands).
  
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  
  For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example, clock)
- Sensitive signals (example, high impedance)

6.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, unused clocks, counters or I/Os, should not be left free. I/Os should be connected to a fixed logic level of 0 or 1 by an external or internal pull-up or pull-down on the unused I/O pin. The other option is to configure GPIO as output mode using software. Unused features should be frozen or disabled, which is their default value.
7 Reference design

7.1 Description

The reference design shown in Figure 16, is based on the STM32L152VB(T6).

This reference design can be tailored to any STM32L1xxx device with a different package, using the pin correspondence given in Table 7: Reference connection for all packages.

7.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X1–32.768 kHz crystal for the embedded RTC
- HSE: X2–8 MHz crystal for the STM32L1xxx microcontroller

Refer to Section 3: Clocks on page 16.

7.1.2 Reset

The reset signal in Figure 16 is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to Section 2.3: Reset and power supply supervisor on page 11.

7.1.3 Boot mode

The boot option is configured by setting switches SW2 (Boot 0) and SW1 (Boot 1). Refer to Section 4: Boot configuration on page 20.

Note: When waking up from Standby mode, the Boot pins are sampled. In this situation, you need to pay attention to their values.

7.1.4 SWJ interface

The reference design shows the connection between the STM32L1xxx and a standard JTAG connector. Refer to Section 5: Debug management on page 22.

Note: It is recommended to connect the reset pins so as to be able to reset the application from the tools.

7.1.5 Power supply

Refer to Section 2: Power supplies on page 7.
### 7.2 Component references

#### Table 5. Mandatory components

<table>
<thead>
<tr>
<th>Reference</th>
<th>Components name</th>
<th>Value</th>
<th>Quantity</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1A</td>
<td>Microcontroller</td>
<td>STM32L152VB(T6)</td>
<td>1</td>
<td>100-pin package</td>
</tr>
<tr>
<td>C5, C10, C11, C12, C13, C14</td>
<td>Capacitor</td>
<td>100 nF</td>
<td>3 ... 6</td>
<td>Ceramic capacitors (decoupling capacitors)</td>
</tr>
<tr>
<td>C9</td>
<td>Capacitor</td>
<td>10 µF</td>
<td>1</td>
<td>Ceramic capacitor (decoupling capacitor)</td>
</tr>
<tr>
<td>C4, C6</td>
<td>Capacitor</td>
<td>1 µF</td>
<td>2</td>
<td>Ceramic capacitor (LCD booster or decoupling capacitor)</td>
</tr>
</tbody>
</table>

#### Table 6. Optional components

<table>
<thead>
<tr>
<th>Reference</th>
<th>Components name</th>
<th>Value</th>
<th>Quantity</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2, R4, R5, R7, R8</td>
<td>Resistor</td>
<td>10 kΩ</td>
<td>9</td>
<td>Pull-up and pull-down for JTAG and Boot mode.</td>
</tr>
<tr>
<td>R6</td>
<td>Resistor</td>
<td>390 Ω</td>
<td>1</td>
<td>Used for HSE: the value depends on the crystal characteristics.</td>
</tr>
<tr>
<td>R1</td>
<td>Resistor</td>
<td>x Ω</td>
<td>1</td>
<td>Used for LSE: the value depends on the crystal characteristics. This resistor value depends on the chosen crystal (refer to application note AN2867).</td>
</tr>
<tr>
<td>R3</td>
<td>Resistor</td>
<td>0 Ω</td>
<td>1</td>
<td>For low pass filter</td>
</tr>
<tr>
<td>C3, C15</td>
<td>Capacitor</td>
<td>100 nF</td>
<td>2</td>
<td>Ceramic capacitors (decoupling capacitors)</td>
</tr>
<tr>
<td>C1, C2</td>
<td>Capacitor</td>
<td>6.8 pF</td>
<td>2</td>
<td>Used for LSE: the value depends on the crystal characteristics. Fits for MC-306 32.768K-E3, which has a load capacitance of 6 pF.</td>
</tr>
<tr>
<td>C7, C8</td>
<td>Capacitor</td>
<td>20 pF</td>
<td>2</td>
<td>Used for HSE: the value depends on the crystal characteristics.</td>
</tr>
<tr>
<td>X2</td>
<td>Quartz</td>
<td>8 MHz</td>
<td>1</td>
<td>Used for HSE</td>
</tr>
<tr>
<td>X1</td>
<td>Quartz</td>
<td>32 kHz</td>
<td>1</td>
<td>Used for LSE</td>
</tr>
<tr>
<td>CN1</td>
<td>JTAG connector</td>
<td>HE10</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>SW1, SW2</td>
<td>Switch</td>
<td></td>
<td>2</td>
<td>Used to select the right boot mode</td>
</tr>
<tr>
<td>B1</td>
<td>Push-button</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>Ferrite bead</td>
<td></td>
<td>1</td>
<td>For EMC reduction on VDDA supply</td>
</tr>
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</table>
Figure 16. STM32L152VB(T6) microcontroller reference schematic
<table>
<thead>
<tr>
<th>Pin name</th>
<th>Pin numbers for LQFP packages</th>
<th>Pin numbers for BGA packages</th>
<th>Pin numbers for UFQFPN package</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>144 pins</td>
<td>100 pins</td>
<td>64 pins</td>
</tr>
<tr>
<td>PH0-OSC_IN</td>
<td>23</td>
<td>12</td>
<td>5</td>
</tr>
<tr>
<td>PH1-OSC_OUT</td>
<td>24</td>
<td>13</td>
<td>6</td>
</tr>
<tr>
<td>PC15-OSC32_OUT</td>
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<td>9</td>
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</tr>
<tr>
<td>PC14-OSC32_IN</td>
<td>8</td>
<td>8</td>
<td>3</td>
</tr>
<tr>
<td>BOOT0</td>
<td>138</td>
<td>94</td>
<td>60</td>
</tr>
<tr>
<td>PB2-BOOT1</td>
<td>48</td>
<td>37</td>
<td>28</td>
</tr>
<tr>
<td>NRST</td>
<td>25</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>PA13</td>
<td>105</td>
<td>72</td>
<td>46</td>
</tr>
<tr>
<td>PA14</td>
<td>109</td>
<td>76</td>
<td>49</td>
</tr>
<tr>
<td>PA15</td>
<td>110</td>
<td>77</td>
<td>50</td>
</tr>
<tr>
<td>PB4</td>
<td>134</td>
<td>90</td>
<td>56</td>
</tr>
<tr>
<td>PB3</td>
<td>133</td>
<td>89</td>
<td>55</td>
</tr>
<tr>
<td>VSS_1</td>
<td>71</td>
<td>49</td>
<td>31</td>
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<tr>
<td>VSS_2</td>
<td>107</td>
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<td>VSS_6</td>
<td>51</td>
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<td>VSS_7</td>
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<td>-</td>
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</tr>
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<td>VSS_8</td>
<td>83</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>VSS_9</td>
<td>94</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>VSS_10</td>
<td>120</td>
<td>-</td>
<td>-</td>
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<tr>
<td>VSS_11</td>
<td>130</td>
<td>-</td>
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<td>VDD_1</td>
<td>72</td>
<td>50</td>
<td>32</td>
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<td>VDD_2</td>
<td>108</td>
<td>75</td>
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<tr>
<td>VDD_3</td>
<td>144</td>
<td>100</td>
<td>64</td>
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<td>VDD_4</td>
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<td>VDD_5</td>
<td>17</td>
<td>11</td>
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<td>VDD_6</td>
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<td>VDD_7</td>
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<tr>
<td>VDD_8</td>
<td>84</td>
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Table 7. Reference connection for all packages (continued)

<table>
<thead>
<tr>
<th>Pin name</th>
<th>Pin numbers for LQFP packages</th>
<th>Pin numbers for BGA packages</th>
<th>Pin numbers for UFQFPN package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>144 pins</td>
<td>100 pins</td>
<td>64 pins</td>
</tr>
<tr>
<td>V_DD_9</td>
<td>95</td>
<td>--</td>
<td>-</td>
</tr>
<tr>
<td>V_DD_10</td>
<td>121</td>
<td>--</td>
<td>-</td>
</tr>
<tr>
<td>V_DD_11</td>
<td>131</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>V_REF+</td>
<td>32</td>
<td>21</td>
<td>-</td>
</tr>
<tr>
<td>V_REF-</td>
<td>31</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>V_SSA</td>
<td>30</td>
<td>19</td>
<td>12</td>
</tr>
<tr>
<td>V_DDA</td>
<td>33</td>
<td>22</td>
<td>13</td>
</tr>
<tr>
<td>V_LCD</td>
<td>6</td>
<td>6</td>
<td>1</td>
</tr>
</tbody>
</table>
## Revision history

### Table 8. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>28-Jun-2010</td>
<td>1</td>
<td>Initial release</td>
</tr>
<tr>
<td>29-Jul-2010</td>
<td>2</td>
<td>Updated the following sections: Section 2.1: Introduction, Section 2.1.1: Independent A/D converter supply and reference voltage, Section 2.1.2: Independent LCD supply, Section 2.3.1: Power-on reset (POR)/power-down reset (PDR), brownout reset (BOR), and Section 2.3.4: System reset. Added Section 2.3.3: Brownout reset (BOR). Replaced Figure 4, Figure 5, Figure 6, and Figure 7. In Section 3.3.2, replaced RCC_ICR register by RCC_CIR register. Replaced PF0_OSC_IN and PF1_OSC_OUT by PH0_OSC_IN and PH1_OSC_OUT in Figure 16 and Table 7. Updated value of C4 and C9 decoupling capacitors in Figure 16.</td>
</tr>
<tr>
<td>01-Oct-2010</td>
<td>3</td>
<td>Modified Section 2.3.4: System reset on page 15 Updated capacitors in Table 5 and Table 5</td>
</tr>
<tr>
<td>07-Apr-2011</td>
<td>4</td>
<td>Changed title of document from &quot;STM32L1xxx hardware development: getting started&quot; to &quot;Getting started with STM32L1xxx hardware development&quot;. Modified Section 3.1: MSI clock, Section 2.2: Power supply schemes, and Figure 2.</td>
</tr>
<tr>
<td>29-Jun-2011</td>
<td>5</td>
<td>Updated Section 2.1.1: Independent A/D converter supply and reference voltage and Section 2.2: Power supply schemes.</td>
</tr>
<tr>
<td>30-May-2012</td>
<td>6</td>
<td>Updated to adapt to STM32L1xxx High density devices</td>
</tr>
<tr>
<td>20-Jun-2013</td>
<td>7</td>
<td>Document reformatted: Replaced “STM32L1xxx” by “STM32L1xxx” in the entire document. Updated: Section 2.1: Introduction, Section 2.1.2: Independent LCD supply, Section 6.2: Component position, Section 6.3: Ground and power supply (VSS, VDD, VSSA, VDDA), Section 6.4: Decoupling and Section 7.1.3: Boot mode Figure 1: Power supply overview, Figure 2: Power supply scheme, Figure 7: Reset circuit and Figure 16: STM32L152VB(T6) microcontroller reference schematic Table 5: Mandatory components and Table 6: Optional components Added: Table 1: Applicable products Section 1: Glossary Figure 3: Optional LCD power supply scheme</td>
</tr>
</tbody>
</table>
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