Introduction

This document describes the STEVAL-ISA115V1, a 12 V, 0.13 A power supply set in buck topology with the VIPer06XS, a new offline high voltage converter by STMicroelectronics, specifically developed for non-isolated SMPS.

The features of the device are:
- 800 V avalanche rugged power section
- PWM operation at 30 kHz with frequency jittering for lower EMI
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition and low standby power consumption

The available protection includes: thermal shutdown with hysteresis, delayed overload protection and open loop failure protection. All protection is auto-restart mode.

Figure 1. STEVAL-ISA115V1 product evaluation board
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1 Adapter features

The electrical specifications of the evaluation board are listed in Table 1.

### Table 1. Electrical specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>$V_{IN}$</td>
<td>[90 V$<em>{AC}$; 265 V$</em>{AC}$]</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{OUT}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Max. output current</td>
<td>$I_{OUT}$</td>
<td>0.15 A</td>
</tr>
<tr>
<td>Precision of output regulation</td>
<td>$\Delta V_{OUT,LF}$</td>
<td>±5%</td>
</tr>
<tr>
<td>High frequency output voltage ripple</td>
<td>$\Delta V_{OUT,HF}$</td>
<td>50 mV</td>
</tr>
<tr>
<td>Max. ambient operating temperature</td>
<td>$T_{AMB}$</td>
<td>60 °C</td>
</tr>
</tbody>
</table>

2 Circuit description

The converter schematic is given in Figure 2. The input section includes a resistor R1 for inrush current limiting, a diode D1 and a Pi filter (C1, L1, C2) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier, internally referenced to 3.3 V. This allows the output voltage value to be set in a simple way through the R4-R5 voltage divider between the output terminal and the FB pin, according to the following equation:

**Equation 1**

$$V_{OUT} = 3.3V \times \left(1 + \frac{R5}{R4}\right)$$

where R4 has been split into R4a and R4b; and R5 into R5a and R5b so to allow a better tuning of the output voltage value.

The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin and is made up of Cc, R3 and C7.

The bleeder resistor Rbl provides about 1 mA minimum load, in order to avoid overvoltage when the output load is disconnected. Its value is a trade-off between output voltage increase and power consumption rise in no load.

At power-up the DRAIN pin supplies the internal HV startup current generator which charges the C3 capacitor up to $V_{DD,on}$ (13 V typical). At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C3, waiting for $V_{OUT}$ reaches its steady-state value. After that, the IC is supplied from the output through the diode Daux. This allows the system to reach very low values of standby consumption because, keeping the $V_{DD}$ voltage always above the $V_{DDCSon}$ threshold, prevents the HV startup generator from being turned on.
Figure 2. Application schematic
## 3 Bill of material

### Table 2. Bill of material

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
<th>Footprint</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>4.7 µF, 400 V</td>
<td>Electrolytic capacitor</td>
<td>Saxon</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>4.7 µF, 400 V</td>
<td>Electrolytic capacitor</td>
<td>Saxon</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>2.2 µF, 25 V</td>
<td>Ceramic capacitor</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>CFB</td>
<td>n.c</td>
<td>Ceramic capacitor</td>
<td>SMD: 0805</td>
<td></td>
</tr>
<tr>
<td>Cf</td>
<td>100 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>CC</td>
<td>n.c</td>
<td>Ceramic capacitor</td>
<td>SMD: 0805</td>
<td></td>
</tr>
<tr>
<td>C7</td>
<td>22 nF, 25 V</td>
<td>Ceramic capacitor</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>C8</td>
<td>150 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>C9</td>
<td>100 µF, 25 V</td>
<td>Electrolytic capacitor</td>
<td>Rubycon, ZL series</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>1N4007</td>
<td>High voltage rectifier</td>
<td>DO-41</td>
<td>Fairchild</td>
</tr>
<tr>
<td>D3</td>
<td>STTH1L06</td>
<td>High voltage ultra fast rectifier</td>
<td>SMB (SOD87)</td>
<td>ST</td>
</tr>
<tr>
<td>D4</td>
<td>STTH1L06</td>
<td>High voltage ultra fast rectifier</td>
<td>SMB (SOD87)</td>
<td>ST</td>
</tr>
<tr>
<td>Daux</td>
<td>1N4148</td>
<td>100 V, 0.15 A fast switch diode</td>
<td>SOD-123</td>
<td>Zetex</td>
</tr>
<tr>
<td>IC</td>
<td>VIPer06XS</td>
<td>High voltage converter</td>
<td>SSO-10</td>
<td>ST</td>
</tr>
<tr>
<td>L1</td>
<td>1 mH</td>
<td>Input filter inductor</td>
<td>SMD</td>
<td>Epcos</td>
</tr>
<tr>
<td>L2</td>
<td>RFB0810-152</td>
<td>1.5 mH power inductor</td>
<td>Coilcraft</td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>22 ohm, 1%</td>
<td>1 W resistor</td>
<td>Panasonic</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>1.2 kohm, 1%</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R4a</td>
<td>12 kohm, 1%</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R4b</td>
<td>0 ohm</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td></td>
</tr>
<tr>
<td>R5a</td>
<td>0 ohm</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td></td>
</tr>
<tr>
<td>R5b</td>
<td>33 kohm, 1%</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R6</td>
<td>not mounted</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td></td>
</tr>
<tr>
<td>Rbl</td>
<td>10 kohm, 1%</td>
<td>1/4 W resistor</td>
<td>SMD: 0805</td>
<td>Panasonic</td>
</tr>
</tbody>
</table>
4 Layout

Figure 3. Layout (top)

Figure 4. Layout (bottom)
5 Testing the board

5.1 Typical waveforms

GND voltage and the current across the inductor L2 (I_L2) in full load condition are shown for the two nominal input voltages in Figure 5 and Figure 6, and for minimum and maximum input voltage in Figure 7 and Figure 8 respectively.

Figure 5. Waveforms at $V_{IN} = 115\, V_{AC}$, full load
Figure 6. Waveforms at $V_{IN} = 230\, V_{AC}$, full load

Figure 7. Waveforms at $V_{IN} = 80\, V_{AC}$, full load
Figure 8. Waveforms at $V_{IN} = 265\, V_{AC}$, full load
5.2 Line/load regulation and output voltage ripple

The output voltage of the board has been measured in different lines and load conditions. The results are shown in Figure 9 and Figure 10.

The output voltage ripple in full load condition is shown in Figure 11 at \( V_{IN} = 115 \, V_{AC} \) and in Figure 12 at \( V_{IN} = 230 \, V_{AC} \).

Figure 9. Line regulation  

![Figure 9. Line regulation](AM16636v1)

Figure 10. Load regulation  

![Figure 10. Load regulation](AM16637v1)

Figure 11. Output voltage ripple at 115 \( V_{AC} \), full load  

![Figure 11. Output voltage ripple at 115 \( V_{AC} \), full load](AM16638v1)

Figure 12. Output voltage ripple 230 \( V_{AC} \), full load  

![Figure 12. Output voltage ripple 230 \( V_{AC} \), full load](AM16639v1)
5.3 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold, \( V_{\text{COMPL}} \) (1.1 V, typical), the switching is disabled and no more energy is transferred to the secondary side. So, the output voltage decreases and the regulation loop makes the COMP pin voltage increase again. As it rises 40 mV above the \( V_{\text{COMPL}} \) threshold, the normal switching operation is resumed. This results in a controlled on/off operation (referred to as "burst mode") as long as the output power is so low that it requires a turn-on time lower than the minimum turn-on time of the VIPER06XS. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy saving regulations.

The figures below show the output voltage ripple when the converter is no/lightly loaded and supplied with 115 \( V_{\text{AC}} \) and with 230 \( V_{\text{AC}} \) respectively.

![Figure 13. Output voltage ripple at 115 \( V_{\text{AC}} \), no load](image1)

![Figure 14. Output voltage ripple at 230 \( V_{\text{AC}} \), no load](image2)

5.4 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltage (\( V_{\text{IN}} = 115 \ V_{\text{AC}} \) and \( V_{\text{IN}} = 230 \ V_{\text{AC}} \)).

External power supplies (the power supplies which are contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 4 "Active Mode Efficiency" criterion, which states an active mode efficiency higher than 65.9% for a power throughput of 1.8 W.

Another standard to be applied to external power supplies in the coming years is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 70.9%.

The presented evaluation board is compliant with both standards, as per Figure 15, where the average efficiencies of the board at 115 \( V_{\text{AC}} \) (79.2%) and at 230 \( V_{\text{AC}} \) (76.4%) are plotted with dotted lines, together with the above limits. In the same figure the efficiency at 25%, 50%, 75% and 100% of load for both input voltages is also shown.
5.5 Light load performance

The input power of the converter has been measured in no load condition for different input voltages and results are reported in Table 3.

Table 3. No load input power

<table>
<thead>
<tr>
<th>$V_{IN}$ [VAC]</th>
<th>$P_{IN}$ [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>32</td>
</tr>
<tr>
<td>115</td>
<td>34</td>
</tr>
<tr>
<td>150</td>
<td>37</td>
</tr>
<tr>
<td>180</td>
<td>39</td>
</tr>
<tr>
<td>230</td>
<td>42</td>
</tr>
<tr>
<td>265</td>
<td>48</td>
</tr>
</tbody>
</table>

In version 4 of the Code of Conduct, the power consumption of the power supply when it is no loaded is also considered. The criteria to be compliant with are reported in Table 4:
The power consumption of the presented board is about six times lower than the limit fixed by version 4 of the Code of Conduct. Even though the performance seems to be disproportionally better than requirements, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption and if the converter is used as an auxiliary power supply, the line filter is often the main line filter of the entire power supply that increases greatly the standby consumption.

Even though version 4 of the Code of Conduct does not have other requirements regarding light load performance, in order to give a more complete overview, the consumption of the evaluation board in two other light load cases ($P_{\text{OUT}} = 25$ mW and $P_{\text{OUT}} = 50$ mW) has also been measured. The results versus line voltage are plotted in Figure 16, together with the no load measurements reported in Table 3.

### Table 4. Energy consumption criteria for no load

<table>
<thead>
<tr>
<th>Nameplate output power</th>
<th>Maximum power in no load for AC-DC EPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to ≤ 50 W</td>
<td>&lt; 0.3 W</td>
</tr>
<tr>
<td>&gt; 50 W &lt; 250 W</td>
<td>&lt; 0.5 W</td>
</tr>
</tbody>
</table>

Several criteria can be adopted to measure the performance of a converter. One criterion is to measure the output power (or the efficiency) when the input power is equal to 1 Watt. This measurement is shown in Figure 17 for different input voltage values.
Another requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded 250 mW. The evaluation board satisfies this requirement, as shown in Figure 18.
6 Functional check

6.1 Startup

The start-up phase at maximum load is shown in Figure 19 and Figure 21 at both nominal input voltages (115 VAC and 230 VAC).

6.2 Overload protection

In case of overload or short-circuit (see Figure 23), the drain current reaches the IDLIM value (or the one set by the user through the RLIM resistor). In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for the time tOVL (50 msec typical, internally set) the overload protection is tripped, the power section is turned off and the converter is disabled for a tRESTART time (1 sec typical). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (Figure 24). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.
After the short removal, IC resumes working normally. If the short is removed during tSS or tOVL, before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during tRESTART, IC must wait for the tRESTART period to elapse before switching is resumed Figure 26.

### 6.3 Feedback loop failure protection

This protection is available any time IC is externally biased. As the loop is broken (R4 shorted or R5 open), the output voltage \( V_{\text{OUT}} \) increases and the VIPER06XS runs at its maximum current limitation. VDD pin voltage increases as well, because it is linked to the \( V_{\text{OUT}} \) voltage through the Daux diode.

If the VDD voltage reaches the VDD clamp threshold (23.5 V min.) in less than 50 msec the IC is shut down by open loop failure protection (see Figure 27 and Figure 28), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low-side resistor of the output voltage divider, \( R_4 = R_{4a1}+R_{4b} \). The same behavior can be induced opening the high-side resistor, \( R_5 = R_{5a}+R_{5b} \).
The protection acts in auto-restart mode with $t_{\text{RESTART}} = 1$ sec (*Figure 28*). As the fault is removed, normal operation is restored after the last $t_{\text{RESTART}}$ interval has been completed (*Figure 30*).
7 Feedback loop calculation guidelines

7.1 Transfer function

The set PWM modulator + power stage is indicated with $G_1(f)$, while $C(f)$ is the "controller", the network in charge to assure the stability of the system.

![Control loop block diagram](image)

The mathematical expression of the power plant $G_1(f)$ in DCM is the following:

**Equation 2**

$$G_1(f) = \frac{\Delta V_{\text{OUT}}}{\Delta \delta} = G_{10} \cdot \frac{1 + \frac{1}{f_z}}{1 + \frac{1}{f_p}}$$

where $f_z$ is the zero due to the ESR of the output capacitor:

**Equation 3**

$$f_z = \frac{1}{2 \cdot \pi \cdot C_{\text{OUT}} \cdot \text{ESR}}$$

and $f_p$ is the pole due to the output load:

**Equation 4**

$$f_p = \frac{1 + \beta \cdot R_{\text{OUT}}}{2 \cdot \pi \cdot C_{\text{OUT}} \cdot (\text{ESR} + R_{\text{OUT}} + \text{ESR} \cdot \beta \cdot R_{\text{OUT}})}$$

with:
In the above formulas, $C_{OUT}$ and ESR are the capacitance and the equivalent series resistance of the output capacitor respectively, $V_y$ is the forward drop of the free-wheeling diode, $R_{OUT} = V_{OUT}/I_{OUT}$ is the output load, $I_{pk}$ is the drain peak current at full load and $\partial = T_{on}\cdot fsw$ is the duty cycle.

If just an RC series between COMP and GND is chosen as a compensation network, as shown in Figure 2 (in fact $C_c$ and $CFB$ are not mounted), the mathematical expression of the compensator $C(f)$ is:

**Equation 8**

$$C(s) = C_0 \frac{1 + \frac{j \cdot f}{f_{zc}}}{j \cdot 2 \cdot \pi \cdot f}$$

where:

**Equation 9**

$$C_0 = \frac{L \cdot fsw \cdot \left(1 - \frac{G_m}{C_7}\right) \cdot R_4}{V_{IN} - V_{OUT}}$$

and:

**Equation 10**

$$f_{zc} = \frac{1}{2 \cdot \pi \cdot R_3 \cdot C_7}$$

they are chosen in order to ensure the stability of the overall system.

The values of $H_{COMP} = \delta V_{COMP}/\delta I_{COMP}$ and of $G_m$ (error amplifier transconductance) are specified in the Viper06 datasheet.
### 7.2 Compensation procedure for a DCM buck

The first step is to choose the pole and zero of the compensator and the crossing frequency.

In this case $C(f_c)$ has only a zero ($f_{zc}$) and a pole at the origin, thus a possible setting is:

- $f_{zc} = k \cdot f_p$
- $f_{cross} = f_{cross\_sel} \leq \frac{f_{sw}}{10}$

where $k$ is chosen arbitrarily. A starting point could be $k = 5$

After selecting $f_{cross\_sel}$, $G_1(f_{cross\_sel})$ can be calculated from Equation 2 and, since by definition it is $|C(f_{cross\_sel}) \cdot G_1(f_{cross\_sel})| = 1$, $C_0$ can be calculated as follows:

**Equation 11**

$$C_0 = \frac{\frac{2 \cdot \pi \cdot f_{cross\_sel}}{1 + \frac{f_{cross\_sel}}{f_{zc}}} \cdot \frac{H_{COMP}}{|G_1(f_{cross\_sel})|}}$$

At this point the Bode diagram of $G_1(f) \cdot C(f)$ can be plotted, in order to check the phase margin for the stability.

If the margin is not high enough, another choice should be made for $k$ and $f_{cross\_sel}$, and the procedure is repeated.

When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated as follows:

from **Equation 9**

**Equation 12**

$$C_7 = \frac{L \cdot f_{sw}}{V_{IN} - V_{OUT}} \left( \frac{L \cdot G_m}{C_0} \right) \cdot \frac{R_4}{R_4 + R_5}$$

and from **Equation 10**

**Equation 13**

$$R_3 = \frac{1}{2 \cdot \pi \cdot f_{zc} \cdot C_7}$$

Quantities found in **Equation 12** and **Equation 13** are suggested values. Commercial values are chosen, let us call them $C_7\_act$, $R_7\_act$, resulting into $f_{zc\_act}$.

**Equation 14**

$$f_{zc\_act} = \frac{1}{2 \cdot \pi \cdot R_3\_act \cdot C_7\_act}$$

$C_0$ value is also recalculated from **Equation 9**
Equation 15

\[ C_{\text{act}} = \frac{L \cdot f_{\text{sw}}}{V_{\text{IN}} - V_{\text{OUT}}} \cdot \left( \frac{|G_{\text{m}}|}{C_{\text{7,act}}} \right) \cdot \frac{R_{\text{4,act}}}{R_{\text{4,act}} + R_{\text{5}(4)_{\text{act}}}} \]

and the compensator becomes:

Equation 16

\[ C_{\text{act}}(f) = \frac{C_{\text{act}}}{H_{\text{COMP}}} \cdot \frac{1 + \frac{f}{f_{\text{zc,act}}}}{j \cdot \frac{f}{2 \cdot \pi} \cdot \frac{f}{f_{\text{zc,act}}}} \]

At this point the Bode diagram of \( G_1(f) \cdot C_{\text{act}}(f) \) should be plotted, and check if the phase margin for the stability is maintained.

8 Thermal measurements

A thermal analysis of the evaluation board in full load condition at \( T_{\text{AMB}} = 25 \, ^\circ\text{C} \) has been performed using an IR camera. The results are shown in the following figures.

Figure 32. Thermal measurement @ \( V_{\text{IN}} = 80 \, V_{\text{AC}} \), full load (130 mA) \( R_{\text{bl}} = 8.2 \, \text{kohm} \)
Figure 33. Thermal measurement @ $V_{IN} = 115\, V_{AC}$, full load (130 mA) $R_{bl} = 8.2\, \text{kohm}$

Figure 34. Thermal measurement @ $V_{IN} = 230\, V_{AC}$, full load (130 mA) $R_{bl} = 8.2\, \text{kohm}$
Figure 35. Thermal measurement @ $V_{\text{IN}} = 265 \, V_{\text{AC}}$, full load (130 mA) $R_{\text{bl}} = 8.2 \, \text{kohm}$
9 EMI measurements

A pre-compliant test of the EN55022 (Class B) European normative has been performed using an EMC analyzer and an LISN. The average EMC measurements at 115 V\textsubscript{AC}/full load and 230 V\textsubscript{AC}/full load have been performed and the results are shown in Figure 36 and Figure 37.

**Figure 36. Average measurement at full load, 115 V\textsubscript{AC}**

![Figure 36](image1)

**Figure 37. Average measurement at full load, 230 V\textsubscript{AC}**

![Figure 37](image2)
Appendix A  Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

*Figure 38* shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the efficiency of converter, which has been measured in different input/output conditions.

### A.1 Measuring input power

With reference to *Figure 38*, the UUT input current causes a voltage drop across the internal shunt resistance of ammeter (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch of *Figure 38* is in position 1 (see also the simplified scheme of *Figure 39*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in light load condition).
In case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in Figure 38 can be changed to position 2 (see simplified scheme of Figure 40) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

On the other hand, the position of Figure 40 may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is recommended the setting of Figure 39 to be used for light load measurements and Figure 40 for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.
After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and measurements can be recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured overtime for both AC input and DC output.

Some wattmeter models allow the integration of the measured input power in a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is calculated dividing by the integration time itself.
10 References

## Revision history

Table 5. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>30-May-2013</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>25-Jul-2013</td>
<td>2</td>
<td>Updated: Figure 5, Figure 6, Figure 7, Figure 8, Figure 19, Figure 21, Figure 23, Figure 24, Figure 25, Figure 26, Figure 27, Figure 28, Figure 29 and Figure 30.</td>
</tr>
<tr>
<td>23-May-2014</td>
<td>3</td>
<td>Changed the title in cover page. Updated Table 2.</td>
</tr>
<tr>
<td>15-Dec-2014</td>
<td>4</td>
<td>Updated Equation 8, Equation 11 and Equation 16.</td>
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</table>
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