

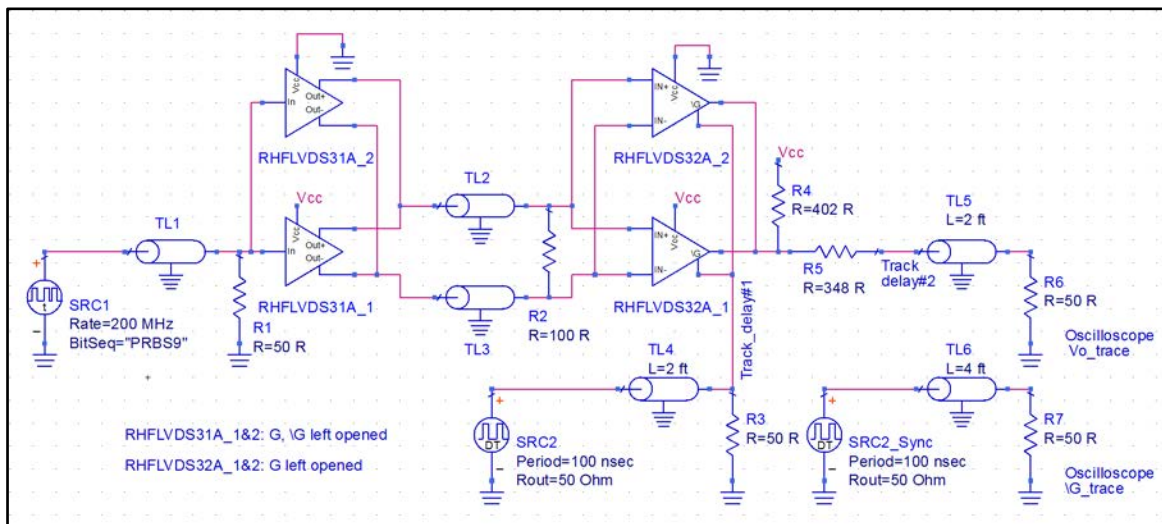
Start time of the RHFLVDS32A receiver

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Introduction

This application note describes the delay it is necessary to wait before data become available at the receiver output of the RHFLVDS32A. To explain this example, *Figure 1* shows a full data link transmission schematic where the RHFLVDS31A and RHFLVDS32A devices are implemented in cold spare mode.

Figure 1: Cold spare, full data link implementation



1. Most of the TL lengths are balanced, both for the RHFLVDS31A_2 and RHFLVDS32A_2 data link (TL2 and TL3) and the measurement utilities (TL4, TL5, and TL6).
2. The length of TL6 simulates a replica of the global delay introduced by the setup (TL4 length compensation).
3. SRC1 is a continuous high speed data source.
4. SRC2 performs the enable control of the RHFLVDS32A_2 and RHFLVDS32A_1 receivers.
5. Only \IG should be considered as the active control line of the RHFLVDS32A_1.

1 Data transmission description

The rad-hard, quad RHFLVDS31A driver and RHFLVDS32A receiver of STMicroelectronics are designed to be used in cold spare mode. This means that a spare operating unit can be connected in parallel to a main operating unit for all pins except Vcc. The Vcc power input of each cold spare unit is tied to ground. In this case, the cold spare feature guarantees that no change in performance occurs compared to the situation when only a single operating unit is used. In [Figure 1](#), the spare operating units are RHFLVDS31A_2 and RHFLVDS32A_2 and the main operating units are RHFLVDS31A_1 and RHFLVDS32A_1.

The suggested data transmission example uses only one of the four cells of each driver and receiver device. The cold spare units RHFLVDS31A_2 and RHFLVDS32A_2 are connected through transmission lines TL2 and TL3. These lines carry the differential data to a target destination of 100 Ω . The data comprise a PRBS9 signal running at 200 MHz.

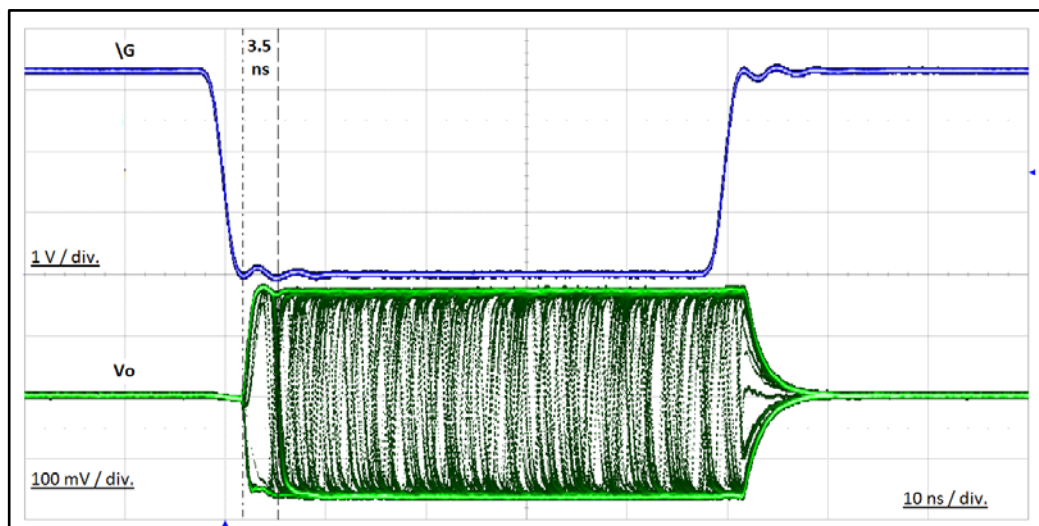
By switching the enable control at a convenient rate on the receiver side of [Figure 1](#), it is possible to obtain a full screening of the output behavior (single-ended CMOS). To achieve this, a 100 ns square signal is applied on the \G input pin of the two receivers (RHFLVDS32A_2 and RHFLVDS32A_1).

The receiver output is prepared for a high impedance state when it is disabled. Output matching is performed thanks to a simple voltage divider which uses a 50 Ω oscilloscope input load. Correct coaxial lengths are included in the measurement chain, to control for delay compensations (i.e. the sum of track delays in the order of 800 ps on the board being used). This implementation is necessary to synchronize the divided output (Vo trace), as well as to display correct timings.

[Figure 2](#) shows:

- \G (upper trace): a perfect replica of the applied enable control of the receivers (RHFLVDS32A_2 and RHFLVDS32A_1).
- Vo (lower trace): a fraction of the output signal, recorded using infinite persistence mode of the oscilloscope to display the PRBS9 data better.

Figure 2: Start time of the RHFLVDS32A_2 and RHFLVDS32A_1 receivers



1. The hatched vertical bars show $\Delta T = 3.5$ ns.

Analysis of the output data demonstrates that after the receivers have been enabled, there is an intrinsic dead time or "delay" before data acquisition begins. This feature, which is called the "start time of the RHFLVDS32A", is typically 3.5 ns. It is mandatory to take this 3.5 ns delay into account before data acquisition whether cold spare implementation has been used or not.

2 Revision history

Table 1: Document revision history

Date	Revision	Changes
14-Feb-2014	1	Initial release

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