AN4337
Application note

The avalanche issue: comparing the impacts of the I_{AR} and E_{AS} parameters

By Vittorio Giuffrida

Introduction

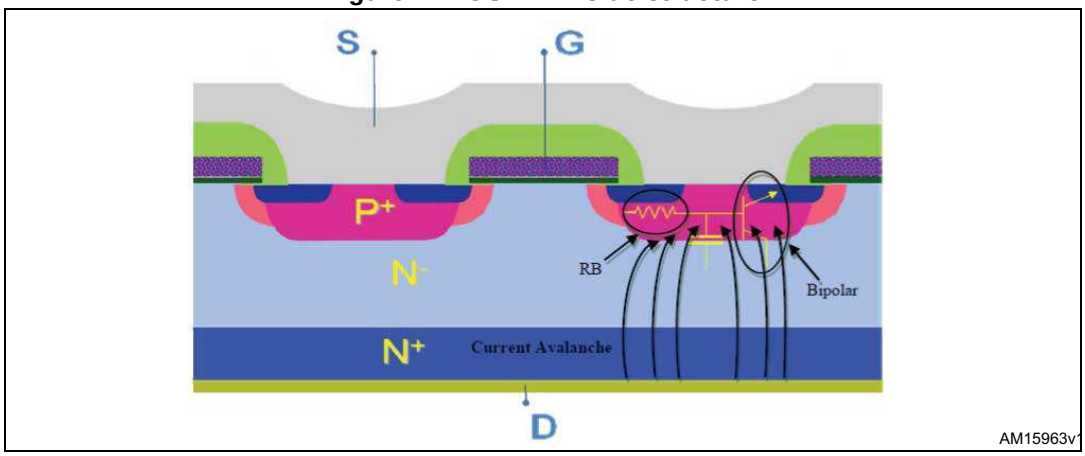
Generally, power MOSFETs are considered rugged with respect to the avalanche phenomenon, however, the quantification of the level of ruggedness depends on the I_{AR} avalanche current and E_{AS} avalanche energy. These two parameters determine the capacity of a MOSFET to be safe during the avalanche. This paper explores the theory of the avalanche effect in a flyback converter, in order to understand how the I_{AR} and E_{AS} parameters affect MOSFET operation and, consequently, how to manage a voltage overshoot higher than the $V_{(BR)DSS}$ absolute maximum rating.

Contents

1 Avalanche failure mode

Power MOSFETs have an intrinsic bipolar transistor in their structure. This vertical device, as illustrated in *Figure 1*, consists of the P+ diffusion, the N- epitaxial layer and the N+ substrate with the base-emitter junction shorted by the source metalization, forming the “Body Diode”. At the OFF-state, this non-symmetrical structure is reverse bias. The maximum reverse bias voltage that can be applied to a p-n body diode is limited by breakdown. When the applied voltage exceeds breakdown, a critical electrical field is reached and the carriers in the transition region are consequently accelerated to energies sufficient to free electron-hole pairs via collisions with bound electrons. This mechanism, known as Avalanche phenomenon, causes an electrical current multiplication that can allow very large currents within materials. Basically, the breakdown mechanism is not destructive for a p-n junction, however, heating caused by the large breakdown current and high breakdown voltage can damage a MOSFET device. In particular, two mechanisms can generate the failure of MOSFETs. The first one occurs because of the creation of thermally generated carriers in the epitaxial/bulk region and hence the creation of hot spots. The second one depends on the avalanche current: if this current creates an increasing voltage drop across the RB resistor (see *Figure 1*) sufficient to forward bias the parasitic BJT, it turns on, with potentially catastrophic results as control of the switch is lost. Due to these “failure modes”, the E_{AS} and I_{AR} parameters have been defined and inserted in the datasheets as absolute maximum ratings. E_{AS} is the maximum avalanche energy that can be dissipated in the device during a single avalanche operation, while I_{AR} is the maximum avalanche current without any bipolar latch up.

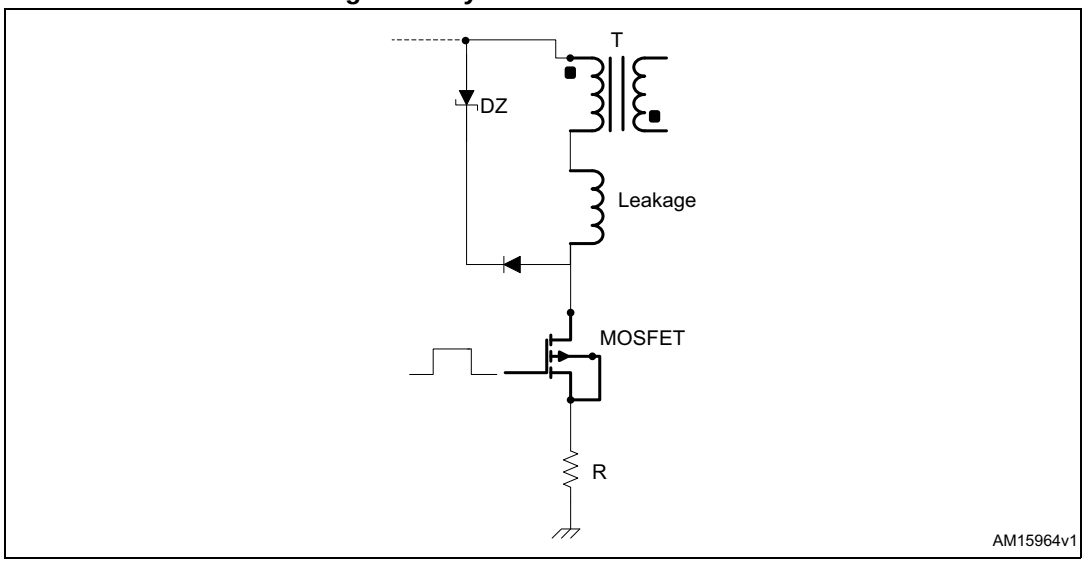
Figure 1. MOSFET inside structure



2 Avalanche phenomenon in the flyback converter

Basically, the application designers don't allow the avalanche operation in a MOSFET device; instead, the voltage across the drain-source is maintained at around 80-90% of $V_{(BR)DSS}$. However, in some cases greater voltage spikes can occur; one such example is the flyback converter.

Figure 2. Flyback circuit schematic

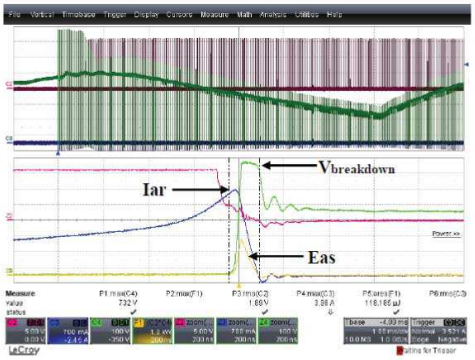


In the flyback converter, the basic issue is the presence of various leakage inductance points in the transformer. If the inductor energy is not properly clamped, during MOSFET turn-off, the leakage inductance causes voltage overshoots that can exceed the $V_{(BR)DSS}$ absolute maximum rating of the MOSFET device. In particular when the MOSFET turns off, the magnetic fields collapse and the voltage across the inductances reverses because the current cannot interrupt suddenly. Since the leakage inductance doesn't participate in this energy transfer, it cannot find a circulating path and thus generates a large positive spike on the MOSFET drain. Therefore, the drain-source voltage is $V_{ds}=V_{leakage} + V_{in} + V_{flyback}$, where $V_{flyback}$ is the reflected output voltage.

In these conditions, if the avalanche phenomenon occurs, I_{AR} avalanche current and E_{AS} avalanche energy needs to be monitored.

Below is a typical waveform of the avalanche phenomenon occurring in a flyback converter during the start up phase.

Figure 3. Details of avalanche phenomenon



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3 I_{AR} and E_{AS} electrical thermal approach

The following section provides step-by-step guidelines on how to achieve the right trade-off between performance and safety margin in terms of I_{AR} and E_{AS} specifications when a MOSFET operates in a flyback converter. We essentially explain how to approach the avalanche phenomenon in order to understand if a MOSFET device can function safely.

3.1 E_{AS} power/thermal evaluations

The E_{AS} single pulse avalanche rating in the datasheet is based on the assumption that the device can sustain an avalanche if the starting case temperature is 25 °C and if a specific value of ID is set.

The first step is to evaluate the maximum energy that the MOSFET must dissipate during the single avalanche phenomenon. As previously mentioned, in the flyback converter, the voltage spike across the drain-source of the MOSFET grows until the maximum $V_{(BR)DSS}$ is reached. In the absence of an external clamping network, we estimate the amount of energy E_{lk}, due to the leakage inductance, dissipated in the power device.

Equation 1

$$E_{lk} = \int_0^{\Delta t} Id(t)Vds(t)dt = \frac{1}{2} I_P \cdot BVD_{ss} \cdot \Delta t$$

Where

Equation 2

$$\Delta t = \frac{L_{lk} \cdot I_P}{BVD_{ss} - V_{out}N}$$

Equation 3

$$E_{lk} = \frac{1}{2} I_P^2 \cdot L_{lk} \frac{BVD_{ss}}{BVD_{ss} - V_{out}N}$$

For example, consider the 650 V/5.4 A device shown below:

Table 1. Electrical rating, absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	650	V
I_D	Drain current (continuous) at T_{case}= 25ºC	5.4	A
I_{AR}	Avalanche current repetitive or not repetitive (pulsed width limited by $T_{j\ max}$)	5.4	A
E_{AS}	Single pulse avalanche energy (starting T_j=25ºC, I_D=I_{AR}, V_{DD}=50V)	100	mJ

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case max	4.17 (TO-220FP)	°C/W
R_{thj-a}	Thermal resistance junction-ambient max	62.5	°C/W

With the following conditions derived from 30 W flyback converter:

- Maximum avalanche current Ip=4 A.
- Starting temperature 25 °C.
- Primary inductance value Lprimary=550 µH.
- Leakage inductance ~ 13 µH.
- Transformer ratio N=2.
- Output voltage Vout=48 V

In these conditions, the energy due to the leakage inductance is 123 µJ. This is the maximum avalanche energy that the MOSFET device must sustain during breakdown. If we presume the case temperature to be fixed at 25 °C, we can estimate the temperature increase due to the avalanche single pulse power dissipation via the following equation:

Equation 4

$$\Delta T_{j-c} = Zth_{j-c} \cdot \sqrt{2} \frac{E_{avalanche}}{\Delta t}$$

Where Δt ~ 100 ns is the avalanche pulse duration (*Equation 2*).

With:

Equation 5

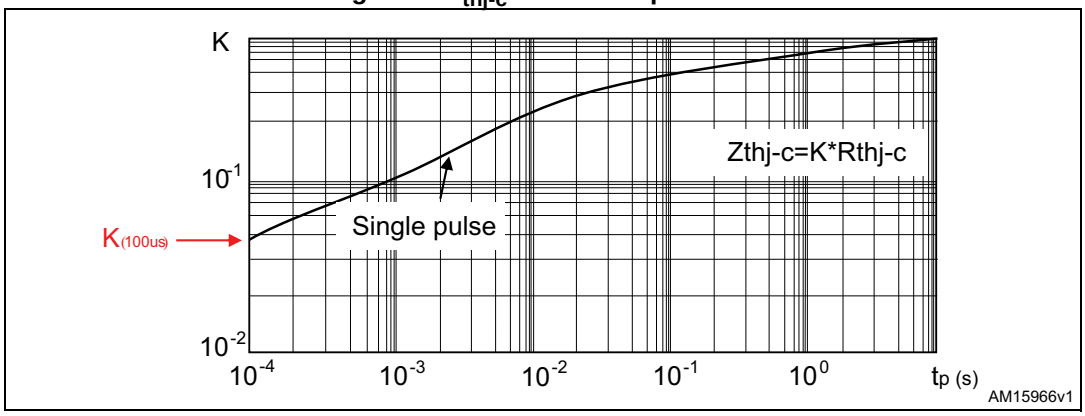
$$Zth_{j-c}(\Delta t) = K(\Delta t) \cdot Rth_{j-c}$$

K thermal transient depends on the duration of the pulse. It can be estimated through the thermal impedance curve using the following equation:

Equation 6

$$K_{(100ns)} = K_{(100\mu s)} \cdot \sqrt{\frac{100ns}{100000ns}}$$

Figure 4. Z_{thj-c} thermal impedance



The temperature increase due to avalanche and the final junction temperature is:

Equation 7

$$\Delta T_{j-c} = Zth_{j-c} \cdot \sqrt{2}\frac{E_{avalanche}}{\Delta t} = 8.7°C$$

Equation 8

$$T_j = T_c + 8.7 = 33.7°C$$

In these working conditions, the MOSFET device (as *Table 1* and *2*) is safe since the final junction temperature and the maximum avalanche energy are much lower than data specifications.

At this point we can calculate the repetitive avalanche energy pulses in order to understand how many pulses are necessary to raise the junction temperature from an initial 25 °C to the maximum specification (T_j=150 °C).

From the following equation:

Equation 9

$$\Delta T_{j-a(\max)} = \sqrt{2}\frac{E_{avalanche}}{\Delta t}\left(\frac{\Delta t}{T} Zth_{j-a}(\tau) + \left(1-\frac{\Delta t}{T}\right)Zth_{j-a}(\Delta t)\right)$$

We have:

Equation 10

$$Zth_{j-a}(\tau) = \frac{T\left[\Delta T_{j-a(\max)} - \left(1-\frac{\Delta t}{T}\right)Zth_{j-a}(\Delta t)\cdot\sqrt{2}\frac{E_{avalanche}}{\Delta t}\right]}{\sqrt{2}E_{avalanche}}$$

Since the Δt duration of a single pulse is very short, we have:

Equation 11

$$Zth_{j-a}(\Delta t) = Zth_{j-c}(\Delta t) = 0.05°C/W$$

Hence, for a period T=20 µs, using *Equation 5* we obtain:

Equation 12

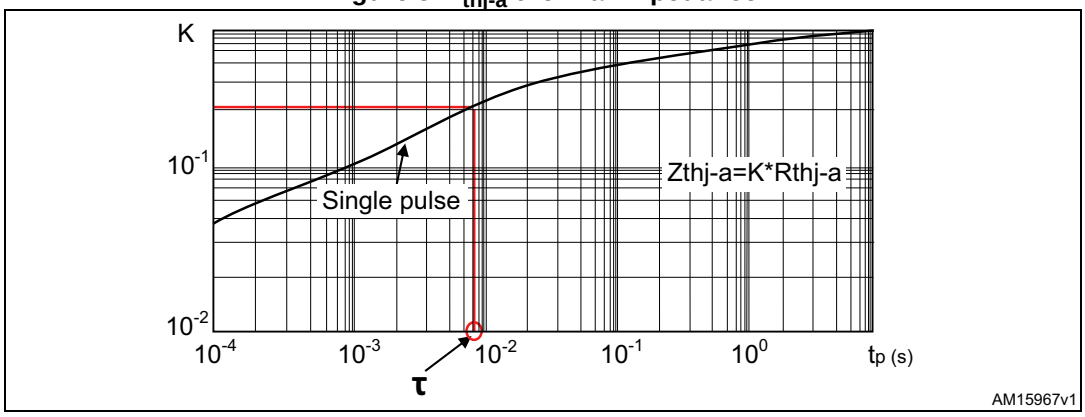
$$Zth_{j-a}(\tau) = \frac{20us\left[125°C - (1 - \frac{100ns}{20us}) \cdot 0.005°C/W \cdot \sqrt{2} \cdot 1230W\right]}{\sqrt{2} * 123uJ} = 13.38°C/W$$

So, in conclusion:

Equation 13

$$k(\tau) = \frac{Zth_{j-a}(\tau)}{Rth_{j-a(\max)}} = \frac{13.38°C/W}{62.5°C/W} = 0.214$$

Figure 5. $Z_{thj\text{-}a}$ thermal impedance



Therefore, the MOSFET device is safe if the duration of repetitive avalanche energy pulses is less than τ=7 ms.

Below, a specific example illustrates how to estimate the quantification of the safety margin for a MOSFET in terms of E_{AS} single pulse avalanche energy.

Using the same previous conditions derived from 30 W flyback converter, we can calculate the theoretical maximum current (not accounting for the instant I_{AR} parameter) and maximum leakage inductance, taking into account the E_{AS}=100 mJ fixed value data specification.

From *Equation 3* we have:

Equation 14

$$I_{P(\max)} = \sqrt{\frac{2E_{as} \cdot (BVD_{ss} - V_{out}N)}{L_{lk} \cdot BVD_{ss}}} \Rightarrow I_{P(\max)} = 114A$$

With E_{AS}=100 mJ and L_{lk}=13 µH.

Equation 15

$$L_{lk(\max)} = \frac{2E_{as} \cdot (BVD_{ss} - V_{out}N)}{I_P^2 BVD_{ss}} \Rightarrow L_{lk(\max)} = 5.8mH$$

With E_{AS}=100 mJ and Ip=5.4 A (data specifications).

Note that specifying E_{AS}=100 mJ results in $I_{p(max)}$ current and $L_{lk(max)}$ leakage inductance being much higher than typical values for real flyback converters. This means that, apart

from the application, it is rather improbable that a MOSFET device will fail for E_{AS} single pulse avalanche energy.

This approach suggests that during an avalanche phenomenon, the I_{AR} parameter should be addressed rather than the E_{AS} one.

3.2 I_{AR} electrical evaluations

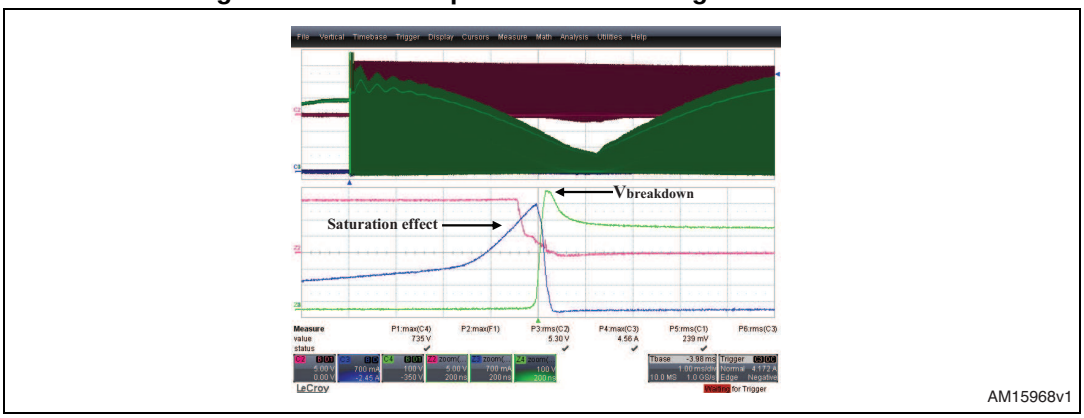
I_{AR} parameter defines the maximum avalanche current without any bipolar latching phenomenon. This parameter doesn't depend on the avalanche energy, which means the MOSFET device is safe if the avalanche energy is lower than the E_{AS} datasheet specification and the avalanche current is lower than I_{AR} absolute maximum rating; vice versa, the MOSFET is certainly safe if the maximum avalanche current is lower than I_{AR}. This last assertion is validated by the result of *Equation 15*; in fact, any leakage inductance in a real flyback converter can have the value of 5.8 mH.

As already mentioned, this suggests that the avalanche current parameter needs to be monitored more than avalanche energy.

The worst case scenario during the avalanche phenomenon is when the ferromagnetic core of the flyback transformer becomes saturated. Due to the uncontrolled saturation effect, the current peak may be very high and hence dangerously close to the I_{AR} specification.

Below is a waveform with typical saturation phenomenon during the avalanche.

Figure 6. Saturation phenomenon during the avalanche

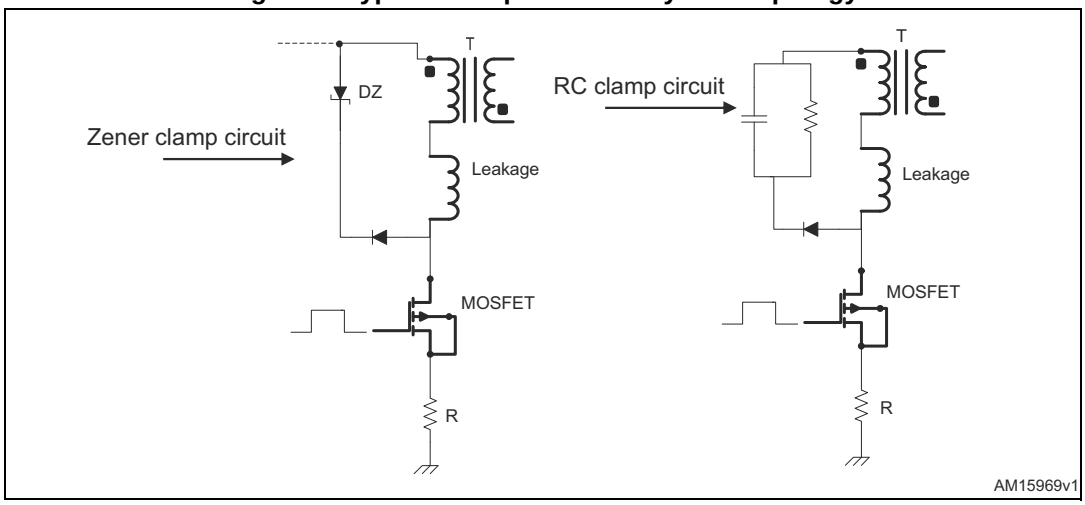


In this condition, two methods exist to increase the safety margin in terms of I_{AR} avalanche current.

The first one is to optimize the driving and the network circuit in order to avoid the avalanche phenomenon. The snubber increase, a different clamp circuit and/or input capacitance increase can satisfy this requirement.

Here some examples:

Figure 7. Typical clamp circuit of flyback topology



The second one is to choose a flyback transformer with ferromagnetic core features such that the saturation current value is higher, thus limiting the uncontrolled effect of the saturation.

However, if the geometry of the flyback transformer cannot be changed, we suggest optimizing the transformer by introducing a gap in the ferromagnetic core. In this way, the saturation phenomenon is reduced since the leakage inductance is slightly increased. Due to this increase in the leakage inductance, the electrical efficiency of the system could decrease slightly, but the safety margin in terms of the I_{AR} avalanche current increases, thus satisfying the initial objective.

4 Conclusions

Understanding how to approach a voltage overshoot which exceeds the $V_{(BR)DSS}$ absolute maximum rating is the key to designing reliable and, consequently, safe MOSFETs. The example in this paper provides step-by-step guidelines on how to obtain the safety margin in terms of I_{AR} and E_{AS} specifications when a MOSFET functions in a flyback converter. In particular, this example suggests that a MOSFET device is safe if the avalanche energy is lower than the E_{AS} datasheet specification and the avalanche current is lower than the I_{AR} absolute maximum rating; vice versa, a MOSFET is certainly safe if the maximum avalanche current is lower than I_{AR}.

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
05-Jun-2014	1	Initial release.