AN4414
Application note

Anti-tampering ferrite less power supply for 3-phase energy meter

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Introduction

This power supply design is dedicated to energy meter applications and an other low power auxiliary supply for systems with galvanic isolation for a single phase or 3-phase input mains supply. The SMPS can cater the super wide input voltage ranging 90 VAC to 440 VAC single phase or 3-phase / 4-wire configurations with low component counts. For energy meter applications, anti-tampering feature is a must nowadays which is governed by electricity board regulatory agencies.

Normally the SMPS are designed with ferrite cores, either a flyback transformer or a buck inductor, which saturates in an environment where strong magnetic fields are available. To avoid the same, some type of magnetic shielding are required, which adds a cost and complexity in manufacturing process of the magnetics. In case of tampering where SMPS are available in energy meters, commonly a strong magnetic field of about 0.5 Tesla strength is applied, which interfaces with the ferrite core and saturates it. Due to saturation, sometimes the failure of power devices may also take place, or the SMPS with integrated switches gets into the protection mode and limiting the output voltage, consequently the meter stops which is a tempered condition.

To overcome this situation, in the present case, an example to design the flyback converter without using any ferrites or a high permeability core for a required magnetizing inductance and so called an air core magnetic approach is described in this application note. If no ferrites are involved, no saturation phenomenon can take place under the influence of an external strong magnetic field and this will comply the energy meter anti-tampering standard, which requires 0.5 Tesla magnetic immunity. The only drawback could be the large number of turns and associated copper losses. Since the required power is very low, the copper losses are acceptable up to a certain extent. The specification of overall input power to be within the limits as per energy meter power supply specifications needs to be complied.

Contents

1 Description of SMPS

The front-end of the power supply comprises of a surge suppressor, rectifiers and a MOSFET as a series regulator. The 3-phase, 4-wire bridge rectification scheme is adopted so as to run the system in case of neutral missing. The input side is protected against spikes using suitable varistors. Then EMI filter is connected across the DC using an undamped LC filter (L1, C8 and C11) for both the common mode and differential mode suppression. The purpose of the voltage clamping circuitry is to protect the flyback stage against overvoltages for a better reliability and it comprises of an N-channel 2 Ω/600 V MOSFET Q1 and a self driven control circuit. The NTC limits the inrush current. The Zeners D5 and D6 regulate the DC bus to the input of the buck stage to about 345 - 350 VDC, while resistors R2, R5 and R7 provides enough of gate-source charge.

The flyback converter is built using an integrated power device - the VIPER17, one of the devices from the VIPer® plus family. Some of the device features are listed below:

- 800 V avalanche rugged power section
- PWM operation with frequency jittering for low EMI
- Operating frequency:
  - 60 kHz for L type
  - 115 kHz for H type
- Standby power < 50 mW at 265 VAC
- Limiting current with adjustable set point
- Adjustable and accurate overvoltage protection
- Onboard soft-start
- Safe autorestart after a fault condition
- Hysteretic thermal shutdown

The device is available in DIP-7 and SO-16 narrow packages as shown in *Figure 1*.

Figure 1. DIP-7 and SO-16 narrow package

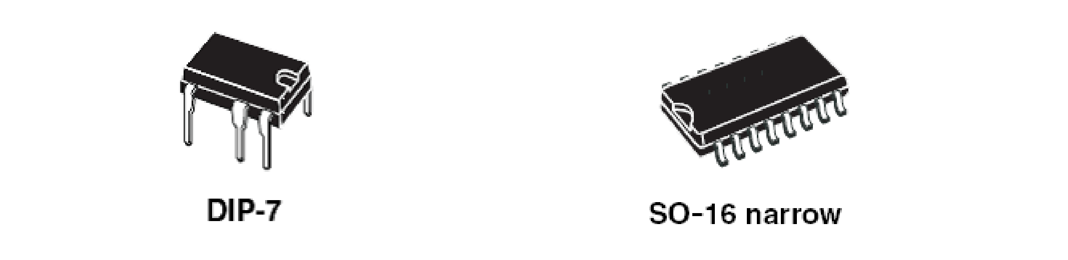


Table 1. Typical power capability of VIPER17

Part number	230 V_{AC}		85 - 265 V_{AC}	
	Adaptor(1)	Open frame(2)	Adaptor(1)	Open frame(2)
VIPER17	9 W	12 W	5 W	7 W

1. Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

The DC output voltage from the clamp circuit is filtered using a 4.7 µF capacitor C10 and supplied to the drain pin of the device. The VCC of the device is supplied through an auxiliary winding of the transformer (pins 1 - 2) and filtered by the capacitor C9. A decoupling capacitor can also be connected to the VCC pin for noise suppression. On the primary side of the transformer RCD clamp is being used using the R3, C3 and D3 to keep the leakage spike as low as possible. The feedback to the device is provided using the optocoupler U2 and TL431, U3 at the secondary side of the transformer. The voltage divider network R11 and R12 provides 2.5 V reference to the pin1 of the TL431. The power supply is designed for 5 V at 100 mA. The transformer primary inductance is sized to limit the peak current through the device below the maximum level. The output DC is filtered using low ESR capacitors C4 and C5. A post LC filter is also used to further scale down the ripple voltage to get ultimate 5 V output required for the microcontroller and other circuitry in the energy meter.

Some of the features of the VIPER17 like “BR” and “CONT” are not used here as the objective is to analyze the VIPER17 application with the air core transformer. Briefly these functions are explained below (Refer to the VIPER17 datasheet for more information on BR and CONT features):

- BR: the input voltage information is provided to the BR pin by using the resistor divider network from rectified bus voltage and can detect the brownout threshold to turn off the device. The resistor divider network R15, R16, R17 and R18 are programmed to achieve brownout protection.
- CONT: with the CONT pin, one can impose a limit on the peak drain current (Idlim can be programmed using the R14) and another feature is to have protection in case output overvoltage (output OVP protection), which can be sensed using the auxiliary winding which is used for VCC biasing.

Table 2. Specification of SMPS

Parameters	Limits
Input voltage range	90 - 440 VAC, 3-phase, 4-wire
Input supply frequency	50 Hz
Input / output isolation	Yes
Output voltage/current	5 V/100 mA
Total output power	0.5 W
Application/load	Metering, auxiliary power supply
Output voltage ripple	<100 mV (pk-pk)
Power factor correction	No
Topology/ devices	Flyback VIPER17HN, STD4NK60Z

1.1 Basic flyback equations

Generally the flyback design calculations are as below:

Equation 1

As we know:

$$V = L \times \frac{di}{dt}$$

Equation 2

Rewriting as below:

$$Vdcmin = Lp \times \frac{Ipkp}{Ton}$$

where:

Vdcmin = minimum DC input to flyback converter

Ipkp = peak primary current

Ton = turn-on time of primary switch (VIPer in this case).

Equation 3

$$Ton = Dmax \times Ts$$

Equation 4

$$Ton = \frac{Dmax}{fsw}$$

where:

Dmax = maximum duty cycle

fsw = operating switching frequency of converter.

Equation 5

$$Vdcmin = Lp \times \frac{Ipkp \times fsw}{Dmax}$$

Equation 6

$$Ipkp = \frac{Vdcmin \times Dmax}{Lp \times fsw}$$

As we know, power = energy transferred x frequency.

Equation 7

$$Pin = \frac{1}{2} \times Lp \times Ipkp^2 \times fsw$$

where *Pin* = input transformer power.

The primary inductance is calculated as:

Equation 8

$$Lp = \frac{2 \times Pin}{Ipkp^2 \times fsw}$$

Equation 9

$$Pin = \frac{Pout}{\eta}$$

where:

η = efficiency of flyback stage

Pout = output power required.

Equation 10

$$Lp = \frac{2 \times Pout}{\eta \times Ipkp^2 \times fsw}$$

Using *Equation 10*, we can rewrite *Equation 6* as:

Equation 11

$$Ipkp = \frac{2 \times Pout}{\eta \times Vinmin \times Dmax}$$

Reflected voltage is defined as:

Equation 12

$$VR = \frac{Dmax}{(1 - Dmax)} \times Vdcmin$$

RMS primary current is:

Equation 13

$$Iprms = Ipkp \times \sqrt{\frac{Dmax}{3}}$$

Turn ratio, n is defined as:

Equation 14

$$n = \frac{VR}{Vout + VF} = \frac{Np}{Ns}$$

where:

Np = number of primary turns

Ns = number of secondary turns.

1.2 Anti-tampering requirement

The E-meter SMPS requires a 0.5 T external magnetic immunity test and generally ferrites saturated with a 0.5 T external magnetic field. In order to comply this norm, a lot of attention is required in making proper shield transformers, which is very expensive and sometimes still difficult to comply the norms easily. The alternative to this is to adapt a ferrite less or air core transformer approach for such low power output requirement.

Considering the classical equations for a DCM (discontinuous conduction mode) flyback converter as described in *Section 1.1: Basic flyback equations* will result in a higher magnetizing inductance of primary of transformer. So using no ferrite material (we call this as “Air core”) to build the high frequency transformer would result in higher number of turns to achieve the required magnetizing inductance and with air core, the primary inductance in the range of 1 mH is itself difficult to achieve with reasonable number of primary turns.

So the first most important criterion to this approach is to select a low primary inductance value, Lp, but the value must be greater than a threshold in order not to cause an excess peak drain current. The high voltage flyback switcher is specified with a finite peak current of MOSFET, depending on its R_{ds_on} and thermal dissipation. Considering the VIPER17 family devices, we have this current as: Idlim = 0.4 A.

So during the wide mains operation, the peak primary current should be well below this value to avoid any protection to activate in a nominal operation. The VIPER17 has a hiccup mode activation above this current level.

As we know, the important parameters for a flyback design are:

Dmax = max duty cycle,

VR = reflected voltage,

Lp = primary inductance,

n = turn ratio, np/ns

Ipkp = peak primary current

fsw = switching frequency

Equation 15

Primary turns

$$Np = \frac{Lp \times Ipkp}{Bmax \times Ae}$$

where:

Ae = cross-sectional area of core chosen

As we know, selecting higher duty cycle will have below impact:

Equation 16

$$D\max \uparrow \rightarrow VR \uparrow \rightarrow n \uparrow \rightarrow Ipkp \downarrow \rightarrow Lp \uparrow$$

This clearly states that selecting a higher duty cycle at a minimum input voltage will cause the peak primary current to decrease and requires a high magnetizing inductance. To attain the required inductance, we will require a larger number of turns and the transformer would be very bulky if no high permeability ferrite material is used to require that inductance. Moreover the DCR of windings will increase due to a long wire length and copper losses will be more, impacting the efficiency and metering standard norms. For 3-phase metering, the power supply consumption should be limited below 8 VA.

Looking into the above challenges, we need to define a very low value of a maximum duty cycle and hence the peak primary (or drain current) at somewhat higher value. On the other hand, this would require lesser turn ratio (n) and there would be a large number of secondary turns in comparison with a traditional flyback transformer.

Note: Maximum primary peak (or a drain current of the device) < Idlim (maximum specified value in the VIPER17 datasheet).

As we know from *Equation 10*:

$$Lp = \frac{2 \times Pout}{\eta \times Ipkp^2 \times fsw}$$

that is:

Equation 17

$$Lp\alpha\frac{1}{fsw}$$

or

$$Lp\alpha\frac{1}{Bmax}$$

So one can use a higher switching frequency of the operation to maintain a lower inductance and hence a lower number of primary turns.

STMicroelectronics® has the VIPER17H for 115 KHz and the VIPER17L for 60 KHz operation.

Select VIPER17H for this application.

1.3 Calculations

Input voltage to converter: 80 V to 265 VAC

Maximum withstanding voltage: 440 VAC line-line.

Output voltage: Vout = 5 V

Maximum output current: Iout = 100 mA

Equation 18

$$Pout = Vout \times Iout$$

The typical power stage to withstand this wide mains operation is to clamp the DC bus voltage to the flyback stage at a lower level. This can be achieved by using a MOSFET and a Zener clamp circuit as a front-end stage as shown in the schematic in *Figure 9 on page 17*. This approach is a simple series pass regulator and well acceptable as we are dealing with a very low power output requirements. The DC input to the flyback stage doesn't exceed the voltage at which the Zener clamp network starts conducting and any further increase in an input rectified voltage will drop across the series MOSFET. Since the current in the MOSFET is very small, we can select a D^2PAK package in order to dissipate the heat on the copper area provided in the printed circuit board.

Minimum DC bus voltage at flyback input:

Equation 19

$$Vdcmin \sim 100\ VDC.$$

Maximum DC bus voltage at flyback input:

Equation 20

$$Vdcmax \sim 360\ VDC$$

Assuming efficiency, η = 65 % (flyback stage):

Equation 21

$$fsw = 115\ KHz$$

Equation 22

$$Ts = \frac{1}{fsw} = 8.69\mu s$$

Equation 23

Let $$VR = 10\ V$$

Equation 24

$$VR = \frac{Dmax}{(1 - Dmax)} \times Vdcmin = 10V$$

Equation 25

this gives $$Dmax = 9.1\%$$

$$Ton = Dmax = 790\ \mu s$$

Which is greater than Tonmin (= 400 ns), the device minimum turn-on time as per the datasheet of the VIPER17HN.

Equation 26

$$Ipkp = \frac{2 \times Pout}{\eta \times Vinmin \times Dmax} = 0.169A$$

Where the max. drain current limitation threshold of the VIPER17 is 400 mA, so at minimum DC input voltage, the device will not enter into the hiccup mode.

Equation 27

$$Lp = \frac{2 \times Pout}{\eta \times Ipkp^2 \times fsw} \sim 540\mu H$$

Case 1

Assuming Lp = 400 µH

Equation 28

as VR = 10 V,

so

Equation 29

$$n = \frac{VR}{Vout + VF} = 2 \text{ (ignoring VF)}$$

Np is two times of *Ns*.

Using a lesser diameter wire (DCR will obviously be high, but select in order to have it < 10 E in any case to avoid copper losses), a large number of turns can be accommodated in the available bobbin. Here we can consider the EE19 bobbin. Common practice to fix this type transformer specification is to wound primary turns as a selected AWG wire on the bobbin till the required inductance (*Lp*) is not achieved. Freeze *Np* at desired *Lp*. Select secondary turns, *Ns* = *Np* / *n* and auxiliary turns to maintain a minimum VCC bias voltage to the device.

With *Lp* = 400 µH and *Pout* = 0.5 W in *Table 3* are the test results:

Table 3. Test results

Vmains (VAC)	Ipkp (mA)	Turn-on time (ns)	Comments
80	175	700	-
120	210	Ton > Tonmin	-
180	290	Ton ~ Tonmin = 400	-
230	350	Ton ~ Tonmin = 400	-
265 and above	~ 400	Ton ~ Tonmin = 400	Device current reaches to Idlim and enters into hiccup mode

We can see that keeping the primary inductance as 400 µH, the drain current reaches to its internal limit threshold level, which is not desirable as the device activates the hiccup mode of operation at this current level, so we need to increase the primary inductance in reasonable limits to avoid higher drain current.

Case 2

Let's take Lp = 680 µH and increasing the reflected voltage slightly: VR = 18 V.

Equation 30

So

$$n = \frac{VR}{Vout + VF} = 3.2 \ \ (\text{considering} \ \ VF = 5V)$$

recalling the equation:

Equation 31

$$V = L \times \frac{di}{dt}$$

In our case

V = voltage at flyback input,

L = primary magnetizing inductance, Lp

and *dt* = turn-on time

With 680 µH as a primary inductance, let's analyze the flyback stage at different DC input conditions. At Vdcmin ~ 100 VDC (which is corresponding to 80 VAC), calculating the peak current through the device in a discontinuous conduction mode.

Equation 32

$$VR = \frac{Dmax}{(1 - Dmax)} \times Vdcmin = 18V$$

This gives:

Equation 33

$$Dmax = 15.2\%$$

Equation 34

$$Ton = Dmax \times Ts = 1.33 \ \mu s$$

Equation 35

$$Ipkp = \frac{Vdcmin \times Ton}{Lp} = 196mA$$

Looking into waveforms in *Figure 2* and *Figure 3.*, we have the same practical results. The waveforms are captured at different input voltage conditions.

As long as the turn-on time of the flyback switch is greater than its minimum turn-on time (internally fixed, 400 ns in the VIPER17), the device peak current is maintained as per the duty decided by the feedback loop. As input voltage increases and duty reduces in order “Tonmin” is achieved, there is no further decrease in turn-on time with a further increase in input voltage and the device peak current will increase as input voltage increases and it can be calculated using *Equation 35* at fixed Tonmin = 400 ns. Since the MOSFET clamp circuit ensures the maximum DC input to flyback as per the Zener biasing and maintains maximum input as 360 V till 440 VAC input mains, hence the peak current through the device is limited.

Looking into the waveform in *Figure 8*, at maximum mains input of 440 VAC (Vdcmax ~ 360 VDC to flyback input), the peak current through the device is 211 mA.

Equation 36

We have:

$$Ipkp = \frac{Vdcmax(Tonmin)}{Lp} = \frac{360V \times 400ns}{680\mu H} = 211mA$$

Figure 2. CH1: FB signal, CH3: drain current, CH4: drain source voltage at 100 VDC

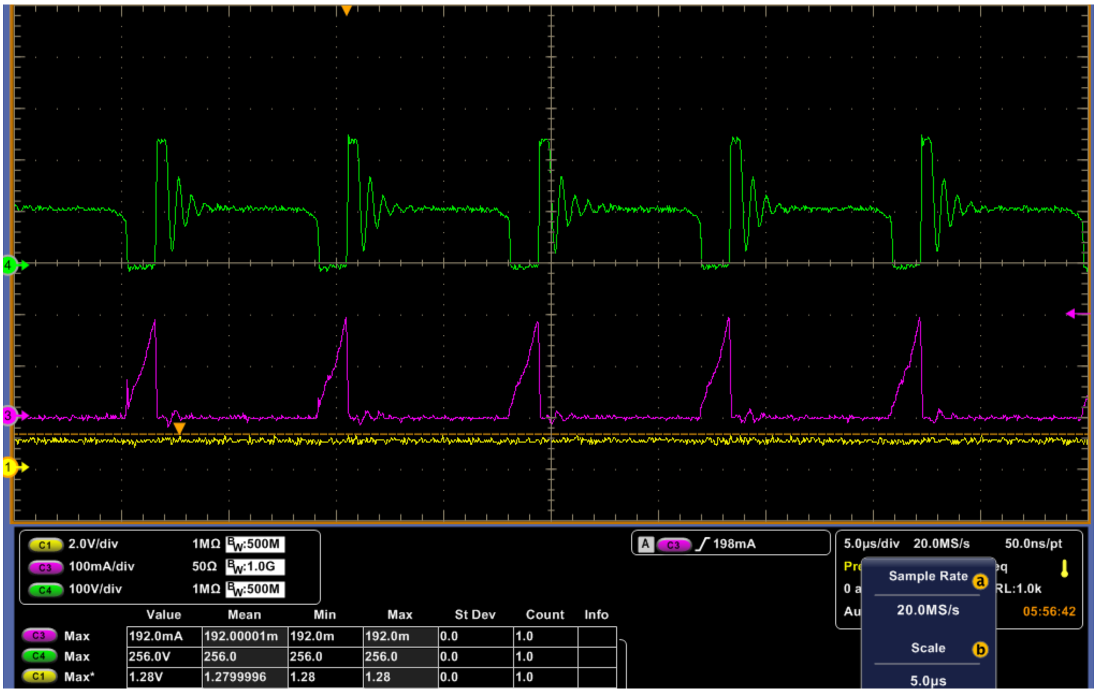
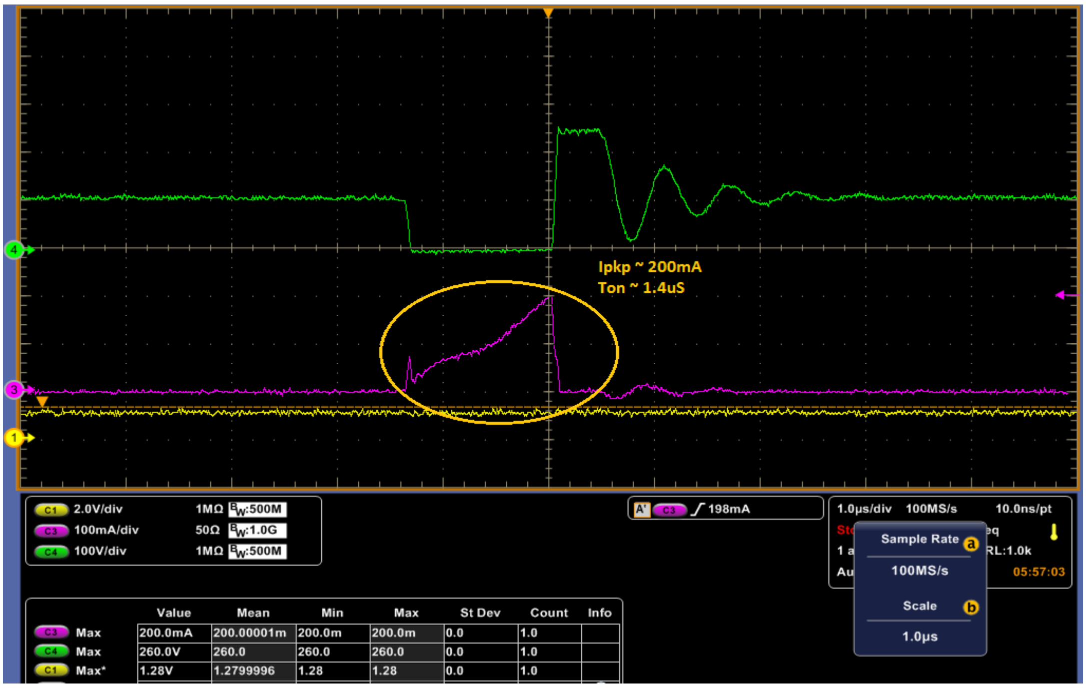
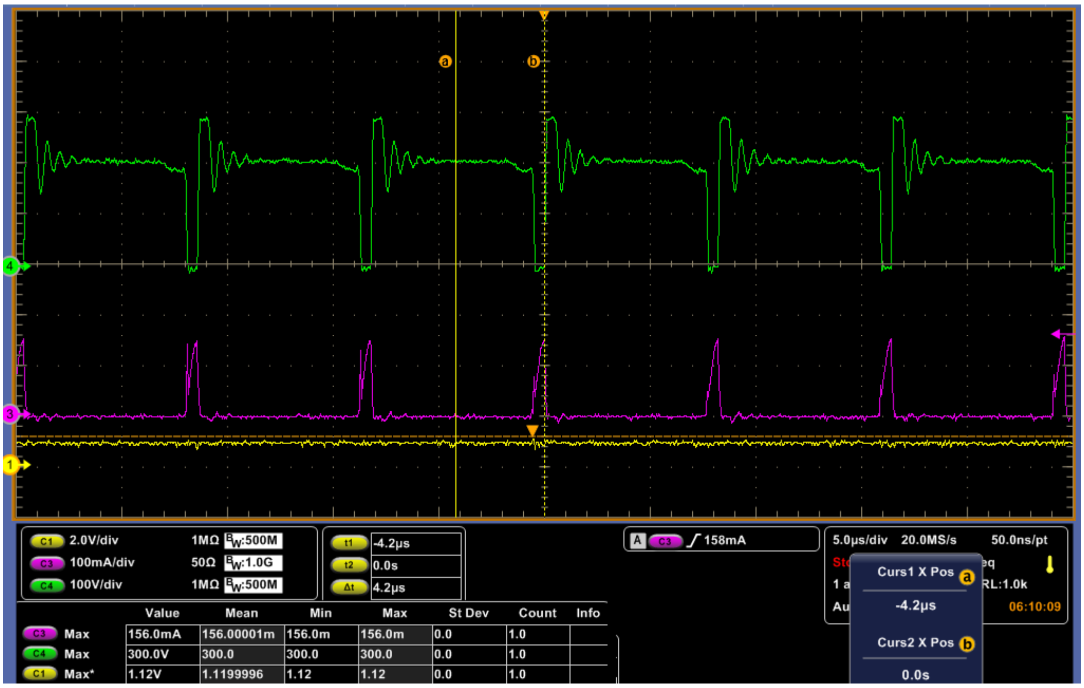


Figure 3. CH1: FB signal, CH3: drain current, CH4: drain source voltage at 100 VDC (expanded)



		Value	Mean	Min	Max	St Dev	Count	Info
C3	Max	200.0mA	200.00001m	200.0m	200.0m	0.0	1.0	
C4	Max	260.0V	260.0	260.0	260.0	0.0	1.0	
C1	Max*	1.28V	1.2799996	1.28	1.28	0.0	1.0	

Figure 4. CH1: FB signal, CH3: drain current, CH4: drain source voltage at 200 VDC



		Value	Mean	Min	Max	St Dev	Count	Info
C3	Max	156.0mA	156.00001m	156.0m	156.0m	0.0	1.0	
C4	Max	300.0V	300.0	300.0	300.0	0.0	1.0	
C1	Max*	1.12V	1.1199996	1.12	1.12	0.0	1.0	

Figure 5. CH1: FB signal, CH3: drain current, CH4: drain source voltage at 200 VDC (expanded)

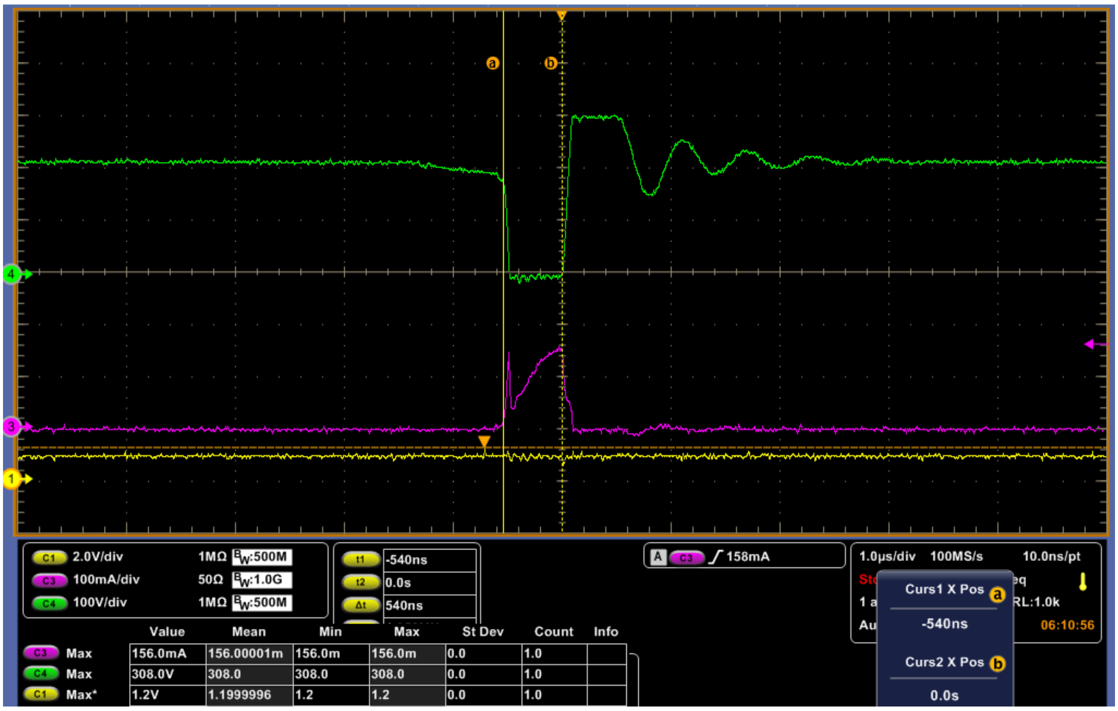


Figure 6. CH1: FB signal, CH3: drain current, CH4: drain source voltage at 300 VDC

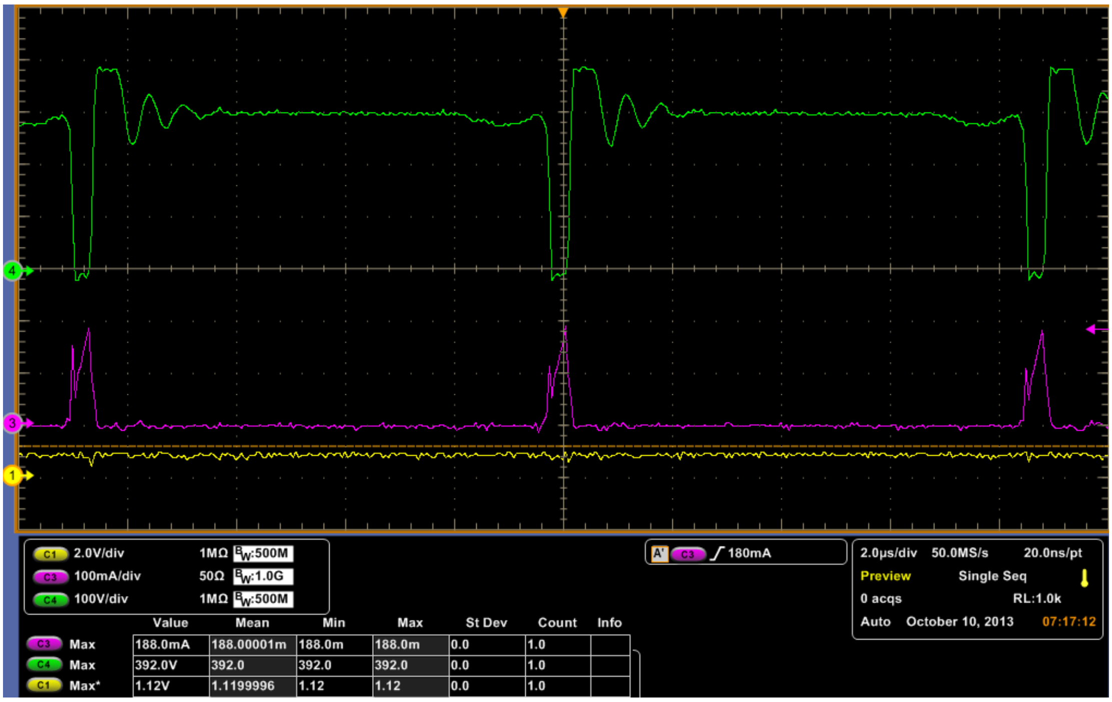


Figure 7. CH1: FB signal, CH3: drain current, CH4: drain source voltage at 300 VDC (expanded)

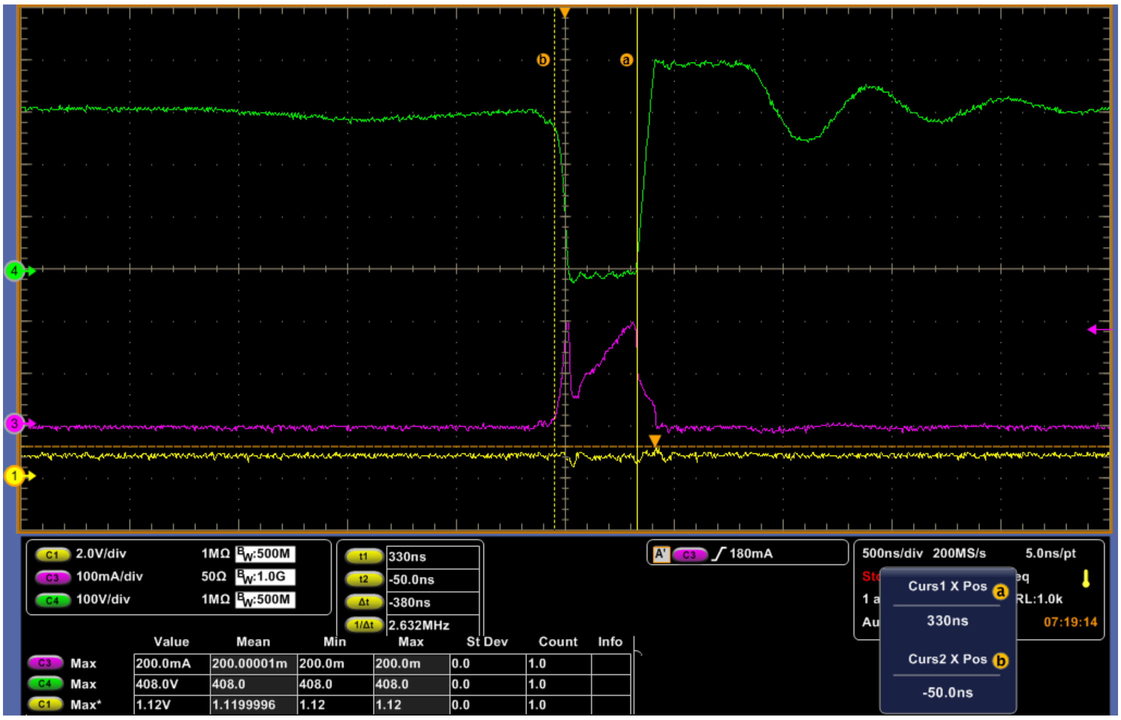


Figure 8. CH1: FB signal, CH3: drain current, CH4: drain source voltage at mains input VAC = 440 AC

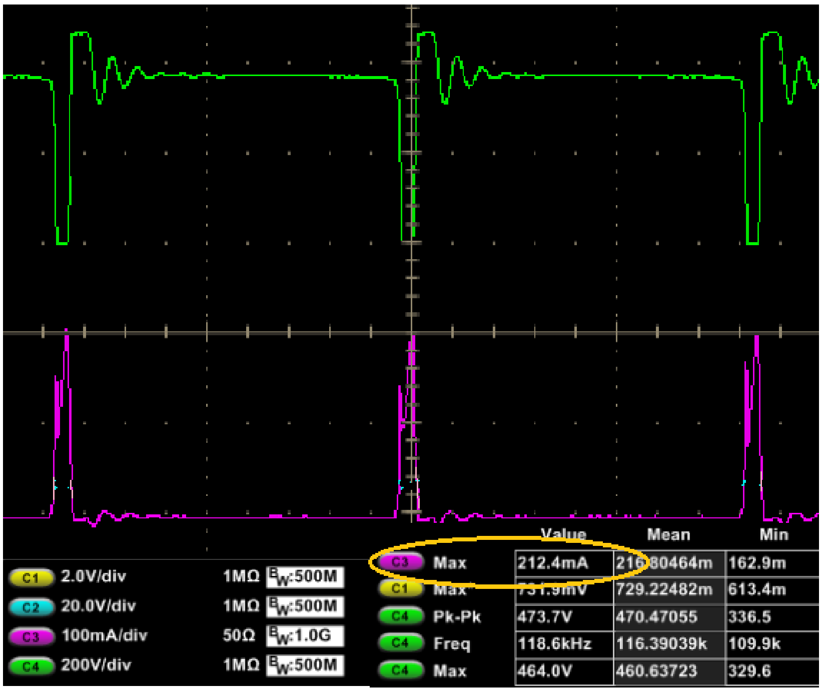


Figure 9. Schematic of SMPS

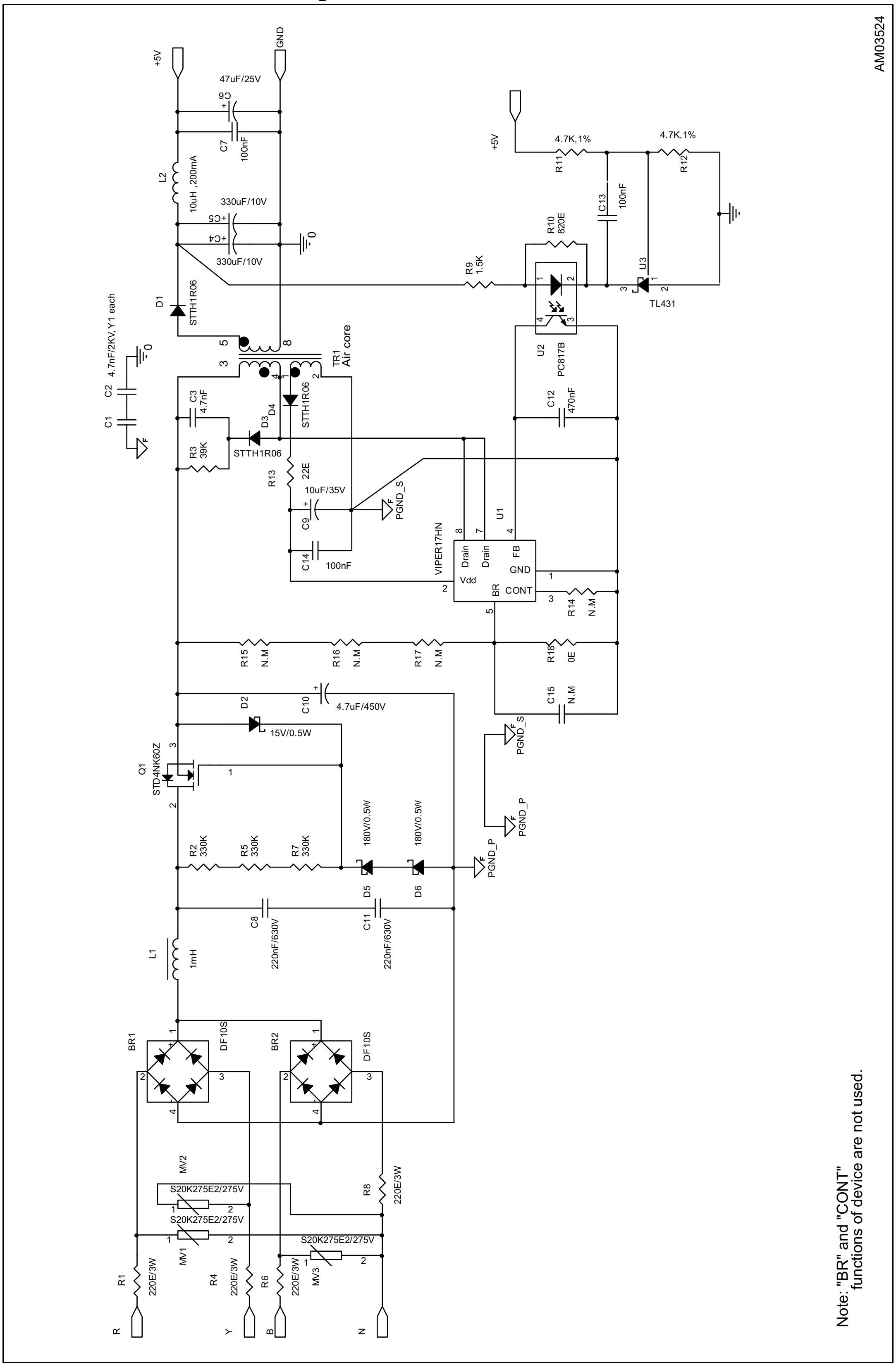


Table 4. Transformer specification

Parameters	Values
Max. output power	0.5 W
Input voltage range	80-440 VAC, 50 Hz
Primary inductance	680 µH
Secondary inductance	133 H
Primary side leakage inductance	< 5% at 1 KHz
Peak primary current	0.4 A max.
Switching frequency	115 KHz fixed
Bobbin size	EE19
Core type	Air core
Bobbin	8 pins vertical
Dielectric strength	2.75 KV

Table 5. Winding details

Winding name	Start	Stop	No. of turns	Wire gauge/DCR	Winding order
Np	4	3	345	0.2 mm / DCR = 6.5 Ω	Bottom
Ns	5	8	107	0.2 mm / DCR = 2.2 Ω	Above Np
Naux	1	2	200	0.09 mm / DCR = 22 Ω	Above Ns

Note: Proper Mylar tapes are inserted between each windings for isolation.

Table 6. Bill of material

Part reference	Quantity	Part description
U1	1	VIPER17HN
U3	1	TL431
Q1	1	MOSFET STD4NK60Z
D1, D3, D4	3	Rectifier STTH1R06

2 Reference

VIPER17 datasheet.

3 Revision history

Table 7. Document revision history

Date	Revision	Changes
21-Feb-2014	1	Initial release.