Introduction

This application note describes a 2-output, 5 W power supply set in BUCK topology with the VIPER26, a new STMicroelectronics offline, high voltage converter specifically developed for non-isolated SMPS.

The device features an 800 V avalanche rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, current limiting with adjustable set point, on-board soft-start, safe auto-restart after a fault condition and low standby power consumption.

The available protection includes thermal shutdown with hysteresis, delayed overload protection and open loop failure protection. All protection is auto-restart mode.
1 Adapter features

The electrical specifications of the board are listed in Table 1. The main output is 16 V/300 mA. A 5 V output able to supply up to 45 mA is obtained from the main output through a linear regulator.

Table 1. Electrical specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>$V_{IN}$</td>
<td>$[80 \text{ V}<em>{AC}; 280 \text{ V}</em>{AC}]$</td>
</tr>
<tr>
<td>Output voltage 1</td>
<td>$V_{OUT1}$</td>
<td>16 V</td>
</tr>
<tr>
<td>Max output current 1</td>
<td>$I_{OUT1}$</td>
<td>0.27 A</td>
</tr>
<tr>
<td>Output voltage 1 (through LDO)</td>
<td>$V_{OUT2}$</td>
<td>5 V</td>
</tr>
<tr>
<td>Max output current</td>
<td>$I_{OUT2}$</td>
<td>0.045 A</td>
</tr>
<tr>
<td>Precision of output regulation</td>
<td>$\Delta V_{OUT1_LF}$</td>
<td>± 5%</td>
</tr>
<tr>
<td>High frequency output voltage ripple</td>
<td>$\Delta V_{OUT1_HF}$</td>
<td>50 mV</td>
</tr>
<tr>
<td>Max ambient operating temperature</td>
<td>$T_{AMB}$</td>
<td>60 °C</td>
</tr>
</tbody>
</table>
2 Circuit description

The converter schematic is given in Figure 2. The input section includes a resistor R1 for inrush current limiting, a diode series D1 + D2 and a Pi filter (C1, L1, C2) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier, internally referenced to 3.3 V. The output voltage $V_{OUT1}$ can therefore be set through the R4-R5 voltage divider between the output terminal and the FB pin, according to the formula:

$$V_{OUT1} = 3.3V \cdot \left(1 + \frac{R5}{R4}\right)$$

...where R4 is split into R4a and R4b and R5 into R5a and R5b to allow better tuning of the output voltage value.

The compensation network is connected between the COMP pin (error amplifier output) and the GND pin and consists of C6, R3 and C7.

The Zener diode D5 protects against overvoltage when the output load is disconnected.

At power-up, the DRAIN pin supplies the internal HV start-up current generator that charges the C3 capacitor up to $V_{DDON}$ (13 V typical). At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C3 until $V_{OUT1}$ reaches its steady state value. When this occurs, the IC is supplied from $V_{OUT1}$ through the diode D6.
Figure 2. Application schematic
### 3 Bill of material (BOM)

#### Table 2. Bill of material

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
<th>Package</th>
<th>Manufacturer</th>
<th>RS code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cin</td>
<td>100 nF</td>
<td>X2 capacitor, B32922 series</td>
<td>Through hole</td>
<td>Arcotronics</td>
<td>824-294</td>
</tr>
<tr>
<td>C1, C2</td>
<td>10 µF, 450 V</td>
<td>Electrolytic capacitor, NHG series</td>
<td>Through hole</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>C3</td>
<td>1 µF, 35 V</td>
<td>Ceramic capacitor</td>
<td>SMD (0805)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>C4</td>
<td>100 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td>SMD (0603)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>C5, C6</td>
<td>not mounted</td>
<td>Ceramic capacitor</td>
<td>SMD (0603)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>C7</td>
<td>1.5 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td>SMD (0603)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>C8</td>
<td>1 µF, 100 V</td>
<td>Ceramic capacitor</td>
<td>SMD (0603)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>C9</td>
<td>330 µF, 25 V</td>
<td>Electrolytic capacitor ultra-low ESR, ZL series</td>
<td>Through hole</td>
<td>Rubycon</td>
<td>365-4830</td>
</tr>
<tr>
<td>C10</td>
<td>100 nF, 50 V</td>
<td>Ceramic capacitor</td>
<td>Through hole</td>
<td>Epcos</td>
<td>211-5378</td>
</tr>
<tr>
<td>R1</td>
<td>22 ohm</td>
<td>1 W resistor</td>
<td>SMD (case 2010)</td>
<td>Panasonic</td>
<td>572-823</td>
</tr>
<tr>
<td>R3</td>
<td>1 k</td>
<td>1/4 W resistor, 1%</td>
<td>SMD (0603)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>R4a</td>
<td>12k ohm</td>
<td>1/4 W resistor, 1%</td>
<td>SMD (0805)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>R4b</td>
<td>0 ohm</td>
<td>1/4 W resistor, 1%</td>
<td>SMD (0805)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>R5a</td>
<td>47 kohm</td>
<td>1/4 W resistor, 1%</td>
<td>SMD (0805)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>R5b</td>
<td>0 ohm</td>
<td>1/4 W resistor, 1%</td>
<td>SMD (0805)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>R6</td>
<td>15 kohm</td>
<td>1/4 W resistor, 1%</td>
<td>SMD (0805)</td>
<td>Panasonic</td>
<td>365-4830</td>
</tr>
<tr>
<td>D1, D2</td>
<td>GF1M</td>
<td>1000 V / 1 A diode</td>
<td>SMD (DO-214BA)</td>
<td>Vishay</td>
<td>629-1123</td>
</tr>
<tr>
<td>D3, D4</td>
<td>STTH1L06</td>
<td>Ultra-fast 600 V diode</td>
<td>SMD (SMB pack)</td>
<td>ST</td>
<td>629-1123</td>
</tr>
<tr>
<td>D5</td>
<td>18 V zener</td>
<td>not mounted</td>
<td>Through hole</td>
<td>ST</td>
<td>629-1123</td>
</tr>
<tr>
<td>D6</td>
<td>LL4148</td>
<td>Diode</td>
<td>SMD (SOD-80)</td>
<td>Fairchild</td>
<td>629-1123</td>
</tr>
<tr>
<td>L1</td>
<td>1 mH</td>
<td>Axial inductor</td>
<td>Through hole</td>
<td>Epcos</td>
<td>191-0712</td>
</tr>
<tr>
<td>L2</td>
<td>0.82 mH</td>
<td>Power inductor</td>
<td>SMD (COIL)</td>
<td>Fairchild</td>
<td>670-8826</td>
</tr>
<tr>
<td>U1</td>
<td>VIPer26LD</td>
<td>Controlled switch</td>
<td>SMD (SO16N)</td>
<td>ST</td>
<td>191-0712</td>
</tr>
<tr>
<td>U2</td>
<td>L78L05</td>
<td>Voltage regulator</td>
<td>Through hole (TO-92)</td>
<td>ST</td>
<td>191-0712</td>
</tr>
</tbody>
</table>
4 Layout

Figure 3. Layout (top)  Figure 4. Layout (asytop)

Figure 5. Layout (bottom)  Figure 6. Layout (asybottom)
5 Testing the board

5.1 Typical waveforms

If the 5 V output is not loaded, the 16 V output can supply up to 320 mA. Since the efficiency standards are usually intended for single output converters, this setting is regarded as “full load” here and in Section 6.

The GND voltage and current waveforms under the full load condition are shown for the two nominal input voltages in Figure 7 and Figure 8, and for the minimum and maximum input voltages in Figure 9 and Figure 10 respectively.

![Figure 7. Waveforms at V\textsubscript{IN} = 115 V\textsubscript{AC}, full load](image1)

![Figure 8. Waveforms at V\textsubscript{IN} = 230 V\textsubscript{AC}, full load](image2)

![Figure 9. Waveforms at V\textsubscript{IN} = 90 V\textsubscript{AC}, full load](image3)

![Figure 10. Waveforms at V\textsubscript{IN} = 265 V\textsubscript{AC}, full load](image4)
5.2 Line/load regulation and output voltage ripple

The output voltage of the board was measured under different line and load conditions, with the results given in the following figures.

![Figure 11. Line regulation](image1)

![Figure 12. Load regulation](image2)

5.3 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages ($V_{IN} = 115\, V_{AC}$ and $V_{IN} = 230\, V_{AC}$).

External power supplies (those housed separately to the end devices they are powering) must comply with the Code of Conduct, version 5 “active mode efficiency” criterion, which stipulates an active mode efficiency higher than 74.8% for a power throughput of 5.2 W (CoC5 tier1, January 2014). CoC5 tier2 will increase this to 78% in January 2016.

Another applicable standard is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 77.9%.

This evaluation board is compliant with all standards @115 $V_{AC}$, and with CoC5 Tier1 @ 230 $V_{AC}$, as can be seen in Figure 13, where the average efficiencies of the board at 115 $V_{AC}$ (78.1%) and at 230 $V_{AC}$ (76.3%) are plotted with dotted lines, together with the above mentioned limits. The efficiency at 25%, 50%, 75% and 100% load for both input voltages is also shown.(a)

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(a) the measurements performed in Section 5.2 and Section 5.4 are only indications as the above mentioned standards only apply to single output converters
CoC5 also imposes a requirement on the active mode efficiency when the output load is 10% of the nominal output power. The table below comparing the requirement for an external power supply with a power throughput of 5.2 W and the performance of the evaluation demonstrates that the STEVAL-ISA116V1 is compliant with both Tier 1 and Tier 2 requirements.

<table>
<thead>
<tr>
<th>CoC5 minimum efficiency requirement in active mode at 10% of full load (for $P_{OUT} = 5.2$ W)</th>
<th>Evaluation board performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 1</td>
<td>Tier 2</td>
</tr>
<tr>
<td>64.8%</td>
<td>68%</td>
</tr>
</tbody>
</table>

### 5.4 Light load performances

In version 5 of the Code of Conduct, the power consumption of the power supply when it is not loaded is also considered. The compliance criteria are given in the table below:

<table>
<thead>
<tr>
<th>Table 4. Energy consumption criteria for no load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nameplate output power ($P_{no}$)</td>
</tr>
<tr>
<td>Tier 1</td>
</tr>
<tr>
<td>0.3W &lt; $P_{no}$ ≤ 49 W</td>
</tr>
<tr>
<td>50W &lt; $P_{no}$ &lt; 250 W</td>
</tr>
</tbody>
</table>

The input power of the converter was measured under a no-load condition for different input voltages, with the results given in Table 5.

The board is compliant with the Tier1 requirement and also with the Tier 2 (at 115 VAC) requirement. In the same table, the consumption of the demonstration board in other light load cases ($P_{OUT} = 25$ mW, $P_{OUT} = 50$ mW and $P_{OUT} = 250$ mW) is also shown.
Depending on the equipment supplied, it is possible to measure the performance of a converter against several criteria. In particular, one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The evaluation board satisfies this requirement, as shown in Table 5.

Another criterion is the measure of output power (or efficiency) when the input power is equal to one watt. This and some other conditions ($P_{IN} = 250$ mW and $P_{IN} = 500$ mW) are shown in the table below.

### Table 5. Light load consumption

<table>
<thead>
<tr>
<th>$V_{IN}$ [V AC]</th>
<th>$P_{IN}$ [mW]</th>
<th>@ $P_{OUT} = 0$</th>
<th>@ $P_{OUT} = 25$ mW</th>
<th>@ $P_{OUT} = 50$ mW</th>
<th>@ $P_{OUT} = 250$ mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>115</td>
<td>73</td>
<td>104</td>
<td>136</td>
<td>384</td>
<td></td>
</tr>
<tr>
<td>230</td>
<td>87</td>
<td>115</td>
<td>155</td>
<td>420</td>
<td></td>
</tr>
</tbody>
</table>

### Table 6. Light load consumption

<table>
<thead>
<tr>
<th>$V_{IN}$ [V AC]</th>
<th>$P_{IN}$ [mW]</th>
<th>@ $P_{IN} = 250$ mW</th>
<th>@ $P_{IN} = 500$ mW</th>
<th>@ $P_{IN} = 1$ W</th>
</tr>
</thead>
<tbody>
<tr>
<td>115</td>
<td>58.7</td>
<td>71.4</td>
<td>77.3</td>
<td></td>
</tr>
<tr>
<td>230</td>
<td>51.2</td>
<td>65.2</td>
<td>73.4</td>
<td></td>
</tr>
</tbody>
</table>
6 Functional check

6.1 Startup

The startup phase at maximum load at both nominal input voltages (115 V\textsubscript{AC} and 230 V\textsubscript{AC}) is shown in Figure 14, Figure 15, Figure 16 and Figure 17.

- Figure 14. Startup at V\textsubscript{IN} =115 V\textsubscript{AC}, full load
- Figure 15. Startup at V\textsubscript{IN} =115 V\textsubscript{AC}, full load, zoom
- Figure 16. Startup at V\textsubscript{IN} =230 V\textsubscript{AC}, full load
- Figure 17. Startup at V\textsubscript{IN} =230 V\textsubscript{AC}, full load, zoom

6.2 Overload protection

In case of overload or short-circuit (see Figure 18), the drain current reaches the I\textsubscript{DLIM} value (or the value set by the user connecting an appropriate resistor between LIM and GND pins, as explained in the VIPER26 datasheet). A counter increments for every cycle that this condition is met and, if it continues for the time t\textsubscript{OVL} (set internally; typically 50 ms), the overload protection is tripped, the power section is turned off and the converter is disabled for a t\textsubscript{RESTART} time (typically 1 s). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection continues indefinitely in the same way (Figure 19).
This ensures a low repetition rate of converter restart attempts, so that it works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.

Once the short is removed, the IC resumes normal operation. If the short is removed before the protection is triggered, i.e., during $t_{SS}$ or $t_{OVL}$, the counter decrements for each cycle down to zero.

If the short-circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before switching is resumed (Figure 21).

### Figure 18. Output short-circuit applied: OLP tripping

![Diagram showing output short-circuit applied.](image)

### Figure 19. Output short circuit maintained: OLP steady-state

![Diagram showing output short circuit maintained.](image)

### Figure 20. Output short circuit maintained: OLP steady-state (zoom)

![Diagram showing output short circuit maintained (zoom).](image)

### Figure 21. Output short-circuit removal and converter restart

![Diagram showing output short circuit removal and converter restart.](image)

### 6.3 Feedback loop failure protection

This protection is available whenever the IC is externally biased. When the loop is broken (R4 shorted or R5 open), the output voltage $V_{OUT1}$ increases and the VIPER26 runs at its maximum current limitation. The $V_{DD}$ pin voltage also increases as it is linked to $V_{OUT1}$ through diode D6.
If the $V_{DD}$ voltage reaches the $V_{DDclamp}$ threshold (23.5 $V_{min}$) in less than 50 ms, the IC is shut down by open loop failure protection (see Figure 22 and Figure 24) or by OLP, as described in the previous section. Loop interruption was simulated by shorting the low side resistor of the output voltage divider, $R_4 = R_{4a1}+R_{4b}$, but the same behavior can be induced by opening the high side resistor, $R_5 = R_{5a}+R_{5b}$.

The protection functions in auto restart mode, where $t_{RESTART} = 1$ s (Figure 23). Once the fault is removed, normal operation is restored after the last $t_{RESTART}$ interval (Figure 25).

![Figure 22. Feedback loop failure protection: tripping](image1)

![Figure 23. Feedback loop failure protection: steady state](image2)

![Figure 24. Feedback loop failure protection: steady state (zoom)](image3)

![Figure 25. Feedback loop failure protection: converter restart](image4)
7 Feedback loop calculation guidelines

7.1 Transfer function

In the figure below, \( G_1(f) \) represents the PWM modulator + power stage set, while \( C(f) \) is the controller or network which ensures the stability of the system.

**Figure 26. Control loop block diagram**

The mathematical expression of the power system \( G_1(f) \) in DCM is the following:

**Equation 2**

\[
G_1(f) = \frac{\Delta V_{out}}{\Delta \delta} = G_{10} \cdot \frac{1 + \frac{j \cdot f}{f_z}}{1 + \frac{j \cdot f}{f_p}}
\]

where \( f_z \) is the zero due to the ESR of the output capacitor:

**Equation 3**

\[
f_z = \frac{1}{2 \cdot \pi \cdot C_{out} \cdot ESR}
\]

and \( f_p \) is the pole due to the output load:

**Equation 4**

\[
f_p = \frac{1 + \beta \cdot R_{out}}{2 \cdot \pi \cdot C_{out} \cdot (ESR + R_{out} + ESR \cdot \beta \cdot R_{out})}
\]

with:

**Equation 5**

\[
\alpha = \frac{V_{IN} + V_{\gamma}}{(V_{out} + V_{\gamma})} \cdot \frac{I_{pk}}{2}
\]
Equation 6
\[ \beta = \frac{V_{IN} + V_G}{(V_{OUT} + V_G)^2} \cdot \frac{I_{pk}}{2} \cdot \delta \]

Equation 7
\[ G10 = \frac{\alpha \cdot Rout}{1 + \beta \cdot Rout} = \frac{(V_{OUT} + V_G) \cdot (V_{In} + V_G) \cdot \frac{I_{pk}}{2} \cdot \frac{\alpha \cdot Rout}{(V_{OUT} + V_G)^2 + (V_{In} + V_G) \cdot \frac{I_{pk}}{2} \cdot \delta \cdot Rout}}{1 + \beta \cdot Rout} \]

In the above formulas, Cout and ESR are the capacitance and the equivalent series resistance of the output capacitor respectively, \( V_G \) is the forward drop of the free-wheeling diode, Rout = Vout/Iout is the output load, Ipk is the drain peak current at full load and \( \delta = \frac{T_{on}}{f_{sw}} \) is the duty cycle.

If the only compensation network between COMP and GND is an RC series as shown in Figure 2 (C5 and C6 are not mounted), the mathematical expression for the compensator \( C(f) \) is:

Equation 8
\[ C(f) = \frac{C_0}{H_{COMP}} \cdot \left( \frac{1 + j \cdot f}{f_{zc}} \right) \cdot j \cdot 2 \cdot \pi \cdot f \]

where \( C_0 \) is given by:

Equation 9
\[ C_0 = \frac{L \cdot f_{sw}}{V_{In} - V_{OUT}} \left( \frac{-Gm}{C7} \right) \cdot \frac{R4}{R4 + R5} \]

and

Equation 10
\[ f_{zc} = \frac{1}{2 \cdot \pi \cdot R3 \cdot C7} \]

must be chosen in order to ensure the stability of the overall system.

The values \( H_{COMP} = \delta V_{COMP}/\delta I_{COMP} \) and \( Gm \) (error amplifier transconductance) are specified in the VIPER26 datasheet.

7.2 Compensation procedure for a DCM BUCK

The first step is to choose the pole and zero of the compensator and the crossing frequency.

In this case, \( C(f) \) only has a zero \( f_{zc} \) and a pole at the origin, thus a possible setting is:

\[ f_{zc} = n \cdot f_{p} \]
\[ f_{cross} = f_{cross\_sel} \leq f_{sw}/10 \]

\( n \) is chosen arbitrarily, a tentative value could be \( n = 25 \). After setting \( f_{cross} \), \( G1(f_{cross\_sel}) \) can be calculated from Equation 2 and, since \( |C(f_{cross\_sel}) \cdot G1(f_{cross\_sel})| = 1 \), \( C_0 \) can be calculated as follows:
Equation 11
\[ C_0 = \frac{\frac{j \cdot \pi \cdot f_{\text{cross}_\text{sel}}}{f_{zc}}}{1 + \frac{j \cdot \pi}{f_{zc} \cdot f_{\text{cross}_\text{sel}}}} \frac{H_{\text{COMP}}}{G_1(f_{\text{cross}_\text{sel}})} \]

At this point, the bode diagram of \( G_1(f) \cdot C(f) \) can be plotted to check the phase margin for stability.

If the margin is not high enough, the procedure should be repeated with new choices for \( f_{zc} \) and \( f_{\text{cross}_\text{sel}} \).

Once stability is achieved, the next step is to find the values of the schematic components, which can be calculated as follows.

From (Equation 9):

Equation 12
\[ C_7 = \frac{L \cdot f_{\text{sw}}}{V_{\text{in}} - V_{\text{out}}} \left( -\frac{G_m}{C_0} \right) \cdot \frac{R_4}{R_4 + R_5} \]

and from (10):

Equation 13
\[ R_3 = \frac{1}{2 \cdot \pi \cdot f_{zc} \cdot C_7} \]

The quantities found in equations (Equation 12) and (Equation 13) are suggested values. Commercial values \( C_7_{\text{act}} \) and \( R_7_{\text{act}} \) are chosen, resulting in \( f_{zc}_{\text{act}} \).

Equation 14
\[ f_{zc}_{\text{act}} = \frac{1}{2 \cdot \pi \cdot R_3_{\text{act}} \cdot C_7_{\text{act}}} \]

The value of \( C_0 \) is also recalculated from (Equation 9):

Equation 15
\[ C_0_{\text{act}} = \frac{L \cdot f_{\text{sw}}}{V_{\text{in}} - V_{\text{out}}} \left( -\frac{G_m}{C_7_{\text{act}}} \right) \cdot \frac{R_4_{\text{act}}}{R_4_{\text{act}} + R_5_{\text{act}}} \]

and the compensator becomes:

Equation 16
\[ C_{\text{act}}(f) = \frac{C_{0_{\text{act}}} \cdot (1 + \frac{f}{f_{zc_{\text{act}}}})}{H_{\text{COMP}}} \frac{1}{j \cdot 2 \cdot \pi \cdot f} \]

At this point, the bode diagram of \( G_1(f) \cdot C_{\text{act}}(f) \) should be plotted and the phase margin checked for stability.
8 Thermal measurements

A thermal analysis of the evaluation board under full load condition at $T_{\text{AMB}} = 25 \, ^\circ\text{C}$ was performed using an IR camera. The results are shown in the following figures, where:

A = VIPer26LD; B = D4; C = L78L05; D = environment.

**Figure 27.** Thermal measurement @ $V_{\text{IN}} = 115 \, V_{\text{AC}}$, full load ($I_{\text{OUT1}} = 270 \, \text{mA}$, $I_{\text{OUT2}} = 45 \, \text{mA}$)

**Figure 28.** Thermal measurement @ $V_{\text{IN}} = 230 \, V_{\text{AC}}$, full load ($I_{\text{OUT1}} = 270 \, \text{mA}$, $I_{\text{OUT2}} = 45 \, \text{mA}$)
9 EMI measurements

A pre-compliance test against the EN55022 (Class B) European normative was performed using an EMC analyzer and an LISN. The average EMC measurements at 115 $V_{AC}$/full load and 230 $V_{AC}$/full load were taken and the results are shown in the following figures.

Figure 29. Average measurement at full load, 115 $V_{AC}$

Figure 30. Average measurement at full load, 230 $V_{AC}$
Appendix A  

Test equipment and measurement of efficiency and light load performance

The converter input power was measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied to give the instantaneous measured power. The sampling frequency is in the 20 kHz range (or higher depending on the instrument used). The display returns the average over short intervals (typ. 1 sec) of the instantaneous power measurements.

*Figure 31* shows the internal block diagram of the wattmeter and its connections with the UUT (unit under test) and the AC source.

A.1 Measuring input power

With reference to *Figure 31*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch in *Figure 31* is in position 1 (see also the simplified scheme in *Figure 32*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input, which of course affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example, when measuring the input power of the UUT under a light load condition).
For a high UUT input current (i.e., for measurements under heavy load conditions), the voltage drop can be significant compared to the UUT real input voltage. In this case, the switch in Figure 31 can be changed to position 2 (see simplified scheme in Figure 33), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

On the other hand, the position of Figure 33 may introduce a significant error during light load measurements, where the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument with infinite input resistance) is not negligible. This is why it is preferable to use the settings in Figure 32 for light load measurements and Figure 33 for heavy load measurements.

If it is not clear which measurement scheme has the least effect on the result, try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements.
After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT is considered stable and the measurements are recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured over time for both the AC input and DC output.

Some wattmeter models allow integration of the measured input power over a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is then calculated dividing by the same integration time.
10 References

- Code of Conduct on energy efficiency of external power supplies, version 5.
- VIPER26 datasheet
11 Revision history

Table 7. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
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<tbody>
<tr>
<td>04-Dec-2014</td>
<td>1</td>
<td>Initial release.</td>
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