AN4461

Application note

100 W LED street lighting application using STLUX385A

Introduction

The STEVAL-ILL066V2 evaluation board is a complete and configurable solution that manages a single high brightness LED string using the STLUX385A digital controller and two stages of power conversion.

The application consists of a PFC regulator followed by a zero voltage switching (ZVS) LC resonant stage. The LED current is adjusted using a primary side regulation (PSR) control technique. The LED brightness can be dimmed by controlling the LED current down to a very low level. Communication interfaces like DALI and UART are present, as well as an insulated 0 - 10 control input.

Visit www.st.com for further information regarding the STLUX385A digital controller (STLUX385A datasheet).

Danger: *High voltages are present on the STEVAL-ILL066V2 evaluation board.*

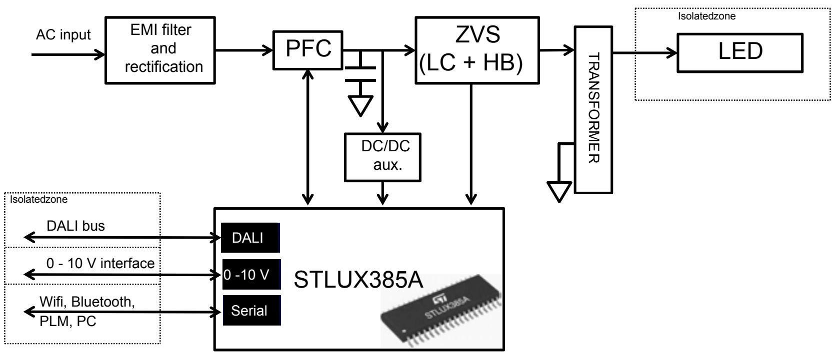
Important:
This board shall be used by qualified and knowledgeable people due to internal high voltage. The user shall take great care when handling the evaluation board, even when no power is supplied.

1 Board features

- Wide input voltage range: 90 V to 265 V AC (50 or 60 Hz) compliant with IEC61000-3-2
- Single isolated output suitable for LED connection.
- Output voltage range (hardware configurable):
  - Standard version: 30 V to 90 V
  - High voltage version (with hardware modification): 60 V to 180 V
- Output current and dimmable range:
  - Standard version: from 10 mA to 1000 mA
  - High voltage range (with hardware modification): from 5 mA to 500 mA
- Output resolution: 11-bit equivalent.
- Maximum output power: 100 W
- Primary side control for higher efficiency (92% at full load)
- Fault detection and protection: short-circuit or open circuit.
- IDLE mode power consumption: < 250 mW
- Remote control:
  - DALI command [IEC62386 (101-102 ed.2.0 and 207-LED ed.1.0)]
  - Isolated serial line
  - Isolated 0 - 10 V (alternative to DALI)
- Two status LEDs:
  - Green = ready-run-CPU load
  - Red = fault
- Primary to secondary and interfaces isolation: 3750 V
- CLO function to compensate varying light level over LED life cycle
- Temperature protection and limitation
- Increase I_{OUT} precision reading V_{OUT}

1.1 Block diagram

Figure 1. PSR-ZVS block diagram



2 Getting started with the STEVAL-ILL066V2 evaluation board

This section provides information regarding connection, power up and control of the evaluation board.

Caution:
Very high voltages are present on the board: suitable IPD ("Individual Protection Devices") and specific skills are required to operate on the board.

Figure 2. **STEVAL-ILL066V2 evaluation board**

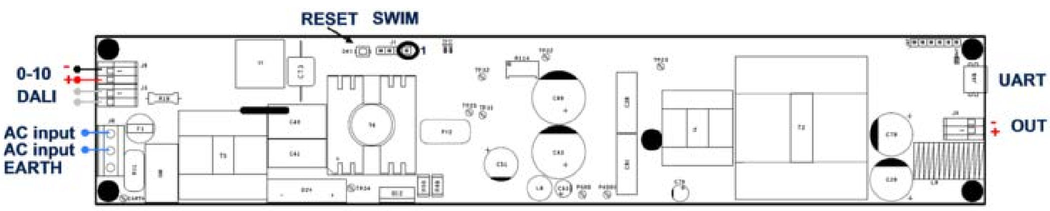


Figure 3. **STEVAL-ILL066V2 board connections**

The user must provide a LED string with the following characteristics:

- total forward voltage and maximum current rate: 90 V at 1 A (default), 180 V at 0.5 A (with hardware modification)

The LED string is connected to the board output connector J4; the output power is isolated from the main AC input.

The minimum LED forward voltage for the board is 30 V when 1 A is selected or (60 V at 0.5 A with hardware modification).

Caution:
Please observe the correct string polarity, as indicated on the PCB. Incorrect LED connection may damage the LED due to the high inverse voltage.

The board supports a wide AC input range (J8 connector) and operates in the 90 VAC – 265 VAC range. This makes the board suitable to be connected directly to mains power. The board also supports a 170 V to 350 V DC input voltage range on the same J8 connector. The AC or DC connection to J8 is shown in Figure 3. STEVAL-ILL066V2 board connections.

The STEVAL-ILL066V2 evaluation board offers three different communication channels: DALI, 0 - 10 V and a serial interface. The DALI and 0 - 10 V interface share the same STLUX385A pins and are therefore mutually exclusive. The active line is selected via GPGUI commands.

The DALI interface can be controlled by any DALI master compliant with the IEC62386-101 and 102 ed. 2.0 standard. When the DALI protocol is used, the DALI bus must be connected before starting the application.

Absence of the DALI line (OPEN DALI) for more than 500 ms from power-up causes the DALI interface to enter "SYSTEM FAILURE LEVEL". When using the DALI interface, the DALI master should be operational before connecting the board. The DALI connector is J3; it has no polarity and it is also isolated from the power stage. The DALI command set implemented on this board is described in Section 9.2.1 List of supported DALI commands.

An isolated 0 - 10 V interface can be activated instead of the DALI bus when the DALI protocol is not required or is unavailable. The 0 - 10 V interface connector is J9 and is polarized.

A voltage below 1 V powers off the output LED strings. A 1 V to 10 V voltage drives the output current from 10% to 100% of the maximum rated value, in a linear fashion. A voltage between 0 V and 1 V switches off the LED.

The serial line is accessible via the J48 micro-USB connector and is isolated from the power stage. A micro USB connector can be used to connect a PC with the serial interface. The board is controlled using a dedicated GPGUI program, available on www.st.com. The USB interface is isolated from the power stage.

The serial input allows the user to interact with the board in parallel with the DALI bus. When the 0 - 10 V interface is selected, the output current is only regulated through the 0 – 10 V interface and no changes are allowed via the serial line. The serial line command set is described in Section 9.3 GPGUI interface on STEVAL-ILL066V2 evaluation board.

The STEVAL-ILL066V2 can be set in a very low-power IDLE state when the LEDs are switched off via DALI commands. In this state all operations are halted until, a new DALI command is received.

The STEVAL-ILL066V2 also automatically enter low power mode if it detects open circuits and short-circuits on the output. When the load returns to normal, the board FW proceeds to restore correct output power. In case of load disconnect, the board detects load re-connection after a maximum of 6 seconds.

The STEVAL-ILL066V2 evaluation board acquires temperature through simulation using the R114 trimmer. When the temperature is rises above a set level, the application is switched off and waits until the temperature normalizes.

2.1 First power-on procedure

Ensure that the STEVAL-ILL066V2 evaluation board is tested using:

- a DALI master or a 0 - 10 V master line or the serial line.
- a micro-USB serial cable shipped with the board
- an AC or DC power supply
- a computer running Windows and the GPGUI program available on www.st.com
- a V_F = 90 V LED string as the load

Before first power-on, connect the serial line thus:

1. Connect the micro-USB serial cable to the USB port of the computer. Windows recognizes the cable as a new COM port and launches the driver installation.
2. Install the appropriate USB TTL serial cable drivers. The drivers are the “virtual COM port (VCP)” and they are provided by FTDI (http://www.ftdichip.com). If you need any help to install the drivers, please refer to your IT administrator. Once the drivers are installed, the Windows device manager panel shows a new USB serial port (COMx) device and the COM number associated.
3. Run the GPGUI program, select the correct COM port associated with the virtual COM port. Click the "connect" button only when board is powered. After downloading the current parameter, the GPGUI waits for a USER command (see Section 9.3 GPGUI interface on STEVAL-ILL066V2 evaluation board).

Whenever the board is powered on, you should verify the following:

- The board input connector is J8 and the input voltage ranges from 96 VAC to 265 VAC (50 Hz or 60 Hz) or 170 VDC to 350 VDC. The user can supply the input from:
  – AC or DC power supply: configure the power supply output to one of the allowed input values; make sure that the power supply output is OFF and connect the power supply to J8.
  – Mains: make sure that the mains output is within the allowed range. Connect the power cable to J8 but do NOT plug the cable into a main socket.
- Connect the LED string to the connector J4: connect the LED string anode to the “+” pole and the cathode to the “-” pole. The LED string forward voltage and current must be within the current board configuration: 90 V (refer to Section 4.1.4 Transformer output voltage).
- Optionally connect the DALI or 0 - 10 V interface.

  - Connect the DALI line to the J3 connector (polarization is not important). Check with the serial line if this interface is enabled (default when the board is skipped).
  - Connect the 0 - 10 V line to the J9 connector (the interfaces is polarized). Check with the serial line if this interface is enabled (disabled when the board is skipped).
- Connect the serial cable to J48 using the USB TTL serial cable.
- Turn on the input power and verify that:
  - The RUN-FAULT LED goes on for few seconds before switching off. If the FAULT LED stays on, this indicates that an error has occurred or a protection is active. Switch off the board and check the problem.
  - The output current begins flowing in the LED string within 1 second. At power on, the output current is low (~1% of total output power). The current level may vary depending on the external interfaces available:
    - If the DALI bus is enabled and active, the output current is set to the “DALI power on level”.
    - If the 0 - 10 V is enabled the output current defined by the voltage applied on J9.
- Verify the correct operation by changing the output current using alternatively DALI commands, 0 - 10 V or the GPGUI command. Note that the GPGUI command only works when the DALI and 0 - 10 are not active.

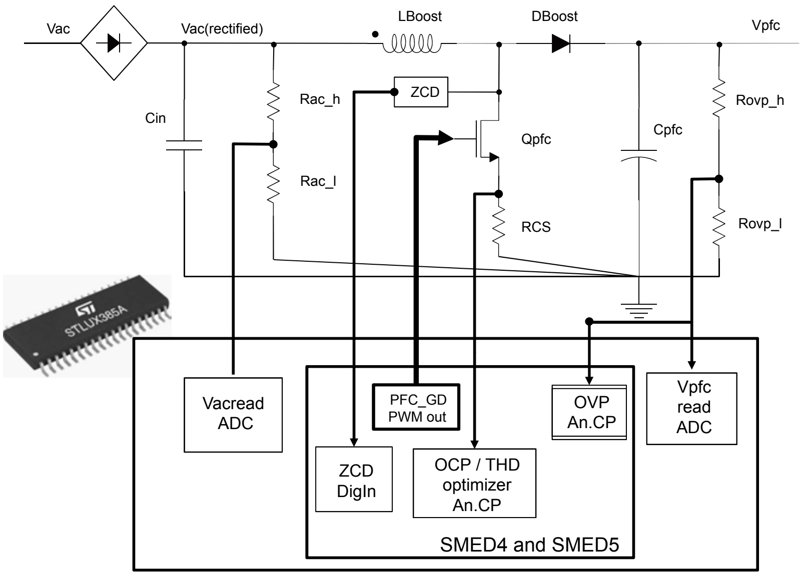
If an error is detected (e.g., no load condition), the PFC and ZVS stages are immediately switched off and the red LED is lit.

3 PFC stage

The STEVAL-ILL066V2 evaluation board is based on two power conversion stages where a first PFC stage generates the DC voltage to apply to the LC resonant stage. The LC resonant stage controls the output current.

3.1 Constant Ton working principles

Figure 4. **PFC concept**



The PFC stage is based on a boost converter operating in a transitional mode (also referred as critical conduction or a boundary mode) using the constant on-time method with enhanced THD optimizer.

In boost topology, the variation of the inductor current during the conduction time of the main switch (T_{ON}) depends on the input voltage, as per the following equation:

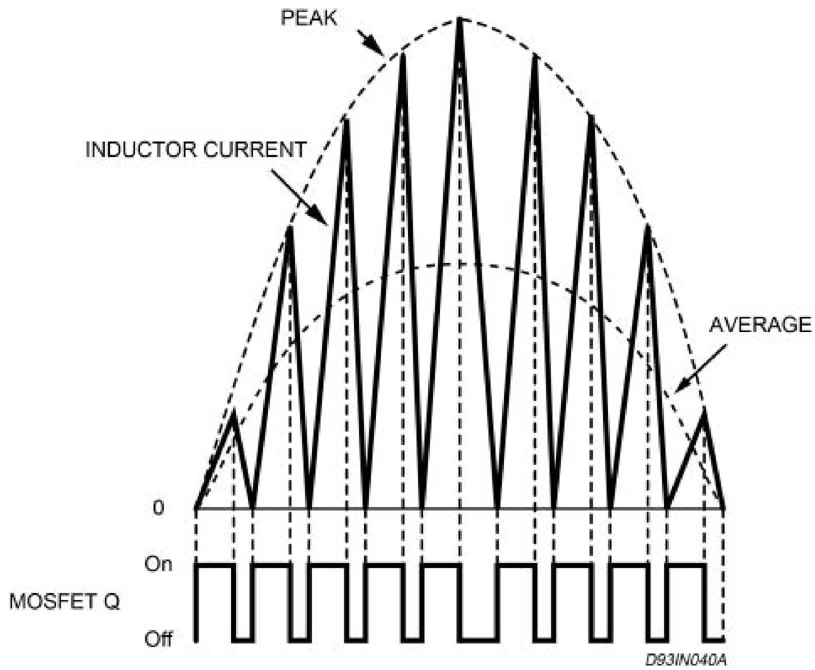
Equation 1

$$\Delta I_{Lboost} = T_{ON} \frac{\sqrt{2} \cdot V_{ac}(sin2\pi \cdot f_{mains} \cdot t)}{L_{Boost}} \quad (1)$$

The conduction time (T_{ON}) is the time the MOSFET remains on. T_{ON} is normally updated every zero voltage transition on the AC cycle and is based on the PFC output voltage using a Proportional-Integral algorithm. The PFC bandwidth is ~5 Hz. The boost MOSFET is turned on when the boost inductor current falls to zero.

The result of this algorithm is that the inductor current is shaped like a series of adjacent triangles where the peaks envelop a half-wave sinusoid in phase with the AC input line voltage. For geometrical reasons, the average current absorbed from the input line is also sinusoidal.

Figure 5. PFC input current



During light load conditions, a valley skipping mechanism is adopted, allowing a lower output voltage ripple and lower operating frequencies.

3.2 PFC stage protection

The STLUX385A device implements several protections that prevent component degradation due to electrical overstress or overheating. The protections implemented in the PFC stage are:

1. **Overvoltage protection (OVP)**: using a resistor partition sensing the PFC output voltage, it stops switching activity when the output capacitor voltage reaches a certain threshold. The PFC is turned on as soon as the capacitor voltage returns below the threshold. This function is provided throgh STLUX pin 28 (CPP[0]) and is active when input level is higher than 1.23 V (typ.).
2. **Overcurrent protection (OCP)**: is activated when the inductor peak current reaches very high values during T_{ON} (e.g., due to input overvoltage or output overloading). The current is read by the RCS shunt resistor and compared with a threshold. The threshold is dynamic and adjusted depending on the input voltage. This function is provided through STLUX input pin 25 (CPP[2]). The OCP current level can be set in the parameter file.
3. **Brownout**: when the input voltage is lower than a threshold the PFC stage is disabled. When the input voltage returns to acceptable levels, the PFC is turned on again. This prevents overstressing the PFC power components due to operations at very low input voltages. This function is provided through STLUX pin 35 (ADCIN[3]) and can be set in the parameter file.
4. **Controlled soft start**: limits the charging current of the Cpfc capacitor. This provides the following advantages: a limited inrush current associated with the PFC activation and improved control of the output voltage to avoid overshooting and corresponding audible noise. The soft start time is approximately 100 ms.

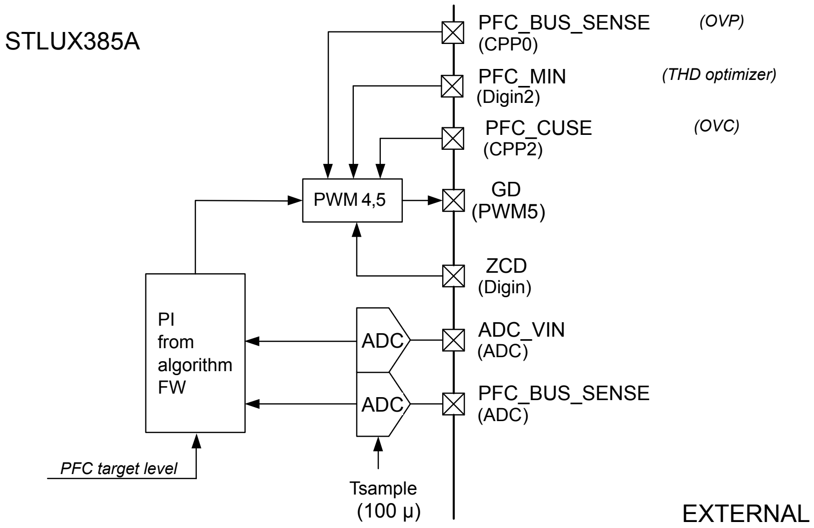
3.3 Implementation on STLUX385A

The PFC stage is implemented with the SMED technology used in the STLUX385A. In particular, two SMEDs in coupled mode drive a single PWM output connected to the PFC MOSFET.

Table 1. STLUX385A input and output pins used by the PFC stage

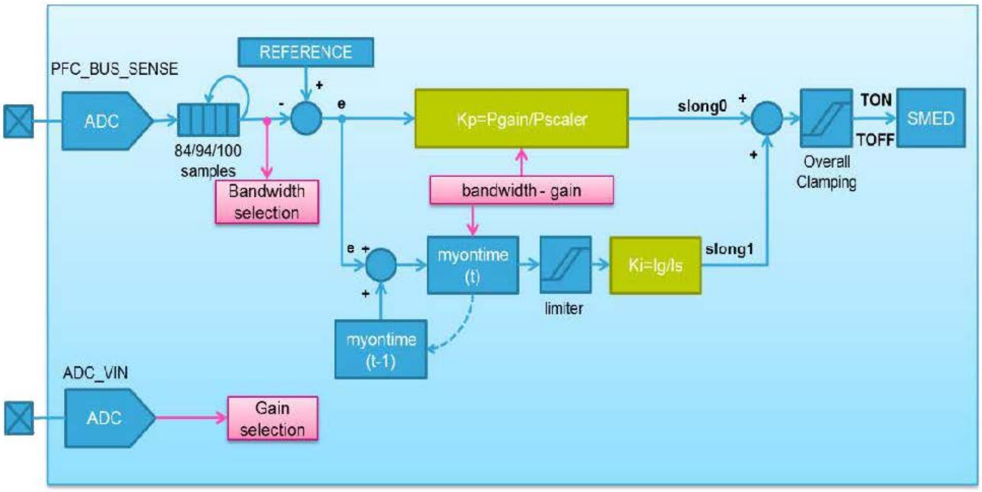
Pin	Description
PWM5	Used as a PWM for the PFC MOSFET. It is internally driven by the SMED4 and SMED5
CPP0	Input for OVP protection
CPP2	Senses the current during T_{ON} time
ADC0	PFC output voltage measurement
ADC3	Input voltage, phase and frequency measurement
DGIN3	“Zero Current Detection” input
DGIN2	Input THD optimizer

Figure 6. PFC physical implementation



The STLUX385A embeds the algorithms used to control the PFC behavior by regulating the PWM switching frequency. The correct switching parameters (T_{ON}, T_{OFF}) are calculated from the PFC output voltage.

Figure 7. **PFC PI FW implementation**



In the STLUX FW, a standard PI algorithm is implemented with parameters “P” and “I”, which can be set with GPGUI. The calculated T_{ON} - T_{OFF} time is applied once every AC cycle. The bandwidth of the PFC control loop is dynamically adjusted when load transients occur (see Figure 7. PFC PI FW implementation).(Refer to the STSW-ILL066V2 firmware user manual on www.st.com.)

The CPP0 input is used to detect an overvoltage and switches off the PWM once the PFC voltage is greater than an internally configured safety threshold. The threshold is adjusted depending on the AC input voltage. Once the PFC output voltage reaches the safety threshold, the PWM is disabled within approximately 50 ns.

The CPP2 input is used to detect the overcurrent protection features on the PFC MOSFET. The CPP2 interacts immediately with the SMED to protect the PFC stage. The level is not fixed; it is a function of the input AC voltage and is defined by the internal DAC level.

The PFC stage is activated 30 ms after power-on or activation. This time is used to sense the input AC voltage and enable the PFC with the appropriate parameters for the given AC voltage.

The ZCD input signal is connected on pin DIGIN3 and interacts with the SMED to start the ON time.

The STLUX385A also implements a THD optimizer approach (ST patents US 2013194842 and US 2013194845) via the DIGIN2 pin.

3.4 PFC stage customization

3.4.1 Inductor

The operating frequency of the PFC stage varies along every half cycle of the rectified AC input voltage and at different load conditions. The inductor value can be selected in order to obtain an operating frequency greater than a minimum value, normally ranging between 35 kHz and 60 kHz.

The following equation can be used to select the minimum operating frequency, using either the minimum or maximum VAC value, whichever gives the lower value for L.

Equation 2

$$L_{boost} = \frac{V_{ac}^2 \left(V_{pfc} \cdot \sqrt{2} V_{ac}\right)}{2 \cdot f_{sw\_min} \cdot P_{in} \cdot V_{pfc}} \quad (2)$$

The saturation current can be set slightly higher than the maximum peak current occurring at the peak of the input sine wave at full output power and low input voltage.

Equation 3

$$I_{Lsat} = 2 \cdot \sqrt{2} \cdot \frac{P_{in}}{V_{ac,min}} \quad (3)$$

Once these two values are obtained, the physical design of the inductor can be completed using one of the approaches described in relevant application notes (e.g., AN966 on www.st.com).

3.4.2 Output capacitor

The output capacitor reduces frequency ripple and maximizes hold-up time. The operating frequency of the secondary LC stage is strongly dependent on its input voltage. It is therefore necessary to minimize the PFC output voltage ripple to avoid very wide frequency variation during the LC half-bridge operations.

The capacitor can be chosen according to the following equation:

Equation 4

$$C_{pfc} \geq \frac{P_{out}}{4\pi \cdot f_{mains} \cdot V_{pfc} \cdot \Delta V_{pfc}} \quad (6)$$

The input filtering capacitor (Cin) and the offline EMI filtering are required to prevent the high frequency noise (generated by PFC and LC switching activity) from being injected back to the input supply.

The STLUX385A device samples the PFC output voltage via a resistive voltage divider (R46, R52, R55, R58, C49, C66 in Section 6 Schematic diagrams). The voltage divider shall be set so that the PFC output voltage reference is divided down to 1.114 V input to the STLUX385A.

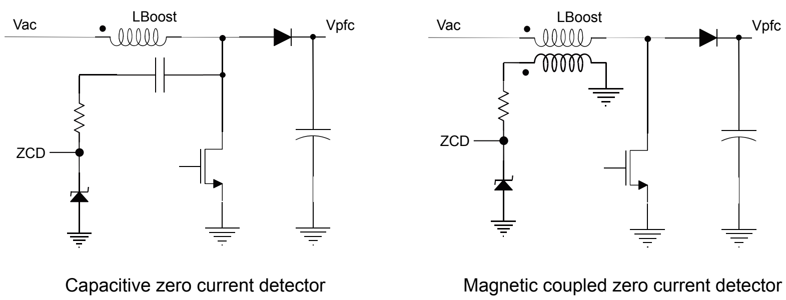
You should configure the PFC output voltage at least 25 V above the maximum voltage expected from the rectifying bridge. The STEVAL-ILL066V2 evaluation board supports a PFC maximum input voltage of 375 V so the PFC output voltage can be set to any value between 390 V and 415 V. The default value is 410 V.

3.4.3 Zero current detection circuit

The STLUX385A detects that the inductor current has fallen to zero via a “Zero Current Detection” circuit.

The STEVAL-ILL066V2 evaluation board supports two different zero current detection mechanisms: one uses a capacitor between the MOSFET drain while the other connects an auxiliary winding across L_{Boost} and detection input pin. In both cases, suitable clamping devices (e.g., Zener diodes or current limiting resistors) are required. The board is currently configured to use the capacitive zero current detection circuit.

Figure 8. PFC - ZCD sensing



3.4.4 PFC output voltage

Using the same approach as an analog chip, the STLUX requests a fixed level on the ADCIN[0] pin to regulate the PFC output voltage. The PFC reference voltage (PFC_Vref) is 1.1151 V.

Example 1

From the schematic (Section 6 Schematic diagrams) the resistor network R46, R52, R55, and R58 provides voltage feedback to STLUX385A.

Given:

$$V_{REF} = V_{OUT} \cdot \frac{R58}{(R58 + R55 + R52 + R46)} \quad (8)$$

…we can change R58 from 18K to 16K to adjust output voltage to 460 V. The OVP level also changes: the internal OVP threshold is 1.23 V so, with the change in R58, the OVP level moves to 507 V.

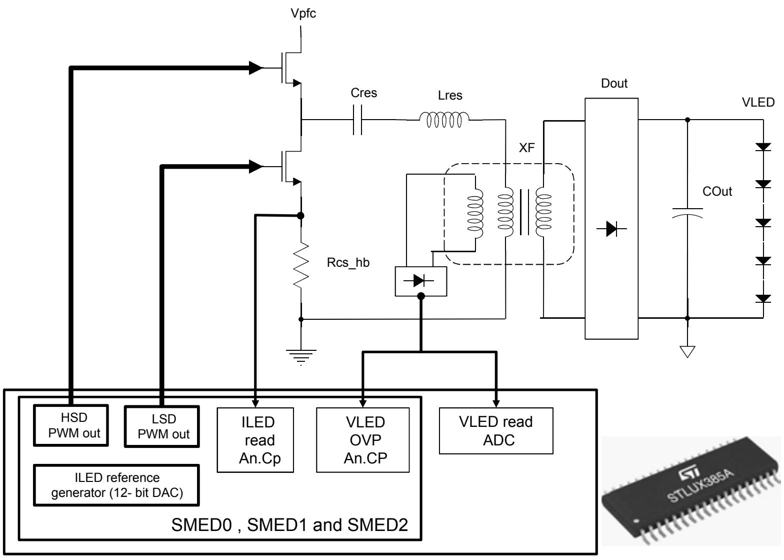
It is necessary to change the voltage ratings of the MOSFET (to 600 V) and bulk capacitor (to 500 V). On the STEVAL-ILL066V2 a spare serial bulk capacitor is available on the PCB.

Note: If you change the bulk capacitor voltage value, you need to trim the PFC PI parameter.

4 ZVS LC resonant stage description

The resonant stage is an LC topology consisting of a half-bridge operating in “Zero Voltage Switching” condition supplying the resonant cell. The half-bridge is connected to the PFC output. The LC stage (Cres, Lres) is separated from the transformer. The transformer XF is responsible for the energy transfer to the secondary side, where a rectifier circuit (Dout) and a filtering capacitor transform the AC current into a ripple free DC current required by the LEDs.

Figure 9. ZVS concept



The transformer XF is designed to maximize the winding coupling and operate similar to an ideal transformer, where the secondary side current is proportional to the primary side current and depends only on the transformer turn ratio (n = NPRI / NSEC). This proportionality is the key to controlling the secondary side current from the primary side.

Lres and Cres are selected to ensure operation above resonance in any condition, therefore guaranteeing a soft switching behavior. The primary current has a triangular shape so we can assume that the average value of the LED current is equal to half of the peak of the resonant secondary current. By regulating the peak current during the low-side conduction period and using a 50% duty cycle, primary side control of the output current is possible.

The transformer is coupled with an auxiliary winding which is used to measure the reflected voltage at the primary side and detect abnormal conditions such as short-circuit or no load.

4.1 LC stage customization

4.1.1 Resonant Cell ZVS design

The following equation must be satisfied to maintain the zero voltage switching condition:

Equation 5

$$n \cdot (V_{LED} + V_{dout}) \text{<} \frac{1}{2} \cdot V_{pfc} \qquad (6)$$

When the half-bridge switching frequency (f_S) is close to the resonance frequency (f_R), then the shape of the resonant tank current is piecewise sinusoidal. Otherwise, when $f_S >> f_R$ then the shape of the resonant tank current is piecewise linear.

For the purpose of the analysis, both the magnetizing current and the AC voltage across the tank capacitor, Cres, are negligible.

Considering that the square wave voltage applied to the resonant tank has 50% duty cycle, it is possible to state:

Equation 6

$$V \cdot (C_{res}) \approx \frac{1}{2} \cdot V_{pfc} \quad (7)$$

Furthermore, the output current is given by the superposition of the currents through the secondary rectifier (Dout) and is a series of contiguous triangles. The DC output current is equal to half of the resonant current peak value multiplied by transfer ratio (n = NPRI / NSEC).

Equation 7

$$I_{LED} \approx \frac{n}{2} \cdot I_{res,pk} \quad (8)$$

It can be demonstrated that the switching frequency of the converter is represented by:

Equation 8

$$f_{hb} = \frac{n}{16 \cdot I_{LED} \cdot L_{res}} \cdot \frac{V_{pfc}^2 - [2n \cdot (V_{LED} + V_{dout})]^2}{V_{pfc}} \quad (9)$$

The half-bridge frequency depends directly on the input voltage and inversely on the LED current, and also depends on the difference between the square of the input voltage and the reflected value of the output voltage.

It should be noted that the half-bridge frequency follows a hyperbolic pattern depending on the output power (I_{LED}, V_{LED}). This behavior is the main difference when compared to an LLC or LCC resonant converter (see AN2644 and AN2450 on www.st.com).

The LC minimum operating frequency is obtained at the maximum output current, maximum output voltage and minimum PFC output voltage. The maximum frequency is, instead, obtained at the minimum output current ($I_{LED,min}$), minimum output voltage (consider short-circuit if required) and maximum input voltage.

For further consideration, it is useful to rewrite Equation 5 as:

Equation 9

$$n = \lambda \cdot \frac{V_{pfc,min}}{2 \cdot (V_{LED} + V_{dout})} \; with \; \lambda \in (0,1) \quad (10)$$

Then the ratio between minimum and maximum frequency can be expressed as:

Equation 10

$$\frac{f_{hb,max}}{f_{hb,min}} = \frac{I_{LED,min}}{I_{LED,max}} \cdot \frac{1}{V_{pfc,min}} \cdot \frac{V_{pfc,max}^2 - V_{pfc,min}^2 \cdot \left(\frac{\lambda \cdot V_{dout}}{V_{LED} + V_{dout}}\right)^2}{V_{pfc,min} \cdot \left(1 - \lambda^2\right)} \quad (11)$$

which can be simplified as follows:

Equation 11

$$\frac{f_{hb,max}}{f_{hb,min}} = \mathrm{I}_{dim} \cdot \frac{\Gamma}{\left(1 - \lambda^2\right)} \; with \; \Gamma = \frac{V_{pfc,max}}{V_{pfc,min}} \; and \; \mathrm{I}_{dim} = \frac{I_{LED,min}}{I_{LED,max}} \quad (12)$$

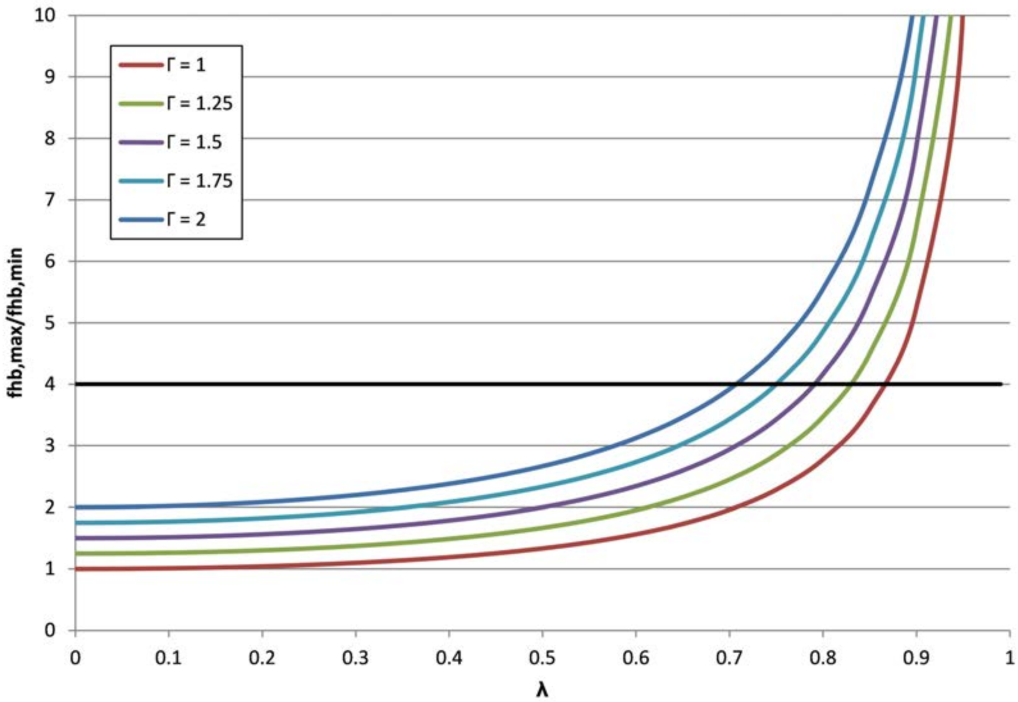
Keeping transient effects and current variations in consideration, it is good empiric design practice to have:

Equation 12

The parameter Γ is directly related to the ripple superimposed on the PFC output voltage. An indication of the required transformer ratio is obtained by combining Equation 11 and Equation 9 .

The following figure shows the frequency range at a fixed current versus λ at different values of the parameter Γ.

Figure 10. ZVS - λ vs. frequency



4.1.2 LC stage characteristic selection

The following procedure can be used to determine the main component values.

Step1: Determine the primary-to-secondary turn ratio *n* of the transformer. From Equation 11 , we can calculate λ for maximum LED current:

Equation 13

$$\lambda = \sqrt{1 - \frac{V_{pfc,max}}{V_{pfc,min}} \cdot \frac{f_{hb,max}}{f_{hb,min}}} \tag{20}$$

Note: $f_{hb,max}$ and $f_{hb,max}$ should be selected so that λ < 0.9 to account for rounding errors, mismatch and tolerances in the transformers.

We can now calculate the transformer transfer ratio n as:

Equation 14

$$n = \frac{NPRI}{NSEC} = \lambda \cdot \frac{V_{pfc,min}}{2 \cdot (V_{LED} + V_{dout})} \tag{21}$$

V_{dout} is the forward voltage of the output rectified (0.5 V for Schottky rectifiers, 0.8 V for p-n rectifiers or Shottky-based Wien bridge rectifiers).

Step 2: Use the following table to calculate the current in different points of the circuit.

Table 2. Current values

Parameter	Primary side	Secondary side
Peak current	$I_{ppk} = \frac{2}{n} \cdot I_{LED}$ (22)	$I_{spk} = 2 \cdot I_{LED}$ (23)
Total current swing	$\Delta I_p = 2 \cdot I_{ppk} = \frac{4}{n} \cdot I_{LED}$ (24)	$\Delta I_s = I_{spk} = 2 \cdot I_{LED}$ (25)

Parameter	Primary side	Secondary side
DC current	$I_{pdc} = 0$ (26) $I_{pav} = \frac{1}{n} \cdot I_{LED}$ (27) $I_{in} = \frac{I_{LED} \cdot (V_{LED} + V_{dout})}{V_{dout}}$ (28)	$I_{sdc} = I_{LED}$ (29)
Total RMS current	$I_{prms} = \frac{2}{n\sqrt{3}} \cdot I_{LED}$ (30)	$I_{srms} = \frac{2}{\sqrt{3}} \cdot I_{LED}$ (31)
AC RMS current	$I_{pac} = \frac{2}{n\sqrt{3}} \cdot I_{LED}$ (32)	$I_{sac} = \frac{1}{\sqrt{3}} \cdot I_{LED}$ (33)

Step 3: From Equation 8 and Equation 13 , calculate the inductance value of L_{res}

Equation 15

$$L_{res} = \frac{\lambda\left(1 - \lambda^2\right)}{32 \cdot I_{LED} \cdot f_{hb,min}} \cdot \frac{V_{pfc,min}^2}{(V_{LED} + V_{dout})} \quad (34)$$

Step 4: determine the capacitance value of the resonant capacitor C_{res} so that the peak amplitude of the AC ripple voltage is much lower (e.g., always 10%) than the DC offset. Indicatively:

Equation 16

$$C_{res} \geq 5 \cdot \frac{I_{LED}}{n \cdot V_{pfc,min} \cdot f_{hb,min}} \quad (35)$$

Step 5: select the output capacitors C_O so that they:

- are rated for the maximum output voltage V_{LED}
- meet the output voltage ripple specification (if any)
- have an adequate AC current ripple rating.

The output current ripple specification must be met. To do so, we first need to find the value of the overall R_{LED} for the LED string by considering the tangent to the forward characteristic in the specified operating point.

The following equation can then be used to find the suitable value for C_O and its ESR.

Equation 17

$$\frac{\Delta I_{LED}}{I_{LED}} \cdot R_{LED} \geq \sqrt{\left(\frac{I_{LED}}{n \cdot V_{pfc,min} \cdot f_{hb,min}}\right)^2 + 4 \cdot ESR^2} \quad (36)$$

The maximum allowed ripple current for C_O must be:

Equation 18

$$\Delta IC_O \geq \frac{I_{LED}}{\sqrt{3}} \quad (37)$$

4.1.3 Half-bridge operation

In order to generate a proper oscillation in the LC resonant tank, the half-bridge must generate a square wave with a 50% duty cycle. Any unbalancing of this duty cycle may cause the loss of zero voltage switching condition and thus increase the risk of component overstress.

The adoption of the same conduction time (T_{ON}) for both half-bridge MOSFETs ensures this condition. Thanks to resonance, when one MOSFET is turned off, the middle point of the half-bridge moves to the opposite side of the half-bridge in a time that depends on the overall capacitance (real or parasitic) connected to the node.

To avoid undesired switching losses, a deadtime longer than this transition time is applied between the time one side of the half-bridge switches off and the time the opposite side turns on.

In order to correctly regulate the LED current, it is important to accurately detect the instant of the peak of the resonant current. The peak is detected by the STLUX385A via a shunt resistor placed between the source of the low-side MOSFET and ground. The sampling time of the peak is therefore dependent on the propagation delay

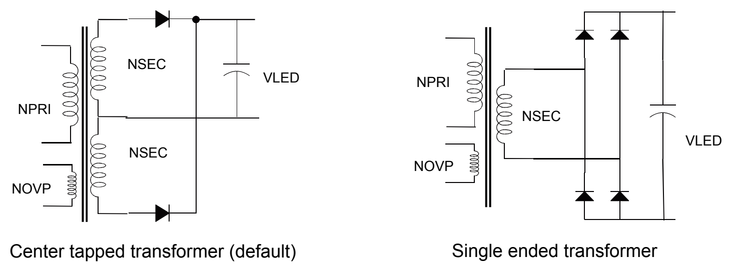
(~200 ns) generated by the driver and the MOSFET gate capacitance. An internal fixed STLUX385A delay must also considered (< 50 ns).

Given that the propagation time depends from the final board construction, you should measure the final propagation time; a GPGUI parameter is available to set up/adapt the real board propagation time. On the STEVAL-ILL066V2 evaluation board, this time is set to 312.5 ns (or 30 SMED clock cycles).

4.1.4 Transformer output voltage

The transformer XF can be realized using a center tapped secondary side winding or a single ended secondary side. The structure of this component and the relevant rectifiers are shown below.

Figure 11. ZVS output circuits



The transformer used in the STEVAL-ILL066V2 evaluation board is configured as center tapped.

In order to change the output from the default 90 V (max. 1 A) to 180 (max. 0.5 A), perform these steps (see):

1. Mount D42 and D43 with the 2 x STTH3R06S (SMC package)
2. Remove R102.

Note: The STTH3R06S components are not included in the STEVAL-ILL066V2 evaluation board.

4.2 Half-bridge stage protection

The STLUX385A offers several levels of protection:

1. **Output undervoltage protection (UVP)**: prevents the LC resonant stage from operating when its input voltage (i.e., the PFC output capacitor voltage) is very low. When an UVP condition arises, the STLUX385A device stops the switching activity on the LC stage until the PFC voltage returns above an acceptable range. This UVP voltage is sensed using the STLUX pin 38 (ADCIN[0]). The default level is a function of the AC input line and is adjustable using the parameter file.
2. **No load**: prevents the LC stage from operating when there is no LED string connected. This protection prevents the resonant output capacitors from being damaged due to overcharge. When the output capacitor voltage reaches a threshold, the STLUX385A disables the resonant activity. The “no load” protection is implemented sensing the STLUX pin 36 (ADCIN[2]) and STLUX pin 27 (CPP[1]). The default level to trigger the no load condition is 1.00 V (at the STLUX pin); but can be adjusted using the parameter file.
3. **Brownout protection**: When the AC input voltage drops under 90 V the resonant stage is disabled at the same time as the PFC. This brownout voltage is sensed using the STLUX pin 38 (ADCIN[0]). The default level is adjustable using the parameter file.
4. **Short-circuit protection**: the STEVAL-ILL066V2 evaluation board architecture senses the output voltage using the STLUX pin 36 (ADCIN[2] - S_CH0 signal). When the level on this pin is below 0.122 V, a short-circuit is detected. The detection point is programmable using the parameter file.

4.3 ZVS LC resonant stage implementation on STLUX385A

Similar to the PFC stage, the LC resonant stage is driven by the SMED technology implemented by the STLUX385A. In particular, one SMED is used to control the half-bridge high-side, while another SMED controls the low-side. The two SMEDs give the STLUX385A device full control over the half-bridge conduction and deadtimes.

An additional PWM (SMED2) is used to feed a low-pass filter and generate a high precision signal with 12-bit resolution. The signal is monitored via ADC1 and continuously adjusted to compensate for the external circuit tolerance.

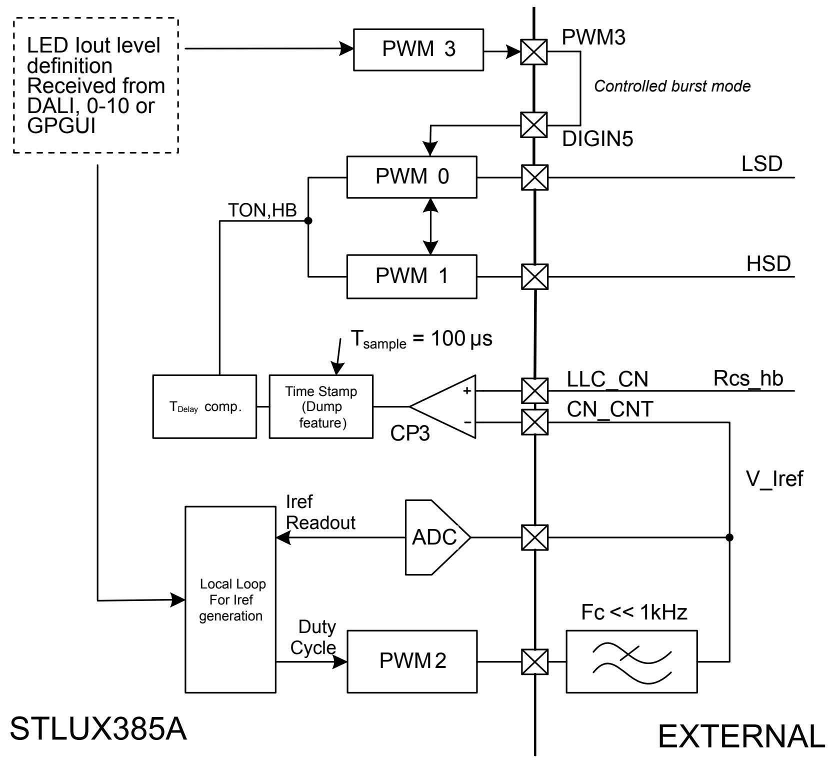
The PWM output from the SMED3 is used to control the HB switching activity during low power (output power below 45%), implementing US patent US20150003117A1.

The following table shows the STLUX385A inputs and outputs used to control the resonant stage.

Table 3. List of STLUX385A pins used by the ZVS LC stage

Pin	Description
PWM0	PWM driving the half-bridge low-side MOSFET. The output is generated by SMED0.
PWM1	PWM driving the half-bridge high-side MOSFET. The output is generated by SMED1.
PWM2	Used to generate a high precision reference with 12-bit resolution. PWM2 is the input to an external low-pass filter which generates the reference.
PWM3	Used for synchronization during low output current.
DIGIN5	Used for synchronization.
CPP3	Monitors the current on the half-bridge.
CPM3	Input of the high precision reference
CPP1	Monitor for no load conditions. The half-bridge operation is stopped when there is no load.
ADC1	Monitor for the high precision reference.
ADC2	Samples the scaled reflected voltage from the transformer to detect a no load condition or a short-circuit.

Figure 12. **Half-bridge logical implementation**



The control stage algorithm of the half-bridge resonator ensures that the half-bridge is always driven at the correct frequency so that the amount of current sensed (CPP3) matches the target current (I_{ref}) selected by the user via the DALI, UART or the 0-10 interface.

The high precision signal generated by the PWM2 (V_Iref) is used as a comparison with the actual pick current (Rcs_hb). The V_Iref is a function of DALI, 0-10 interface or GPGUI input. The maximum level of V_Iref is equal to 1.25 V, obtained when the GPGUI sets a raw value of 4093.

The relation between the GPGUI raw value and V_Iref is (RawVal/4)*(1.25/1023).

The minimum level of V_Iref is defined in the FW by the "HB_OL_LIM" definition and corresponds to 351 mV (or 1150 row value). Below this level, the PWM3 and USUS20150003117A1 patent is used to regulated the output current.

The control loop bandwidth is 10 KHz. The minimum allowed frequency is 40 KHz and maximum frequency is 400 KHz.

The STLUX controls the increase or decrease rate of the output current to meet the DALI standard requirements. Currently, the MINIMUM FAST FADE TIME is set to 26 ms from PHM to 100% or vice-versa.

5 STLUX - pinout

The following table describes the STLUX pins used by the STEVAL-ILL066V2 evaluation board.

Table 4. **STLUX385A pinout**

Pin	Dir.	Function	Note
1	OUT	PWM [0]	Low-side MOSFET driving signal for ZVS resonant stage (SMED0)
2	OUT/IN	DIGIN [0] /CCO	Used for internal synchronization or for the 0 - 10 V interface clock
3	IN	DIGIN [1]	Reserved
4	OUT	PWM [1]	High-side MOSFET driving signal for ZVS resonant stage (SMED1)
5	OUT	PWM [2]	PWM to generate high resolution reference signal (DAC) (SMED2)
6	IN	DIGIN [2]	THD optimizer input for the PFC stage
7	IN	DIGIN [3]	Zero current sensing for PFC stage
8	OUT	PWM [5]	PFC MOSFET driving signal (SMED5 and SMED4)
9	I/O	SWIM	SWIM connection
10	I/O	RESETn	Reset signal
11	PS	VDD	Power supply input
12	PS	VSS	Power supply reference voltage
13	PS	VOUT	Power supply reference voltage (core)
14	OUT	DALI TX	DALI transmit signal
15	IN	DALI RX	DALI receive signal
16	OUT	GPIO1 [4]	Reserved
17	IN	DIGIN [4]	Reserved
18	IN	DIGIN [5]	Connected to PWM3 output
19	OUT	PWM [3]	Used for synchronization
20	OUT	GPIO0 [2]	Red LED - fault indication
21	OUT	GPIO0 [3]	Green LED - running, CPU load, indication
22	OUT	UART TX	UART TX signal
23	IN	UART RX	UART RX signal
24	A-IN	CPP3	Half-bridge current sensing (SMED0)
25	A-IN	CPP2	PFC current sensing (SMED5)
26	A-IN	CMP3	Half-bridge current reference (generated by PWM2)
27	A-IN	CPP1	Half-bridge OVP detection (SMED1)
28	A-IN	CPP0	PFC OVP protection (SMED4)
29	PS	VDDA	Analog power supply input
30	PS	VSSA	Analog reference voltage
31	A-IN	ADCIN [7]	Temperature voltage monitor
32	A-IN	ADCIN [6]	3.3 V power voltage monitor
33	A-IN	ADCIN [5]	14 V power voltage monitor
34	A-IN	ADCIN [4]	0 - 10 voltage monitor
35	A-IN	ADCIN [3]	AC input voltage monitor

Pin	Dir.	Function	Note
36	A-IN	ADCIN [2]	Half-bridge auxiliary winding voltage sensing
37	A-IN	ADCIN [1]	Current reference compensation for PWM2
38	A-IN	ADCIN [0]	PFC output voltage monitor

6 Schematic diagrams

Figure 13. Schematic - STLUX385A - top

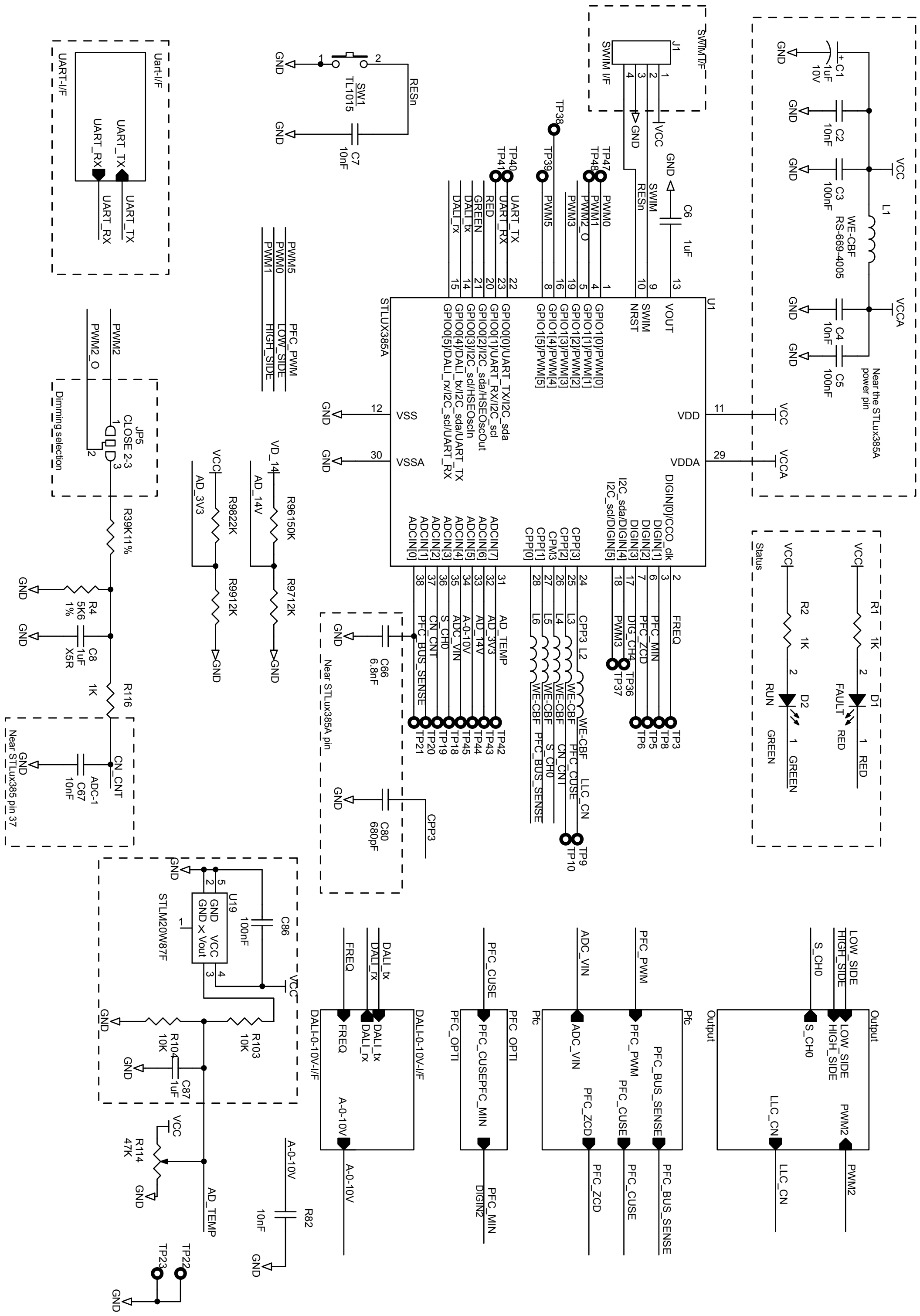


Figure 14. Schematic - PFC and DC/DC zone

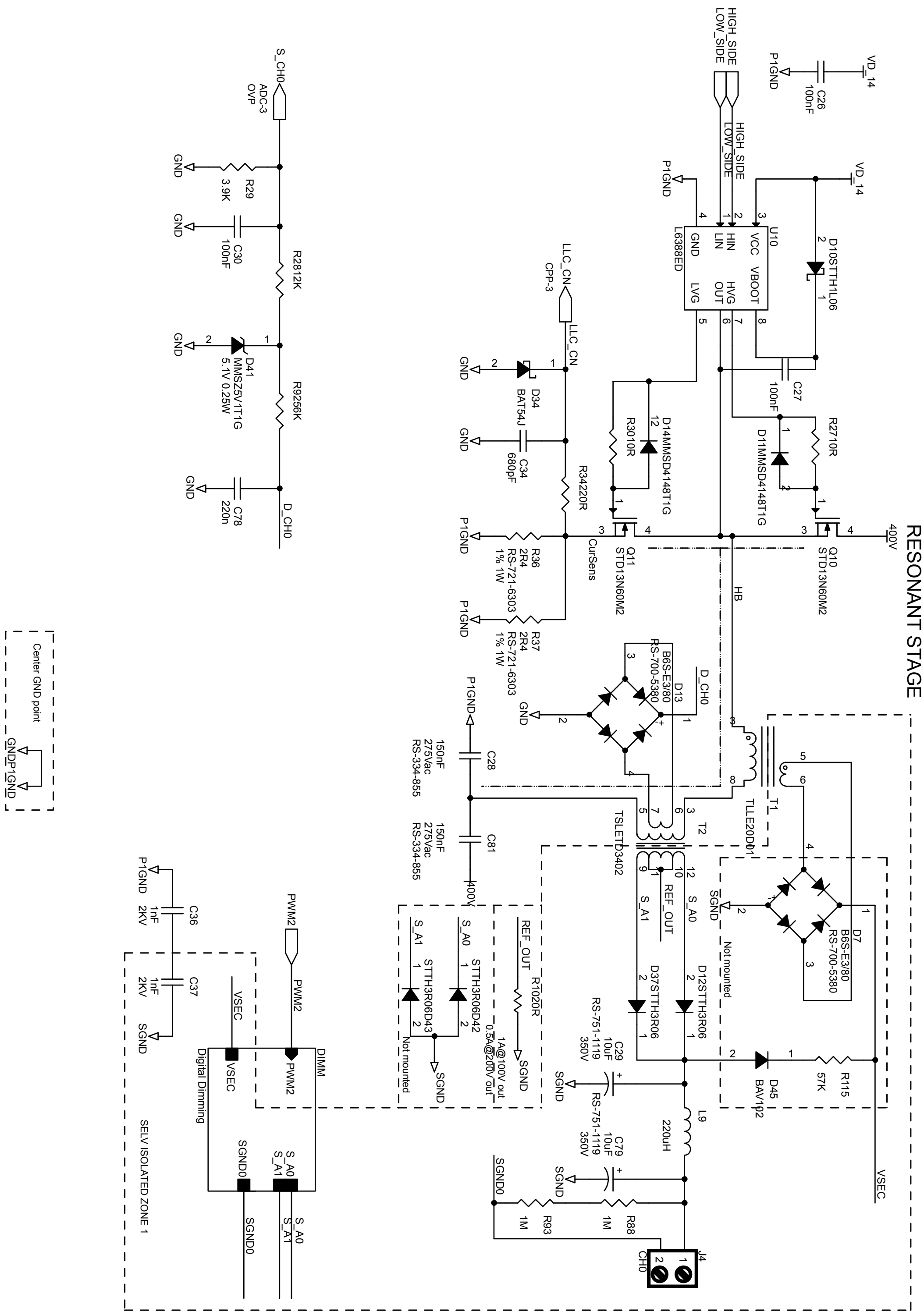


Figure 15. Schematic - PSR-ZVS stage

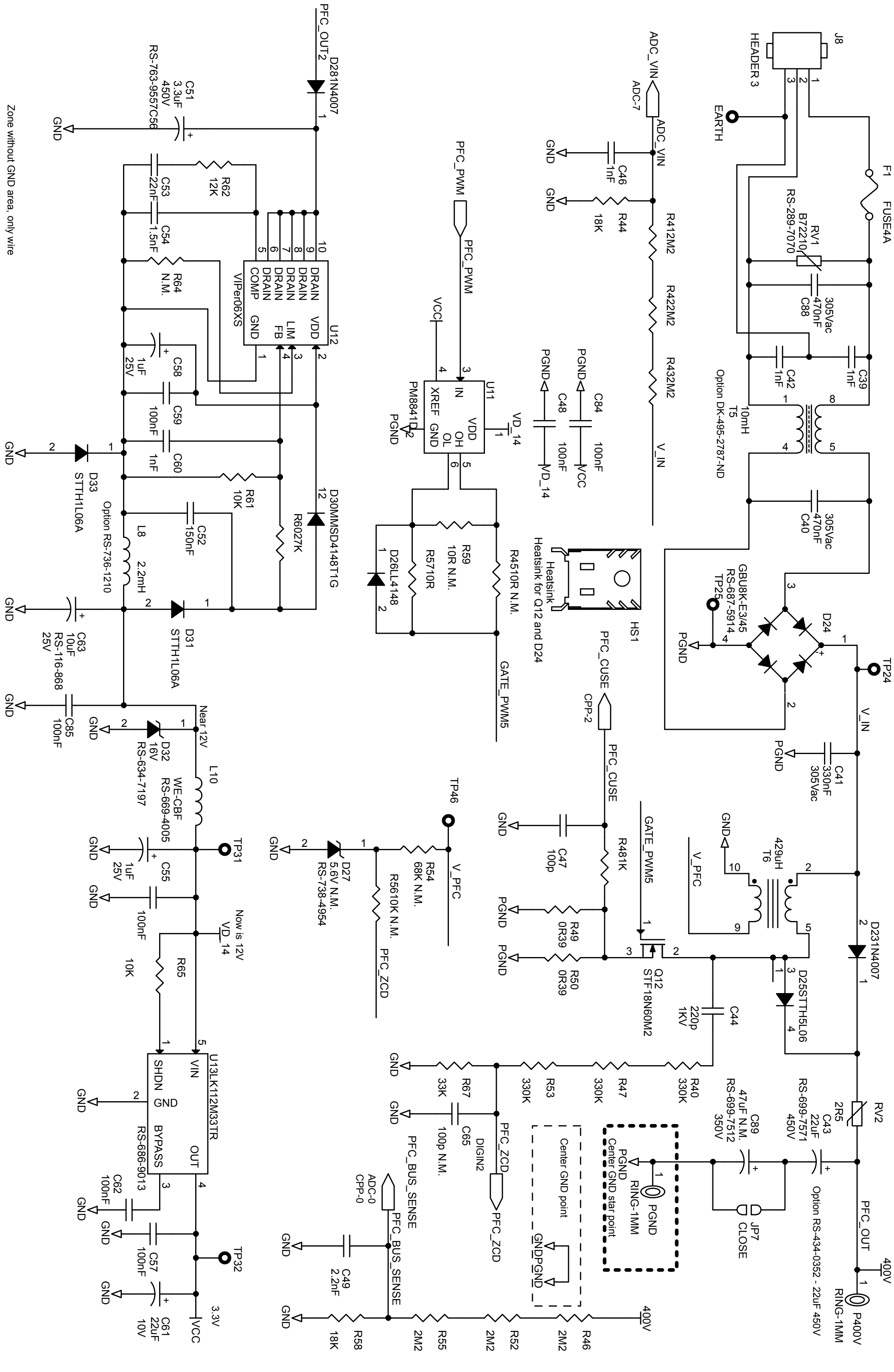


Figure 16. Schematic - digital dimming stage

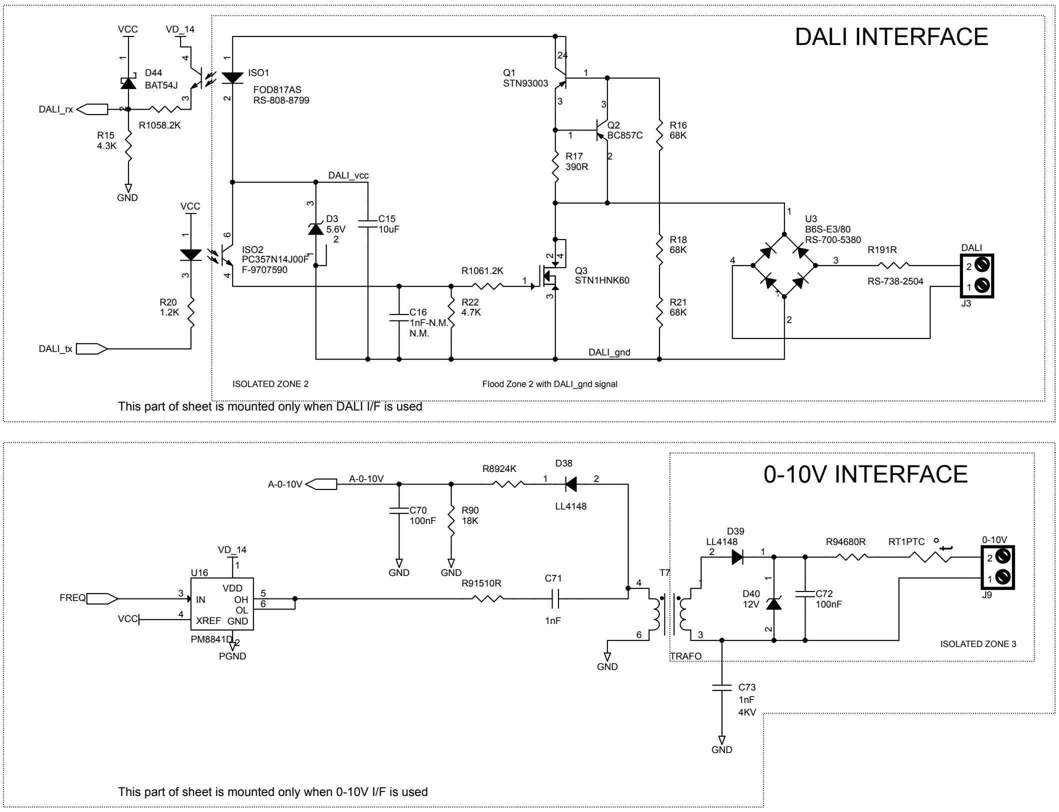


Figure 17. Schematic - THD optimizer

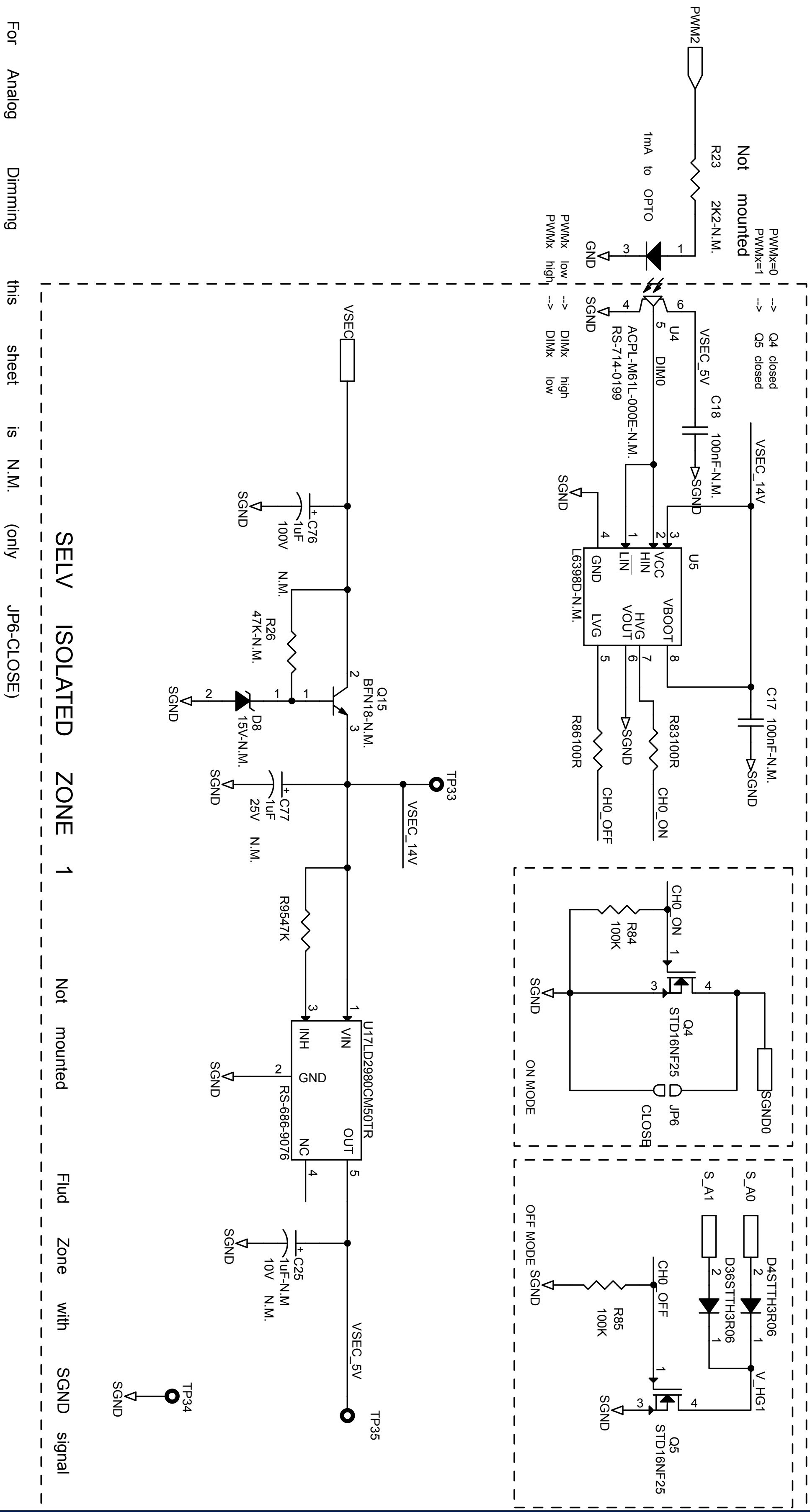
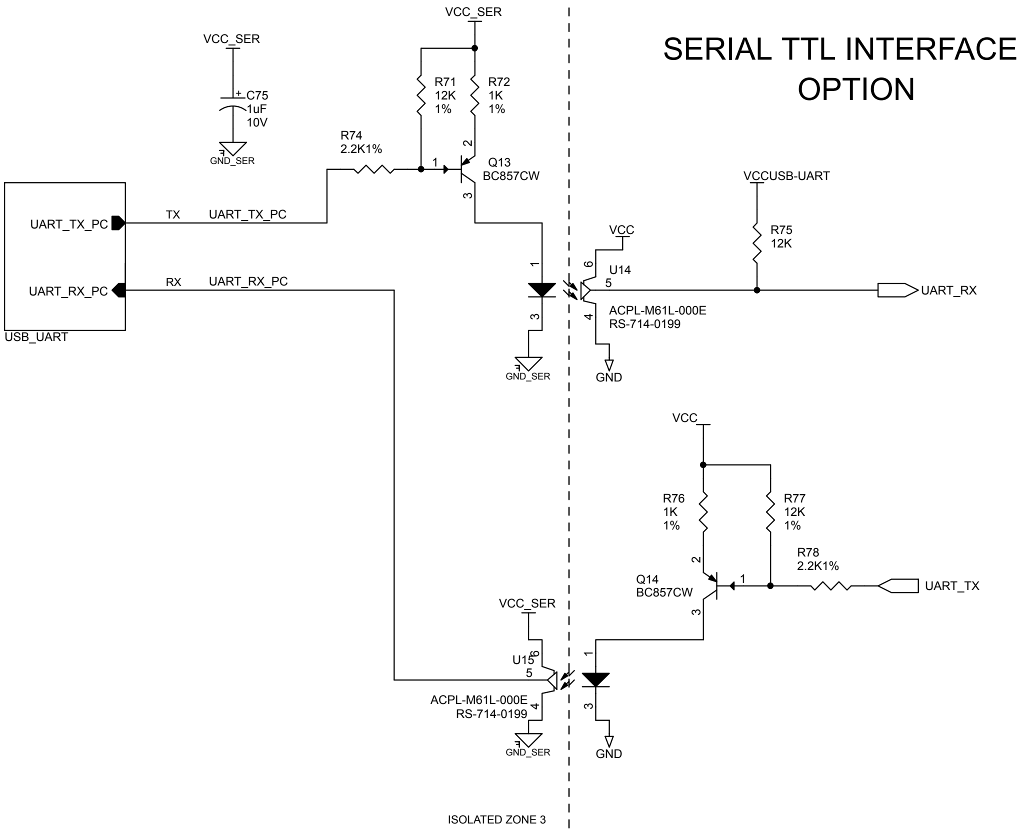


Figure 18. Schematic - DALI and 0 - 10 interfaces



This sheet is mounted only when UART I/F is used (only R75 is always mounted)

Figure 19. Schematic - serial interfaces

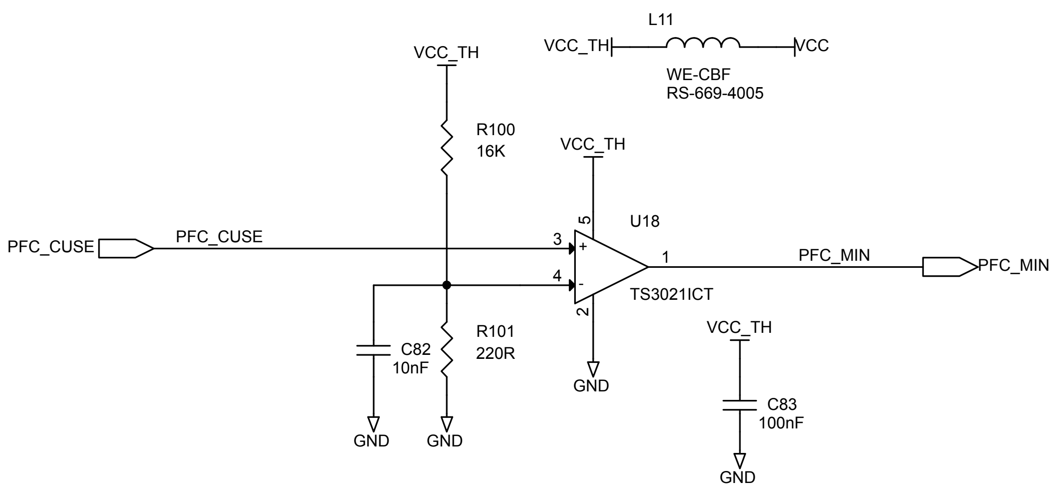
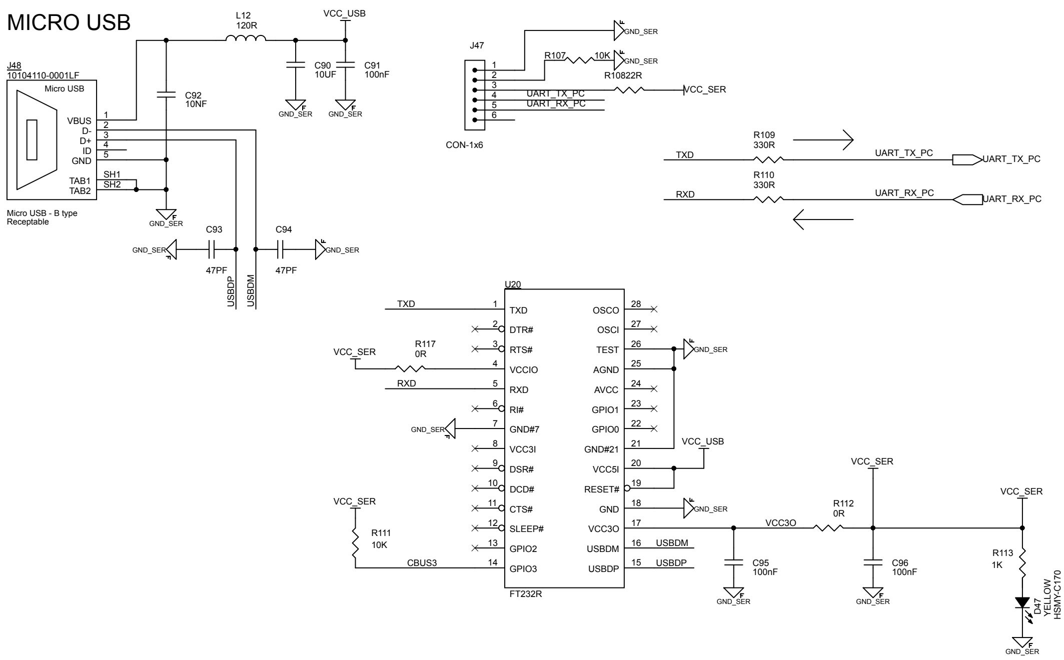


Figure 20. Schematic - USB interfaces



If use J48: mount R117, R111, R112, R109, R110 (default)

If use J47: remove R117, R111, R112, R109, R110

7 Bill of materials

Table 5. **Bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	3	C1, C6, C75	1 µF, 0603	Capacitors	AVX	0603ZG105ZAT2A
2	6	C2, C4, C7, C67, R82, C82	10 nF, 0603	Capacitors	AVX	06033C103KAT2A
3	15	C3, C5, C26, C30, C48, C56, C57, C59, C62, C70, C72, C83, C84, C85, C86	100 nF, 0603	Capacitors	AVX	06033G104ZAT2A
4	2	C8, C87	1 µF, 0603	Capacitor	TDK	C1608X5R1H105K080AB
5	1	C15	10 µF, 0805	Capacitor	Murata	GRM21BR61E106KA73L
6	1	C16	1 nF, 0603 - N.M.	Capacitor		
7	1	C17	100 nF, 0603 - N.M.	Capacitor		
8	1	C18	100 nF, 0805 - N.M.	Capacitor		
9	1	C25	1 µF, 0603 -N.M	Capacitor		
10	1	C27	100 nF, 0805	Capacitor	AVX	06033G104ZAT2A
11	2	C28, C81	150 nF, P15L6	Capacitors	EPCOS	B32922C3154K
					Wurth Elektronik	890334025022CS
12	2	C29, C79	10 µF, R13H20-P5	Capacitors	Rubycon	350BXC10MEFC10X20
13	2	C34, C80	680 pF, 0603	Capacitors	KEMET	C0603C681J5GACTU
14	2	C36, C37	1 nF, C1210	Capacitors	AVX	1210GC102KAT1A
15	2	C39, C42	1 nF, 1206	Capacitors	KEMET	C1206C102KDRACTU
16	2	C40, C88	470 nF, 175X100X165-P15	Capacitors	Vishay	BFC233920474
					Wurth Elektronik	890334025039CS
17	1	C41	330 nF, 175X85X150-P15	Capacitor	Vishay	2222 339 20334
					Wurth Elektronik	890334025034CS
18	1	C43	22 µF, R16H21-P75	Capacitor	Panasonic	EEUEE2W220S
19	1	C44	220 pF, 1206	Capacitor	AVX	1206AA221KAT1A
20	2	C46, C60	1 nF, 0603	Capacitors	AVX	06035C102KAT2A
21	1	C47	100 pF, 0603	Capacitor	KEMET	C0603C101J5GACTU
22	1	C49	2.2 nF, 0603	Capacitor	Vishay	VJ0603Y222KNAAO
23	1	C51	3.3 µF, R10HXX-P5	Capacitor	Rubycon	450PK3R3MEFC8X11.5
24	1	C52	150 nF, 0603	Capacitor	Murata	GRM188R71E154KA01D
25	1	C53	22 nF, 0603	Capacitor	AVX	06035C223KAT2A
26	1	C54	1.5 nF, 0603	Capacitor	KEMET	C0603C152K1RACTU
27	2	C55, C58	1 µF, 0805	Capacitors	Murata	GCM21BR71E105KA56L

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
28	1	C61	22 µF, 1206	Capacitor	KEMET	C1206C226M8PACTU
29	1	C63	10 µF, r5h11-p25	Capacitor	Panasonic	ECEA1EKS100
30	1	C65	100 pF, 0603 - N.M.	Capacitor		
31	1	C66	6.8 nF, 0603	Capacitor	Kemet	C0603C682K5RACTU
32	1	C71	1 nF, 0805	Capacitor	KEMIT	C0805C102J5GACTU
33	1	C73	1 nF, 850X800-175	Capacitor	MURATA	DEBB33F102KN3A
34	1	C76	1 µF, r5h11-p25	Capacitor		
35	1	C77	1 µF, 0805	Capacitor		
36	1	C78	220 nF, 0603	Capacitor	TDK	C1608X7R1H224K080AB
38	1	C89	47 µF, R16H21-P75 - N.M.	Capacitor	Panasonic	EEUEE2V470
39	1	C90	10 µF, 0805	Capacitor	Murata	GRM219R61E106KA12D
40	3	C91, C95, C96	100 nF, 0603	Capacitors	AVX	06033G104ZAT2A
41	1	C92	10 nF, 0603	Capacitor	AVX	06033C103KAT2A
42	2	C93, C94	47 pF, 0603	Capacitors	Kemet	C0603C470J5GACTU
43	1	D1	FAULT, 0603	LED	OSRAM Opto Semiconductors	LS Q976
44	1	D2	RUN, 0603	LED	OSRAM Opto Semiconductors	LT Q39G-Q1S2-25-1
45	1	D3	5.6 V, SOT23	Diode	DiodesZetex	BZX84C5V6-7-F
46	2	D4, D36	STTH3R06	TURBO 2 ultrafast high voltage rectifier	ST	STTH3R06
47	1	D7	B6S-E3/80	PONTE-SMD-MBXS	Vishay	B6S-E3/80
48	1	D8	15 V-N.M.	POWERDI323		
49	1	D10	STTH1L06	TURBO 2 ultrafast high voltage rectifier	ST	STTH1L06U
50	1	D11	MMSD4148T1G	SOD123	ONSemiconductors	MMSD4148T1G
51	2	D12, D37	STTH3R06	TURBO 2 ultrafast high voltage rectifier	ST	STTH3R06S
52	2	U3, D13	B6S-E3/80	PONTE-SMD-MBXS	Vishay	B6S-E3/80
53	2	D14, D30	MMSD4148T1G	SOD123	ONSemiconductors	MMSD4148T1G
54	1	D23	1N4007	DIODO-SMA	DiodesZetex	S1J-13-F
55	1	D24	GBU8K-E3/45	KBU8XXG	Taiwan Semiconductor	KBU807G T0
56	1	D25	STTH5L06	TURBO 2 ultrafast high voltage rectifier	ST	STTH5L06B-TR
57	1	D26	LL4148	sod80	Vishay	LL4148-GS18

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
58	1	D27	5.6 V, SOD123 - N.M.	Diode	DiodesZetex	BZT52C5V6-7-F
59	1	D28	1N4007, SMA	Diode	DiodesZetex	S1J-13-F
60	2	D31, D33	STTH1L06A	TURBO 2 ultrafast high voltage rectifier	ST	STTH1L06A
61	1	D32	16 V, SMA	Diode	Vishay	SML4745-E3
62	1	D34	BAT54J, SOD323	Small signal Schottky diode	ST	BAT54J
63	2	D38, D39	LL4148, SOD123	Diodes	ONSemiconductors	MMSD4148T1G
64	1	D40	12 V, SOD123	Diode	DiodesZetex	DDZ9699-7
65	1	D41	MMSZ5V1T1G, SOD123	Diode	ONSemiconductors	MMSZ5V1T1G
66	2	D42, D43	STTH3R06	TURBO 2 ultrafast high voltage rectifier	ST	STTH3R06S
67	1	D44	BAT54J, SOD323	Diode	ST	BAT54J
68	1	D45	BAV102, SOD80	Diode	Nexperia	BAV102-GS08
69	1	D47	YELLOW, 0805	LED	Lumex	SML-LXT0805YW-TR
70	7	TP22, TP23, TP24, TP25, TP31, TP32, EARTH	TP	Test points	Keystone Electronics	5013
71	1	F1	pth-r85h80-p5	Fuse	Wickmann	3701400000
72	1	HS1	LS205-RS2342328	Heatsink	Any	Heatsink for Q12 and D24
73	1	ISO1	FOD817AS	OPTO-SOP254P-1050X460-4	Fairchild Semiconductor	FOD817AS
74	1	ISO2	PC357N14J00F	OPTO-SOP254P-700X210-6-NO25	SHARP	PC357N14J00F
75	1	JP5	JUMPER	JP3SO	Any	Any
76	1	JP6	JUMPER	JP2SO	Any	Any
77	1	JP7	JUMPER 0 R RES	RESC-1206	Any	Any
78	1	J1	SWIM I/F	STRIP254P-M-4	Any	Any
79	1	J3	DALI	MOR-2POLI-WAGO-250-402	WAGO	250-402
80	1	J4	CH0	MOR-2POLI-WAGO-250-402	WAGO	250-402
81	1	J8	HEADER 3	MOR-3POLI-508	TE Connectivity	282837-3

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
82	1	J9	0-10V	MOR-2POLI-WAGO-250-402	WAGO	250-402
83	1	J47	CON-1x6	STRIP254P-M-6	Any	Any
84	1	J48	10104110-0001LF	MICRO_USB-B-10104110	Amphenol FCI	10104110-0001LF
85	3	L1, L10, L11	WE-CBF	Ferrite beads	Wurth Elektronik	74279262
86	5	L2, L3, L4, L5, L6	WE-CBF	Ferrite beads	Wurth Elektronik	74279269
87	1	L8	2.2 mH, R75H92-P3	Inductor	Itacoil	SLD0608222
88	1	L9	220 µH	Inductor	Wurth Elektronik	7447060
89	1	L12	120 R	Inductor	Wurth Elektronik	74279262
90	2	P400V, PGND	1 mm	Test point	Keystone Electronics	5001
91	1	Q1	STN93003, SOT223	High voltage fast switching PNP power transistor	ST	STN93003
92	1	Q2	BC857C	PNP transistor	Nexperia	BC857C
93	1	Q3	STN1HNK60, SOT223	N-channel 600 V, 7.3 Ohm typ., 1 A SuperMESH Power MOSFET	ST	STN1HNK60
94	2	Q4, Q5	STD16NF25, DPAK	N-channel 250 V, 0.195 Ohm, 14 A STripFET II Power MOSFET	ST	STD16NF25
95	2	Q10, Q11	STD13N60M2, DPAK	N-channel 600 V, 0.35 Ohm typ., 11 A MDmesh M2 Power MOSFET	ST	STD13N60M2
96	1	Q12	STF18N60M2	N-channel 600 V, 0.255 Ohm typ., 13 A MDmesh M2 Power MOSFET	ST	STF18N60M2
97	2	Q13, Q14	BC857CW	Bipolar transistor	Infineon	BC 857CW
98	1	Q15	BFN18-N.M.	SOT89	Any	Any
99	1	RT1	PTC	Mountable PTC resettable fuse	Bourns	MF-NSMF012-2
100	1	RV1	B72210, SIOV-S10K300	Varistor	EPCOS	B72210S0301K101
101	1	RV2	2R5	Thermistor	EPCOS	B57237S259M

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
102	6	R1, R2, R48, R72, R76, R116	1 K, 0603	Resistors	Vishay	CRCW06031K00FKEA
103	1	R3	9K1, 0603	Resistor	Panasonic	ERJPA3F9101V
104	1	R4	5K6, 0603	Resistor	Vishay	CRCW06035K60FKEA
105	1	R15	4.3 K, 0603	Resistor	Vishay	CRCW06034K30FKEA
106	3	R16, R18, R21	68 K, 0603	Resistors	Any	Any
107	1	R17	390 R, 0603	Resistor	Any	Any
108	1	R19	1 R, 900X320-P15-1W2	Resistor	Ohmite	OL10G5E
109	2	R20, R106	1.2 K, 0603	Resistors	Any	Any
110	1	R22	4.7 K, 0603	Resistor	Any	Any
111	1	R23	2K2, 0603-N.M.	Resistor		
112	1	R26	47 K, 0805 - N.M.	Resistor		
113	2	R27, R30	10 R, 0805	Resistors	Bourns	CR0805-FX-10R0GLF
114	1	R28	12 K, 0603	Resistor	Any	Any
115	1	R29	3.9 K, 0603	Resistor	Any	Any
116	1	R34	220 R, 0603	Resistor	Any	Any
117	2	R36, R37	2R4	Resistors	Panasonic	ERJ1TRQF2R4U
118	3	R40, R47, R53	330 K, 1206	Resistors	TE Connectivity	CRGH1206J330K
119	6	R41, R42, R43, R46, R52, R55	2M2, 1206	Resistors	Vishay	CRCW12062M20FKEA
120	2	R44, R58	18 K, 1206	Resistors	Vishay	CRCW120618K0FKEA
121	2	R45, R59	10 R , 0805 - N.M.	Resistors	Bourns	CR0805-FX-10R0GLF
122	2	R49, R50	0R39, 2512	Resistors	Panasonic	ERJ1TRQFR39U
123	1	R54	68 K, 0603 - N.M.	Resistor		
124	1	R56	10 K, 0603 - N.M.	Resistor		
125	1	R57	10 R, 0805	Resistor	Bourns	CR0805-FX-10R0GLF
126	1	R60	27 K, 0603	Resistor	Any	Any
127	1	R61	10 K, 0603	Resistor	Bourns	CR0603-FX-1002HLF
128	5	R62, R75, R77, R97, R99	12 K, 0603	Resistors	Vishay	CRCW060312K0FKEA
129	1	R64	N.M.	Resistor		
130	1	R65	10 K, 0805	Resistor	Any	Any
131	1	R67	33 K, 1206	Resistor	Vishay	CRCW120633K0FKEA
132	1	R71	12 K, 0603	Resistor	Kemet	C0805C102J5GACTU
133	2	R74, R78	2.2 K, 0603	Resistor	Vishay	CRCW06032K20FKEA
134	2	R83, R86	100 R, 0805	Resistors	Any	Any
135	2	R84, R85	100 K, 0603	Resistors	Any	Any
136	2	R88, R93	1 M, 1206	Resistors	TE Connectivity	CRG1206F1M0

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
137	1	R89	24 K, 0603	Resistor	Any	Any
138	1	R90	18 K, 0603	Resistor	Any	Any
139	1	R91	510 R, 0603	Resistor	Any	Any
140	1	R92	56 K, 0603	Resistor	Any	Any
141	1	R94	680 R, 0805	Resistor	Any	Any
142	1	R95	47 K, 0805	Resistor	Any	Any
143	1	R96	150 K, 0603	Resistor	Vishay	CRCW0603150KFKEA
144	1	R98	22 K, 0603	Resistor	Vishay	CRCW060322K0FKEA
145	1	R100	16 K, 0603	Resistor	Vishay	CRCW060316K0FKEA
146	1	R101	220 R, 0603	Resistor	Vishay	CRCW0603220RFKEA
147	1	R102	0 R, 1206	Resistor	Any	Any
148	2	R103, R104	10 K, 0603	Resistor	Any	Any
149	1	R105	8.2 K, 0603	Resistor	Any	Any
150	1	R107	10 K, 0603	Resistor	Any	Any
151	1	R108	22 R, 0603	Resistor	Any	Any
152	2	R109, R110	330 R, 0603	Resistors	Any	Any
153	1	R111	10 K, 0603	Resistor	Any	Any
154	2	R112, R117	0 R, 0603	Resistors	Any	Any
155	1	R113	1 K, 0603	Resistor	Any	Any
156	1	R114	47 K, TRIMM-100X50 X110-64 W	Resistor	Any	Any
157	1	R115	57 K, 1206	Resistor	Any	Any
158	1	SW1	TL1015	Switch button	E-Switch	TL1015BF160QG
159	22	TP3, TP5, TP6, TP8, TP9, TP10, TP18, TP19, TP20, TP21, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP47, TP48	TPSMD-50RD	Test points	Any	Any
160	3	TP33, TP34, TP35	TPSMD-50RD	Test points	Any	Any
161	1	TP46	TPSMD-50RD	Test points	Any	Any
162	1	T1	TLLE20D01	Transformer	Itacoil	TLLE20D01
163	1	T2	TSLETD3402	Transformer	Itacoil	TSLETD3402
164	1	T5	10 mH	Inductor	Itacoil	SCLE25103
					Wurth Elektronik	750317193
165	1	T6	429 µH-SMC037-10011 3	Transformer	Itacoil	TCLPQ262501
166	1	T7	SMLEP1303	Transformer	Itacoil	SMLEP1303
					Wurth Elektronik	750510810

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
167	1	U1	STLUX385A, TSSOP050P-640X120-38	Digital controller for lighting and power conversion applications	ST	STLUX385ATR
168	1	U4	ACPL-M61L-000E-N.M.	OPTO-SOP127P-700X210-6-NO2	Any	Any
169	1	U5	L6398D-N.M.	SOP127P-600X168-8	Any	Any
170	1	U10	L6388ED, SOP127P-600X168-8	HV high and low side driver with embedded bootstrap diode	ST	L6388ED
171	1	U11	PM8841D, SOT23-6	Single channel low-side gate driver	ST	PM8841D
172	1	U12	VIPer06XS, ssop100p-620x175-10	VIPerPlus family: energy saving high voltage converter for direct feedback	ST	VIPER06XSTR
173	1	U13	LK112M33TR, SOT23-5	Low noise and low drop voltage regulator with shutdown function	ST	LK112M33TR
174	2	U14, U15	ACPL-M61L-000E, SOP127P-700X210-6-NO2	Optocoupler	Broadcom	ACPL-M61L-000E
175	1	U16	PM8841D, SOT23-6	Single channel low-side gate driver	ST	PM8841D
176	1	U17	LD2980CM50TR, SOT23-5	Ultra low drop voltage regulators compatible with low ESR output capacitors	ST	LD2980CM50TR
177	1	U18	TS3021ICT, SC70-5	Rail-to-rail 1.8 V high-speed comparator	ST	TS3021ICT
178	1	U19	STLM20W87F, SOT323-5	Ultra-low current, 2.4 V, high precision analog temperature sensor	ST	STLM20W87F
179	1	U20	FT232R, SSOP065P-820X200-28	USB to serial UART interface	FTDI	FT232RL

8 Board connector pinout

Table 6. Connector J8 pinout - AC-DC input

Name	Type	Function
ACIN	Power	Main AC/DC input
ACIN	Power	Main AC/DC input
EARTH	Power	Protection reference level

Table 7. Connector J4 pinout - DC output

Name	Type	Function
+	Power	Positive load connection.
-	Power	Negative load connection.

Table 8. Connector J3 pinout - DALI interfaces

Name	Type	Function
DA	DALI signal	DALI signal for isolated DALI interfaces - without polarization
DA	DALI signal	DALI signal for isolated DALI interfaces - without polarization

Table 9. Connector J9 pinout - 0 - 10 V

Name	Type	Function
+	Positive reference	Positive reference for isolated 0 - 10 V interfaces
-	Negative reference	Negative reference for isolated 0 - 10 V interfaces

Table 10. Connector J48 pin-out – USB-serial interface

NAME	Type	Function
1 - USB Vbus	Power	Power for isolated UART area
2 - USB D-	Negative USB data	Negative USB data
3 - USB D+	Positive USB data	Positive USB data
4 - USB ID	Not connected	Not used
5 - GND	Negative power	Reference ground

Table 11. Connector J1 pinout - SWIM interfaces

Name	Type	Function
1	VCC_SWIM	Power reference from board
2	SWIM	SWIM signal to/from STLUX
3	GND_SWIM	Directly connected to primary GND

Name	Type	Function
4	RESn	Connected to STLUX NRST pin

9 User interface

The user can interact with the board via multiple interfaces: the DALI, serial and 0 - 10 V interface. While the 0 - 10 V interface lets you control the LED current remotely, both DALI and serial interfaces allow the configuration of several operating and start-up parameters. The DALI and 0 - 10 V interface are mutually exclusive and the user can select which one to enable. For safety reasons, the DALI, serial and 0 - 10 V interfaces are isolated.

The serial line is convenient for connecting the evaluation board to additional interfaces, such as Bluetooth®, power line modems, Wi-Fi, etc.

The user can quickly monitor the status of the board by looking at the two status LEDs (red, green) on the board.

9.1 Status LEDs

There are two status LEDs on the board, one green and one red.

- Green LED (status): active when the input power is correct and the STLUX385A device is running.
  - LED on: STLUX385A running
  - LED off: STLUX385A is in low power mode (when the LED string is switched off)
  - LED toggling (1 s on, 1 s off): debug mode active. The board is not operating
  - LED toggling (50 ms on, 6 s off): open circuit detected
- Red LED (failure): used to report an error or the intervention of a protection to preserve the hardware. The cause of error is shown in the GPGUI program.

9.2 DALI implementation

The DALI IEC-62386 contains general requirements for different control gear systems. Therefore, some parameters have been included in the standard that is subdivided in generic and special sections. The STEVAL-ILL066V2 evaluation board includes the generic control gear DALI requirements (extensions 101 and 102 ed.2.0) and the LED specific extension (207 ed.1.0).

In the STEVAL-ILL066V2, the following parameters can be customized according to DALI specifications:

- MEMORY BANK 0 is free to store Customer Parameters (recompile the source code after the change).
- MEMORY BANK 1 is free to store Customer Parameters using the “available DALI command”.
- "POWER ON LEVEL" equal to DAPC 254 level
- "SYSTEM FAILURE LEVEL" equal to DAPC 254 level
- “PHISICAL MIN LEVEL”. The STEVAL-ILL066V2 evaluation board provides a minimum of 10 mA and consequently the minimum DAPC level is set to 1%.
- The STEVAL-ILL066V2 evaluation board implements the logarithmic level table and the linear level table.
- “QUERY OPERATING MODE” response is only 0x00. No other manufacturer mode is implemented.
- “IDENTIFY DEVICE” forces two light level to identify the control gear under identification. The high level is set to 785 mA, the low level is set to 450 mA.

The IEC-62386-207 ed.1.0 extension implements these features:

- The “MIN_FAST_FADE_TIME” value: default value of this parameter on the STEVAL-ILL066V2 evaluation board is 26 ms, as required by the DALI standard. The first available FAST FADE TIME value is 75 ms (“0x03”). It can be increased using DALI commands.
- “QUERY GEAR TYPE” response is “0x0D”: LED power supply integrated, AC supply possible and DC. supply possible
- “QUERY POSSIBLE OPERATING MODES” response is “0x06: AM mode is possible and output is current controlled
- “QUERY FEATURES” response is “0x63”:
  - Short-circuit detection can be queried
  - open circuit detection can be queried
  - thermal shut down can be queried
  - light level reduction due a high temperature

- “DEVICE TYPE” response is “0x06” (LED type).

The DALI stack implemented on the STEVAL-ILL066V2 evaluation board FW is qualified using the IEC-62386 101, 102 ed. 2.0 and 207 ed.1.0 test procedure.

Important:
The DALI certification for STEVAL-ILL066V2 evaluation board, does not release the user of the responsibility to re-check/ qualify the DALI STACK on his or her hardware/software implementation.

9.2.1 List of supported DALI commands

The internal DALI stack has implemented all the standard commands defined in the DALI standard. Also, the LED extension is implemented directly in the STLUX firmware.

Table 12. List of supported DALI commands

Command number	Command code	Mnemonic command name
-	YAAA AAA0 XXXX XXXX	DIRECT ARC POWER CONTROL
0	YAAA AAA1 0000 0000	OFF
1	YAAA AAA1 0000 0001	UP
2	YAAA AAA1 0000 0010	DOWM
3	YAAA AAA1 0000 0011	STEP UP
4	YAAA AAA1 0000 0100	STEP DOWN
5	YAAA AAA1 0000 0101	RECALL MAX LEVEL
6	YAAA AAA1 0000 0110	RECALL MIN LEVEL
7	YAAA AAA1 0000 0111	STEP DOWN AND OFF
8	YAAA AAA1 0000 1000	ON AND STEP UP
9	YAAA AAA1 0000 1001	ENABLE DAPC SEQUENCE
10	YAAA AAA1 0000 1010	GO TO LAST ACTIVE LEVEL
16 - 31	YAAA AAA1 0001 XXXX	GO TO SCENE
32	YAAA AAA1 0010 0000	RESET
33	YAAA AAA1 0010 0001	STORE ACTUAL LEVEL IN THE DTR
34	YAAA AAA1 0010 0010	SAVE PERSISTENT VARIABLE
35	YAAA AAA1 0010 0011	SET OPERATING MODE (DTR0)
36	YAAA AAA1 0010 0100	RESET MEMORY BANK (DTR0)
37	YAAA AAA1 0010 0101	IDENTIFY DEVICE
42	YAAA AAA1 0010 1010	STORE THE DTR AS MAX LEVEL
43	YAAA AAA1 0010 1011	STORE THE DTR AS MIN LEVEL
44	YAAA AAA1 0010 1100	STORE THE DTR AS SYSTEMFAILURE LEVEL
45	YAAA AAA1 0010 1101	STORE THE DTR AS POWER ONLEVEL
46	YAAA AAA1 0010 1110	STORE THE DTR AS FADE TIME
47	YAAA AAA1 0010 1111	STORE THE DTR AS FADE RATE
48	YAAA AAA1 0011 0000	SET EXTENDED FADE TIME (DTR0)
64 - 79	YAAA AAA1 0100 XXXX	STORE THE DTR AS SCENE
80 - 95	YAAA AAA1 0101 XXXX	REMOVE FROM SCENE
96 - 111	YAAA AAA1 0110 XXXX	ADD TO GROUP
112 - 127	YAAA AAA1 0111 XXXX	REMOVE FROM GROUP

Command number	Command code	Mnemonic command name
128	YAAA AAA1 1000 0000	STORE DTR AS SHORT ADDRESS
129	YAAA AAA1 1000 0001	ENABLE WRITE MEMORY
144	YAAA AAA1 1001 0000	QUERY STATUS
145	YAAA AAA1 1001 0001	QUERY CONTROL GEAR
146	YAAA AAA1 1001 0010	QUERY LAMP FAILURE
147	YAAA AAA1 1001 0011	QUERY LAMP POWER ON
148	YAAA AAA1 1001 0100	QUERY LIMIT ERROR
149	YAAA AAA1 1001 0101	QUERY RESET STATE
150	YAAA AAA1 1001 0110	QUERY MISSING SHORT ADDRESS
151	YAAA AAA1 1001 0111	QUERY VERSION NUMBER
152	YAAA AAA1 1001 1000	QUERY CONTENT DTR
153	YAAA AAA1 1001 1001	QUERY DEVICE TYPE
154	YAAA AAA1 1001 1010	QUERY PHYSICAL MINIMUM LEVEL
155	YAAA AAA1 1001 1011	QUERY POWER FAILURE
156	YAAA AAA1 1001 1100	QUERY CONTENT DTR1
157	YAAA AAA1 1001 1101	QUERY CONTENT DTR2
158	YAAA AAA1 1001 1110	QUERY OPERATING MODE
159	YAAA AAA1 1001 1110	QUERY LIGHT SOURCE TYPE
160	YAAA AAA1 1010 0000	QUERY ACTUAL LEVEL
161	YAAA AAA1 1010 0001	QUERY MAX LEVEL
162	YAAA AAA1 1010 0010	QUERY MIN LEVEL
163	YAAA AAA1 1010 0011	QUERY POWER ON LEVEL
164	YAAA AAA1 1010 0100	QUERY SYSTEM FAILURE LEVEL
165	YAAA AAA1 1010 0101	QUERY FADE TIME/FADE RATE
166	YAAA AAA1 1010 0110	QUERY MANUFACTURER SPECIFIC MODE
167	YAAA AAA1 1010 0111	QUERY NEXT DEVICE TYPE
168	YAAA AAA1 1010 1000	QUERY EXTENDED FADE TIME
169	YAAA AAA1 1011 1001	QUERY CONTROL GEAR FAILURE
176 - 191	YAAA AAA1 1011 XXXX	QUERY SCENE LEVEL (SCENES 0 - 15)
192	YAAA AAA1 1100 0000	QUERY GROUPS 0 - 7
193	YAAA AAA1 1100 0001	QUERY GROUPS 8 - 15
194	YAAA AAA1 1100 0010	QUERY RANDOM ADDRESS (H)
195	YAAA AAA1 1100 0011	QUERY RANDOM ADDRESS (M)
196	YAAA AAA1 1100 0100	QUERY RANDOM ADDRESS (L)
197	YAAA AAA1 1100 0101	READ MEMORY LOCATION
224 - 254	YAAA AAA1 111X XXXX	Refer to standard IEC62386 - part 207
255	YAAA AAA1 1111 1111	QUERY EXTENDED VERSION NUMBER
256	1010 0001 0000 0000	TERMINATE
257	1010 0011 XXXX XXXX	DATA TRANSFER REGISTER (DTR)
258	1010 0101 XXXX XXXX	INITIALISE

Command number	Command code	Mnemonic command name
259	1010 0111 0000 0000	RANDOMISE
260	1010 1001 0000 0000	COMPARE
261	1010 1011 0000 0000	WITHDRAW
262	1010 1100 0000 0000	PING
264	1011 0001 HHHH HHHH	SEARCHADDRH
265	1011 0011 MMMM MMMM	SEARCHADDRM
266	1011 0101 LLLL LLLL	SEARCHADDRL
267	1011 0111 0AAA AAA1	PROGRAM SHORT ADDRESS
268	1011 1001 0AAA AAA1	VERIFY SHORT ADDRESS
269	1011 1011 0000 0000	QUERY SHORT ADDRESS
270	1011 1101 0000 0000	PHYSICAL SELECTION
272	1100 0001 XXXX XXXX	ENABLE DEVICE TYPE X
273	1100 0011 XXXX XXXX	DATA TRANSFER REGISTER 1 (DTR1)
274	1100 0101 XXXX XXXX	DATA TRANSFER REGISTER 2 (DTR2)
275	1100 0111 XXXX XXXX	WRITE MEMORY LOCATION

Table 13. IEC62386 part 207 - command extension

Command number	Command code	Mnemonic command name
224	YAAA AAA1 1110 0000	REFERENCE SYSTEM POWER – command not implemented
225	YAAA AAA1 1110 0001	ENABLE CURRENT PROTECTOR – command not implemented
226	YAAA AAA1 1110 0010	DISABLE CURRENT PROTECTOR – command not implemented
227	YAAA AAA1 1110 0011	SELECT DIMMING CURVE
228	YAAA AAA1 1110 0100	STORE DTR AS FAST FADE TIME
237	YAAA AAA1 1110 1101	QUERY GEAR TYPE
238	YAAA AAA1 1110 1110	QUERY DIMMING CURVE
239	YAAA AAA1 1110 1111	QUERY POSSIBLE OPERATING MODES
240	YAAA AAA1 1111 0000	QUERY FEATURES
241	YAAA AAA1 1111 0001	QUERY FAILURE STATUS
242	YAAA AAA1 1111 0010	QUERY SHORT-CIRCUIT
243	YAAA AAA1 1111 0011	QUERY OPEN CIRCUIT
244	YAAA AAA1 1111 0100	QUERY LOAD DECREASE – command not implemented
245	YAAA AAA1 1111 0101	QUERY LOAD INCREASE – command not implemented
246	YAAA AAA1 1111 0110	QUERY CURRENT PROTECTOR ACTIVE – command not implemented
247	YAAA AAA1 1111 0111	QUERY THERMAL SHUT DOWN
248	YAAA AAA1 1111 1000	QUERY THERMAL OVERLOAD
249	YAAA AAA1 1111 1001	QUERY REFERENCE RUNNING - not implemented
250	YAAA AAA1 1111 1010	QUERY REFERENCE MEASUREMENT FAILED – command not implemented
251	YAAA AAA1 1111 1011	QUERY CURRENT PROTECTOR ENABLED – command not implemented
252	YAAA AAA1 1111 1100	QUERY OPERATING MODE

Command number	Command code	Mnemonic command name
253	YAAA AAA1 1111 1101	QUERY FAST FADE TIME
254	YAAA AAA1 1111 1110	QUERY MIN FAST FADE TIME
255	YAAA AAA1 1111 1111	QUERY EXTENDED VERSION NUMBER
272	1100 0001 0000 0110	ENABLE DEVICE TYPE 6

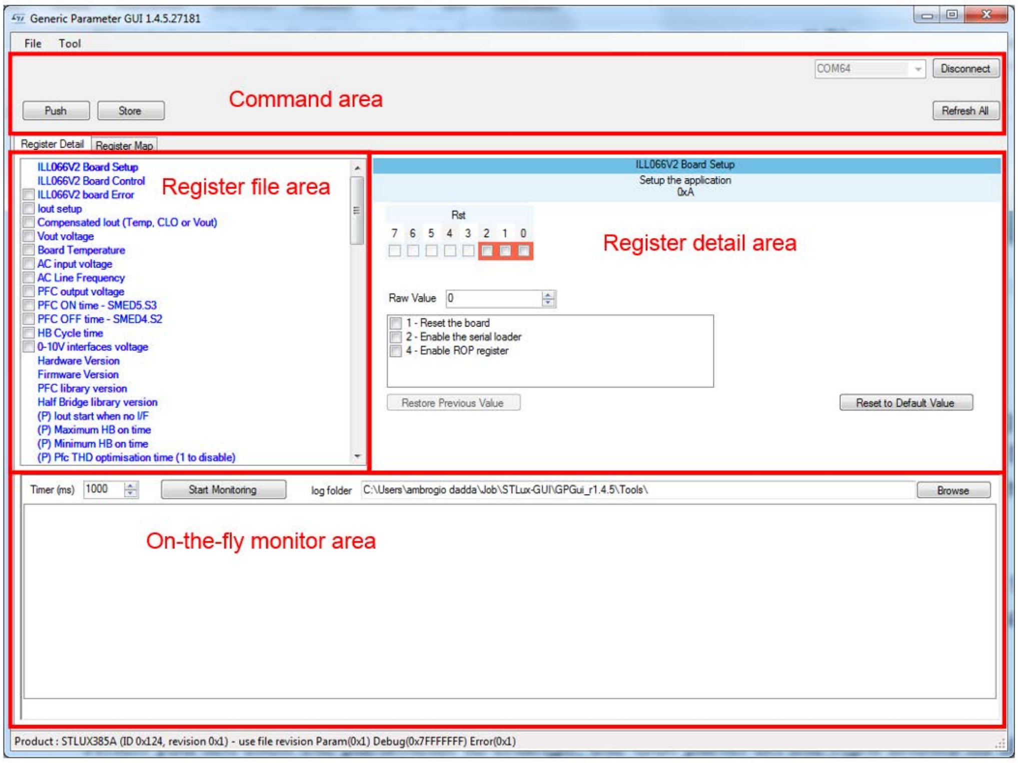
Refer to the IEC 62383 DALI standard on www.iec.ch for further information.

9.3 GPGUI interface on STEVAL-ILL066V2 evaluation board

The GPGUI interface lets you monitor several evaluation board parameters and configure the board before you use it. The program runs on a PC; it communicates through a COM interface with the evaluation board and uses a standard miniUSB-USB cable.

When the GPGUI program connects with the board, it reads all the current board parameter values, which are then displayed in the GPGUI window. The board parameters are not automatically updated on the GPGUI, but you can force a refresh.

Figure 21. - Generic Parameter GUI



The GPGUI window is divided into four different areas:

Command area to connect, disconnect, refresh all and push/store the changed parameters on the STEVAL-ILL066V2 evaluation board.

Register file area to identify the parameter to monitor, read or write. Select one file in this area and the Register detail area shows information for this register. There is more than one register type.

1. If the register name it is not preceded by a check box, (P) or (C), it is a generic, read only or board setup register. Only the first two registers are board setup registers, which is confirmed on the board when the Push button is used.

2. If the register name is preceded by a check box, it is a read/write/monitor register.
3. If the register name are preceded by a (P), it is a board parameter file register and only the Store button confirms any change on the board.(1)
4. If the register name is preceded by a (C), it is a CLO parameter file register. The Push button stores the changed value onto the evaluation board. Any changes in this area is apply immediately to the board when Push button is used. The CLO parameters are only present only if the CLO module is enabled and loaded on the board.

1. New values are only applied to the board after a hard reset (power off – power on).

Register detail area shows details for the register selected in Register file area. You can monitor some values cyclically in this windows without enabling the On-the-fly monitor area. It is also possible to immediately read a value or store a changed value. When you choose another register in the Register detail area, the active monitor function is ends automatically.

To restore a default value, press the Reset to Default value button.

If the Read button appears in the Register detail area, this button lets you read evaluation board parameters on the fly.

The Write button lets you change evalution board parameters on the fly for the Iout setup and On Board Time registers only. The Iout value is overwritten if the DALI or 0-10V is active.

For read/write/monitor registers, the Auto refresh check box refreshes parameter values of the evaluation board during operation at the frequency set in the time (ms) frame. This features is available for debug purposes; you should set a relatively long interval (more than 1 or 2 seconds) due to the CORE load.

On-the-fly monitor area is used when one or more register check boxes are selected to show periodic (according to the Timer (ms) frame) data acquired from the evaluation board.

Click on the Start Monitoring button to begin viewing the selected parameter values. When enabled, the value shown in the window is also logged in the Excel file path given in the log folder frame. Take care not to overload CORE activity with this feature.

Important: *Before powering off or removing the UART cable, click the Disconnect button in the GPGUI interface.*

Note: *When the board is set in low power mode (when output light is OFF using DALI commands), the GPGUI ceases activity until the board exits low power mode is removed.*

Register files modified by the user are highlighted in red. To commit these changes:

- for type (a), type (b) and type (d) registers, click the Push button above the parameters list.
- for type (c) registers, click the Store button.

Click the Refresh All button to refresh the GUI with current board parameters.

Table 14. STEVAL-ILL066V2 parameters

#	Type	Parameter name	Action	Def	Function
1	(a)	Board Setup	RD/PUSH	0x00	Bit field register: 0x01 - Resets the board when Push button is clicked. 0x02 - Enables serial loads. Push button confirms this action and is active only after the next power on 0x04 - The ROP register is enabled and reading of the memory code area is disabled. The Push button confirms this action. All the GPGUI functions (read/write/monitor) are disabled

#	Type	Parameter name	Action	Def	Function
2	(a)	Board Control	RD/PUSH	0x2E	Bit field register: 0x01 - Board is disabled and debug mode is active. 0x02 – Activates PFC functionality 0x04 - Activates HB functionality 0x08 - Enables the DALI interface and the DALI stack drive the output current 0x10 - Enable the 0-10V interfaces to drive the output current (can only be enabled when DALI is disabled) 0x20 - HB loops are closed and control the output current 0x40 - Iout is compensated by reading the Vout value.
3		Board Error	RD/MON	n.d.	Reports the last board error (see Section 9.4 Error codes)
4	(b)	Iout setup	RD/WR/MON	n.d.	The Register detail area enables changing the output current using the mA value or "Il" value. When one field is entered, the corresponding parameters are calculated and displayed.
5		Compensated Iout (Temp, CLO or Vout)	RD/MON	n.d.	Is the real Iout current driven by the board. This value differs to iout setup because the thermal protection, CLO and Vout compensation can alter the real output current.
6		Vout voltage	RD/MON	n.d.	Shows the output voltage acquire by the STLUX. The internal data ("raw data") and the approximate Voltage ("Formatted Value") are returned.
7		Board Temperature	RD/MON	n.d.	Shows the board temperature in degrees centigrade.
8		AC input voltage	RD/MON	n.d.	Shows the AC input voltage.
9		AC Line Frequency	RD/MON	n.d.	Shows the AC input frequency acquired by STLUX.
10		PFC output voltage	RD/MON	n.d.	Shows the PFC output voltage acquired by the STLUX.
11		PFC ON time - SMED5.S3	RD/MON	n.d.	Shows the variable part of the PFC ON time.
12		PFC OFF time - SMED4.S2	RD/MON	n.d.	Shows the variable part of the PFC OFF time.
13		HB cycle time	RD/MON	n.d.	Shows the variable part of the HB ON time.
14		0-10V interfaces voltage	RD/MON	n.d.	Monitors the 0-10V voltage at the 0-10V connector interface.
15		Hardware version	REFRESH	n.d.	The hardware version.
16		Firmware version	REFRESH	n.d.	The firmware version.
17		PFC library version	REFRESH	n.d.	The PFC library version.
18		Half Bridge library version	REFRESH	n.d.	The Half Bridge library version.
19	(c)	(P) Iout start when no I/F	STORE	539	The power on output current when DALI or 0-10 interfaces are disabled.
20	(c)	(P) Maximum HB on time	STORE	950	The maximum controlled HB on time in 96MHz clock period. This parameter define the minimum HB frequency
21	(c)	(P) Minimum HB on time	STORE	61	The minimum controlled HB on time in 96MHz clock period. This parameter defines the maximum HB frequency.
22	(c)	(P) Pfc THD optimization time (1 to disable)	STORE	2000	This parameter defines the maximum waiting time for the THD optimizer circuit. The value represents the number of 96MHz cycles.
23	(c)	(P) DAC level on emergency	STORE	7	Define the DAC level used when an error is detected by the FW.
24	(c)	(P) DAC level during high Vac	STORE	8	Define the DAC level when the Vac input line is detected as the HIGH level

#	Type	Parameter name	Action	Def	Function
25	(c)	(P) DAC level during middle Vac	STORE	11	Define the DAC level when the Vac input line is detected as the MIDDLE level
26	(c)	(P) DAC level during low Vac	STORE	13	Define the DAC level when the Vac input line is detected as the LOW level
27	(c)	(P) Vac startup level	STORE	269	Define the minimum Vac input voltage to allow evaluation board startup.
28	(c)	(P) Vac UVLO voltage	STORE	267	Define the low Vac level to detect the input UVLO voltage.
29	(c)	(P) Vac start high range zone	STORE	518	Define the high range zone when the input Vac is more than this level.
30	(c)	(P) Vac start middle range zone	STORE	422	Define the middle range zone when the input Vac is between this level and high range.
31	(c)	(P) Vac start low range zone	STORE	251	Define the low range zone when the input Vac is between this level and middle range.
32	(c)	(P) PFC output UVLO high range zone	STORE	329	Define the level to detect the PFC output UVLO when high zone is selected.
33	(c)	(P) PFC output UVLO middle range zone	STORE	289	Define the level to detect the PFC output UVLO when middle zone is selected.
34	(c)	(P) PFC output UVLO low range zone	STORE	189	Define the level to detect the PFC output UVLO when low zone is selected.
35	(c)	(P) PFC Controlled ON time used during start-up	STORE	70	Define the PFC ON time during PFC startup.
36	(c)	(P) PFC Controlled OFF time used during start	STORE	1	Define the PFC OFF time during PFC startup.
37	(c)	(P) Time (mS) to detect AC missing	STORE	100	Define the time to detect the AC input line missing
38	(c)	(P) Output voltage to detect no load	STORE	818	Define the Vout to detect the load disconnect
39	(c)	(P) HB propagation delay time	STORE	30	Define the hardware propagation delay between STLUX output and SMED input (STLUX adds an internal 50 ns).
40	(c)	(P) HB high side symmetry time	STORE	4	Define the SMED clock increment to create a symmetric HB signal on HB middle point.
41	(c)	(P) HB dead time	STORE	33	Define the HB dead time used by the SMED.
42	(c)	(P) PFC Proportional Gain	STORE	130	Define the PFC PI proportional gain parameter.
43	(c)	(P) PFC Proportional divisor	STORE	13	Define the PFC PI proportional divisor parameter.
44	(c)	(P) PFC Integral Gain	STORE	140	Define the PFC PI integral gain parameter.
45	(c)	(P) PFC Integral divisor	STORE	15	Define the PFC PI integral divisor parameter.
46	(c)	(P) High level to trig PFC fast reaction	STORE	1023	Define the PFC high output voltage to trigger the PFC fast reaction.
47	(c)	(P) Low level to trig PFC fast reaction	STORE	850	Define the PFC low output voltage to trigger the PFC fast reaction.
48	(c)	(P) PFC fast reaction gain	STORE	500	Define the PFC fast reaction gain.
49	(c)	(P) Vout to detect short circuit	STORE	100	Define the trigger level below which an output short-circuit is detected.
50	(c)	(P) Temperature to shut down	STORE	900	Define the temperature above which the power shut-down is triggered.
51	(c)	(P) Temperature to trigger power reduction	STORE	750	Define the temperature above which power reduction is triggered.
52	(c)	(P) Il slope when power reduction	STORE	100	Define the “Il” number reduction every centigrade starting from temperature to trigger power reduction.

#	Type	Parameter name	Action	Def	Function
53	(d)	(C) CLO flags	PUSH	0	Bit field: 1 - Raises the on-board time to apply the CLO increment. 2 - Clears the on-board time to 0.
54	(d)	(C) CLO board time	RD/WR/ STORE	n.d.	The on-board time in seconds before first board power on.
55	(d)	(C) CLO slot [0 to 15] time	PUSH	0	Define the time (khours) when the increment is applied. The time is the sum of the previous slot times.
56	(d)	(C) CLO slot [0 to 15] inc	PUSH	0	The increment (between 0 and 15%) applied when the on-board time reaches the time specified by the sum of the previous slot times.

Note: *Every parameter has a minimum and maximum value that cannot be exceeded.*

9.3.1 Current regulation on STEVAL-ILL066V2 evaluation board

The GPGUI Iout setup parameter lets you change the Iout current on the LED load. This command should be used only when DALI or 0 - 10 V interfaces are not active as they have higher priority than the GPGUI command. The possible GPGUI values range from 2 (minimum current) to 4094 (maximum current). For the STEVAL-ILL066V2 evaluation board, the GPGUI parameters should be configured between 539 (minimum current) and 4093 (maximum current).

Note: *The GPGUI program is not aware of the output configuration and always shows an output current of 1 A scale even if a 180 V output voltage is selected.*

The LED can be switched off using parameter 0. Once the LEDs are switched off with the GPGUI command, then the LED can only be switched on again via the GPGUI command (and not from 0 - 10 V or DALI interface).

The STEVAL-ILL066V2 evaluation board implements the output current slope rate at 39.6 mA/ms (from min. to max., 26 ms) to protect the output capacitors and LED strings.

Caution:
Do not set a current level greater than the maximum current allowed by the LED strings connected. The board injects the configured current regardless of the LED ratings.

The following table defines the value imposed by the “raw value” and the corresponding output current values. The GPGUI show an approximated output current (±10 mA) in the “formatted value” field.

Table 15. Relation between raw value and formatted value in GPGUI - Iout setup parameter

GPGUI value	Output current (1 A scale)	Output current (500mA scale)
539	10 mA	5 mA
661	100 mA	50 mA
800	200 mA	100 mA
936	300 mA	150 mA
1074	400 mA	200 mA
1356	500 mA	250 mA
1758	600 mA	300 mA
2159	700 mA	350 mA
2561	800 mA	400 mA
2962	900 mA	450 mA
3364	1000 mA	500 mA
3766	1100 mA	550 mA

GPGUI value	Output current (1 A scale)	Output current (500mA scale)
4093	1181 mA	590 mA

9.3.2 CLO function on STEVAL-ILL066V2 evaluation board

The Constant Light Output (CLO) function compensates the output light level during the LED life. It uses the on board time and a modifiable table to simulate the light variation over the LED life. You can specify the time and the increment applied during the LED life.

The CLO function is disabled by default in the parameter file.

The on board time counts a maximum of 232-1 seconds (more than 136 years), which is automatically saved to an EEPROM area every power-off and restored at every power-on (when the AC power line is used). The on board time is not saved when the board is powered by the 12 Vdc-14 Vdc.

The CLO function is programmable by the user using the GPGUI interface. The maximum CLO (Iout) increment is +20% and you should take this into account in your board design if you want to use the full CLO increment. You must set up an appropriate CLO table ("CLO_ct[]" on clo.c file) to compensate the variation in your particular LEDs.

Note: The STEVAL-ILL066V2 evaluation board is only able to use Iout increments of +13% to +15% due to a hardware limitation.

The CLO function uses sixteen slots (from 0 to 15) to set up the user LED light variation. Every slot is indexed to identify the slot, with a time to identify the hours (x1000) and with the percentage increment (from 0% to 20%).

- The time parameter defines the waiting increment (Khrs) before applying the CLO output current compensation (increment), from 1 ($x10^3$) hrs to 100 ($x10^3$) hrs. The total time applied is the sum of the previous time slots starting from slot 0 plus the time of actual slot. The CLO table ends when this parameter (time) is set to 0. Any following CLO slot after s slot with time=0 is ignored.
- The increment parameters define the percentage to add to the actual Iout value. This increment is applied when the on board time is equal to or more than the sum of the previous times plus the current time slot. You can set increments from 0% to 20%. The percentage to add is applied at every output current level.

A simple example is shown below:

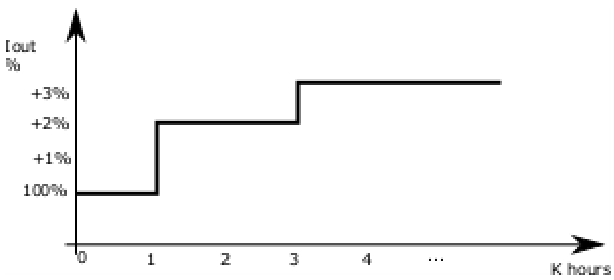
- The first slot (#0) waits 1 Khours before applying a 2% Iout increment; staring from the very first power on to 1000 hours on board time, the output is the expected current without CLO compensation.
- The second slot (#1) waits 2 Khours before applying a 3% Iout increment.
- The last "cl" command (slot #2) ends the CLO table by setting the time increment to 0.

The equivalent GPGUI setup is this:

- slot 0: time=1; increment=2
- slot 1: time=2; increment=3
- slot 2: time=0 (end of CLO table); increment not considered

The result of the previous CLO setup is shown in the next figure.

Figure 22. Simple CLO increment graph



The CLO speed-up flag instructs the CLO function to count hours instead of Khours. Whenerever the board is powered on, this flag is cleared so that counting resumes with the default Khour scale.

The reset CLO time flag clears the on board timer to zero.

9.3.3 Temperature protection on the STEVAL-ILL066V2 evaluation board

The STEVAL-ILL066V2 FW implements temperature protection. The temperature is acquired from the ADC ch 7 line using a trimmer. The acquired voltage is converted to temperature using the STLM20W87F second order parabolic equation.

The STEVAL-ILL066V2 FW implements two temperature trigger points and one level reduction.

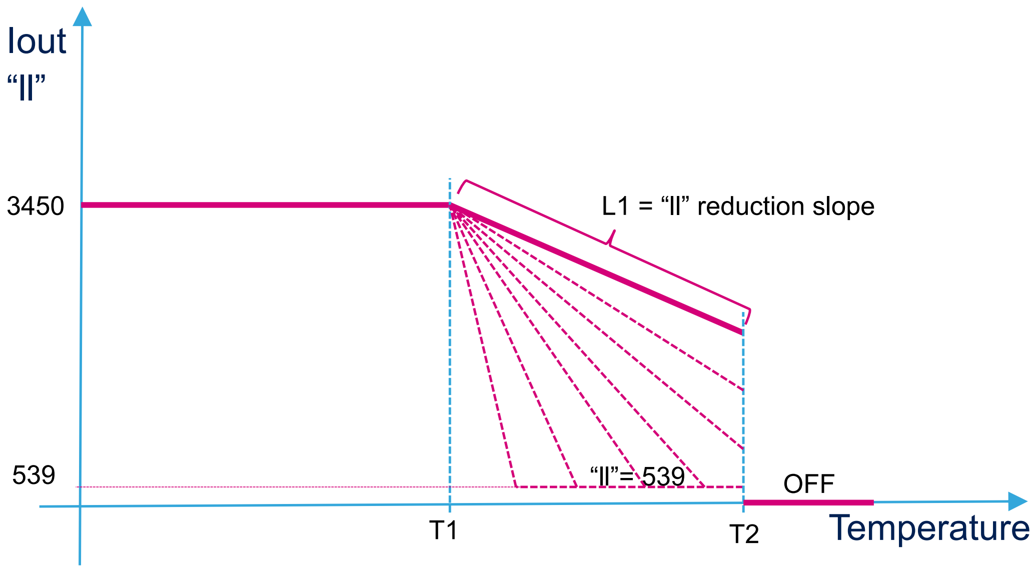
- T1 - Temperature to commence light level reduction. The reduction slope is defined by the L1 parameter.
- T2 - Temperature to set the thermal shut down trip point.
- L1 – The “ll” reduction slope every degree unit. This reduction is applied as is to every Iout level.

Note: T1 and T2 must be between 1 °C and 120 °C

If the T1 is higher than T2, the T1 behavior is never applied.

The hysteresis applied on the T2 trigger point is 10 °C; i.e., when the temperature exceeds T2, the restart temperature is T2 – 10 °C.

Figure 23. STEVAL-ILL066V2 FW temperature protection regime



9.4 Error codes

The STLUX385A firmware performs several system checks during execution. When an error is detected, a corresponding string is displayed on the GPGUI when the user reads the parameter.

Table 16. Error codes and actions performed by the STEVAL-ILL066V2 application FW

Error codes	Cause	Action
1	DALI stack error	No action
2	Reset not from Power ON	No action
3	PFC Overcurrent Protection	Stops HB, PFC and restarts every 4 s
4	PFC input UVLO protection	Stops PFC and HB, automatically restarts if AC input voltage returns to correct zone
5-9	Not used	No action
10	PFC over time to start	Restart PFC activity every 4 s
11	Half Bridge time stamp error	Output current is not regulated

Error codes	Cause	Action
12	FLASH write error	The application startup value is not restored due to a write error check
13	FLASH write error	Some DALI default initializations are missing
14	Half Bridge - No load detection	Stops HB and PFC, automatically checks and restarts every 6 s
15	Not used	No action
16	Output in short circuit	The STLUX detects an output short-circuit. Restarts automatically every 6 s when short is removed
17	Thermal Shut Down	Thermal Shut Down triggered; restarts when temperature returns to an allowed range
18	Debug mode active	The Debug mode is selected, no board activity
19	Serial Loader not allowed	The serial loader is not enabled on this STLUX chip
20	GPGUI Store CMD not implemented	GPGUI interaction error, update xml file - No error on evaluation board
21	GPGUI Index receive not implemented	GPGUI interaction error, update xml file - No error on evaluation board
22	ROP active, no change allowed	ROP is active, no GPGUI change allowed
23	GPGUI writing to a read only register	GPGUI error, update xml file - No error on evaluation board
24	GPGUI Board configuration error	User configuration error, change GPGUI configuration and repeat

9.5 0 - 10 V interface

The 0 - 10 V interfaces can be enabled using the GPGUI command described in Section 9.3 GPGUI interface on STEVAL-ILL066V2 evaluation board. By default, the 0 - 10 V interface is disabled on the STEVAL-ILL066V2 evaluation board. The 0 - 10 V and DALI interfaces are mutually exclusive.

The 0 - 10 V reference signal can be generated via a 0 - 10 V generator, or you can simulate the external signal with a potentiometer. The correct value of this potentiometer is 110 KΩ, which can be obtained using a 10 KΩ and 100 KΩ potentiometer in series. The 100 KΩ potentiometer is used when the output voltage is over 5 V, while the 10 KΩ potentiometer is used when the output voltage is below 5 V.

The power required to read the input voltage is automatically generated by the STEVAL-ILL066V2 evaluation board. This solution provides excellent insulation for all the features of the evaluation board. The maximum 0 - 10 V interface input voltage accepted here is 15 V.

The on/off transaction is regulated via a hysteresis mechanism. LEDs are switched off when the 0 - 10 V interface reaches V < 1 V. LEDs are switched on when V > 1.25 V.

Table 17. Relationship between 0 - 10 V voltage and LED output current

Voltage applied to connector J9	Output current (1 A scale)	Output current (500 mA scale)
More than 10 V and less then 15 V	1 A	500 mA
10 V	1 A	500 mA
9 V	900 mA	450 mA
8 V	800 mA	400 mA
7 V	700 mA	350 mA
6 V	600 mA	300 mA
5 V	500 mA	250 mA
4 V	400 mA	200 mA
3 V	300 mA	150 mA
2 V	200 mA	100 mA
1 V	100 mA	50 mA

Voltage applied to connector J9	Output current (1 A scale)	Output current (500 mA scale)
Below 1 V	Off	Off

10 Measurements

This section details board performance, power consumption, output current precision etc.

10.1 Output current precision

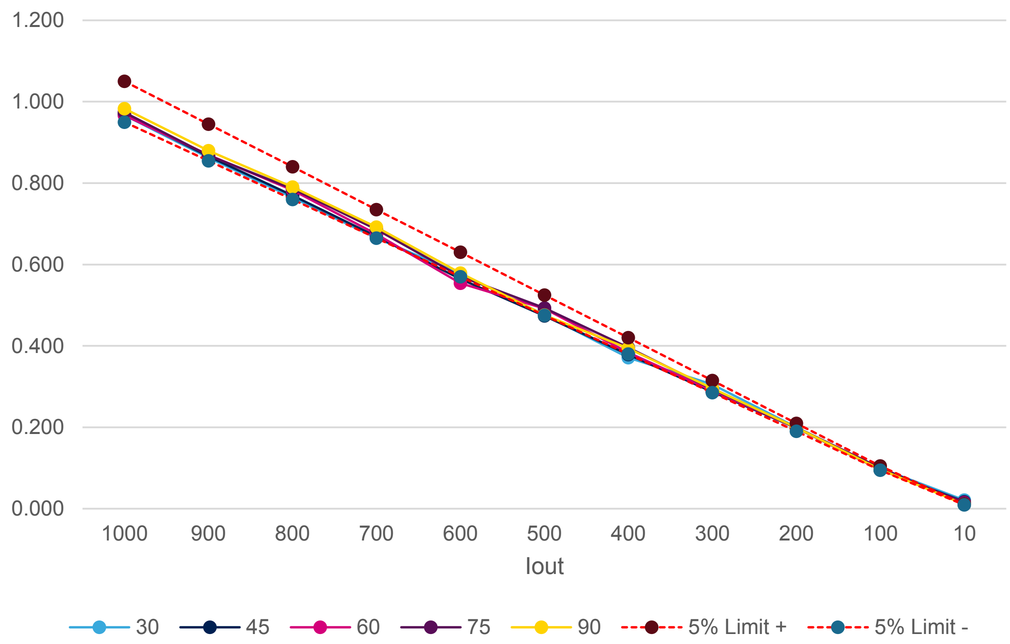
In this test we demonstrate the correct current regulation at different Vf levels and different output current (imposed by the DALI stack in linear mode). The DALI working points are 1%, 25%, 50%, 75% and 100% of the nominal output power.

Table 18. Output current precision and Figure 24. Output current precision when Iout vs Vout compensation is active are acquired enabling the "Iout vs Vout compensation" flag to increase the Iout current precision.

Table 18. Output current precision

Nominal output current		Vf = 30 V	Vf = 45 V	Vf = 60 V	Vf = 75 V	Vf = 90 V
DALI	mA	mA	mA	mA	mA	mA
1%	10	15	13	11	10	8.5
25%	250	258	245	242	243	238
50%	500	545	475	475	488	494
75%	750	740	733	742	744	750
100%	1000	989	981	991	994	996

Figure 24. Output current precision when Iout vs Vout compensation is active



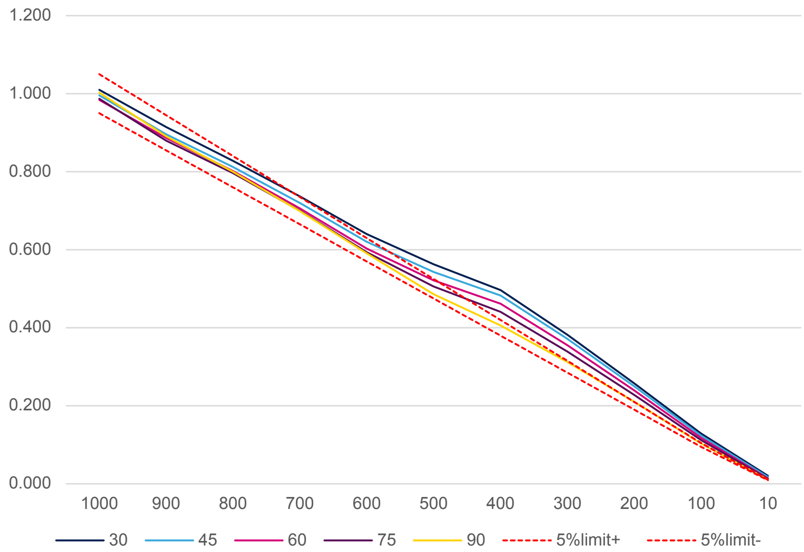
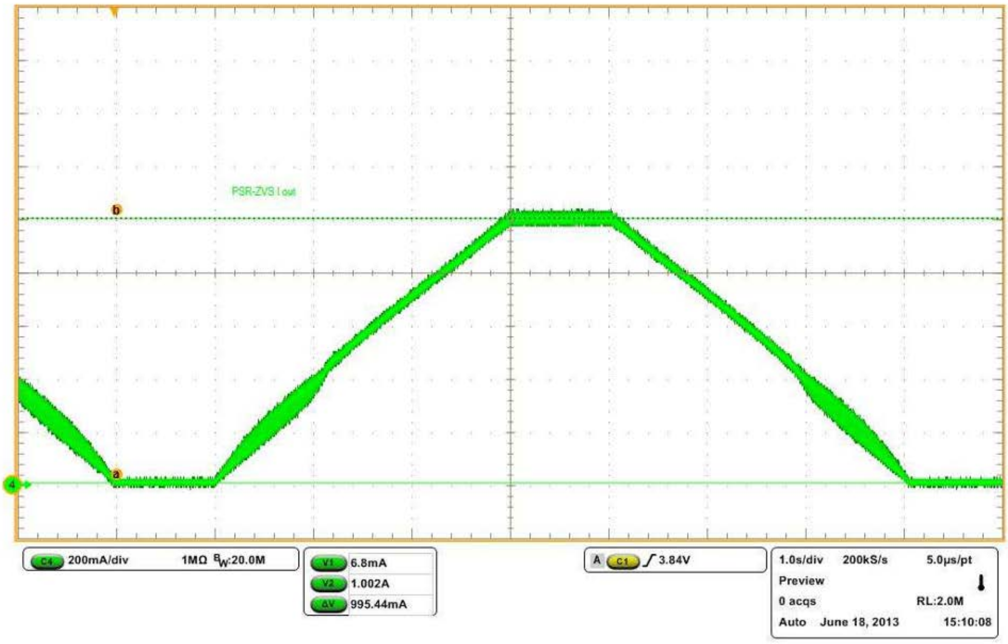


Figure 25. Output current precision when Iout vs Vout compensation is not active

10.2 Output current regulation

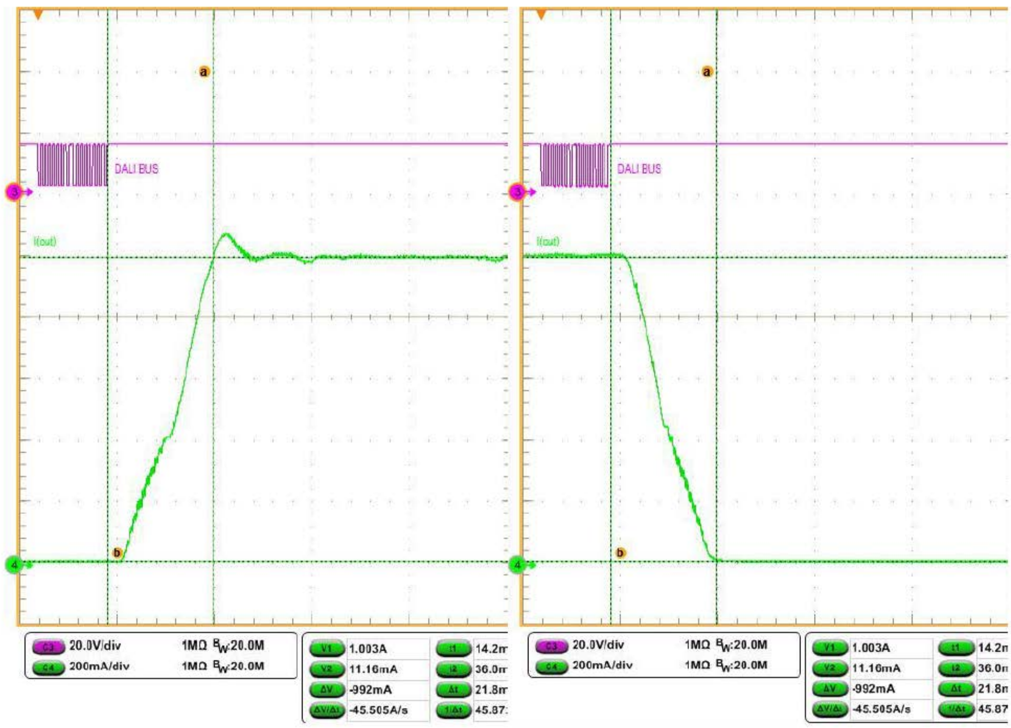
This section shows the current transaction from minimum to maximum power and from maximum to minimum power. The output current level is generated using the DAPC(254) and DAPC(85) DALI commands; each command is sent every 4 seconds. The output is captured with the current probe acquired on V_f = 90 V. The total transaction (up or down) is completed in 3 seconds using DALI fade transition and the linear table.

Figure 26. **Output current ramp-up and down**



The minimum Iout change (green line) is less than 26 ms, as per DALI requirements (see figure below).

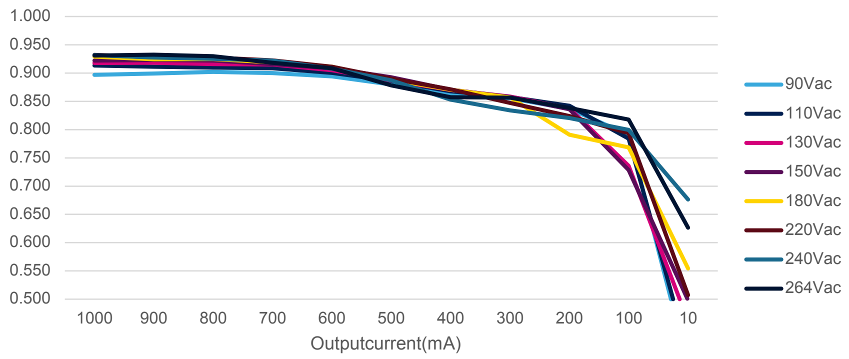
Figure 27. **Iout falling and rising time without DALI fading**



10.3 Efficiency

Figure 28. Evaluation board efficiency vs Load and Vac input shows the efficiency of the evaluation board at different input AC voltages and at different output power. The output power is applied via DALI commands and the output current is 10 mA and every 100 mA in the 100 mA to 1 A range. The output voltage of this test is fixed at 90 V. The board efficiency peaks at 92% for high loads. When the entire input voltage range is considered, the maximum efficiency at high load is more than 90%.

Figure 28. Evaluation board efficiency vs Load and Vac input



10.4 IDLE and minimum power

Table 19. Board standby power and power consumption in different conditions shows the power required by the STEVA-ILL066V2 evaluation board when the DALI puts the evaluation board in standby mode with the light-off command (no current on output LEDs string).

The table also shows the minimum input power when the output current is an open circuit, short-circuit or the lowest allowed current (~10 mA). All the values in the table are acquired using a mean value over 36 s.

Table 19. Board standby power and power consumption in different conditions

AC input voltage	standby (W)	Open Load (W)	Short-circuit (W)	Active - output 10mA@75Vf (W)
90	0.154	0.335	0.320	2.07
110	0.159	0.330	0.273	1.94
130	0.165	0.340	0.275	1.83
160	0.175	0.380	0.290	1.70
180	0.184	0.400	0.350	1.63
220	0.204	0.405	0.380	1.55
264	0.230	0.425	0.390	1.50

10.5 Demonstration board power factor and THD

The following figure show the power factor and the THD distortions of the STEVAL-ILL066V2 evaluation board. The value is given for different input AC voltages and under different load conditions.

Figure 29. Demonstration board - power factor vs. output power at different Vin

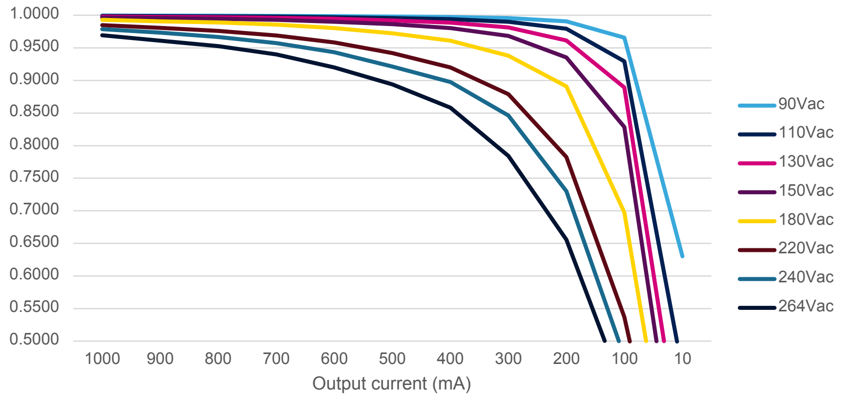


Figure 30. Demonstration board - THD distortion vs. output power at different Vin

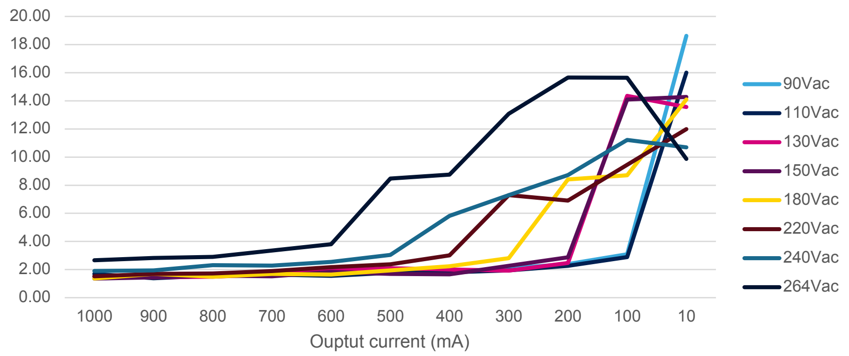


Figure 31. Input current at 220ac with THD optimizer disabled

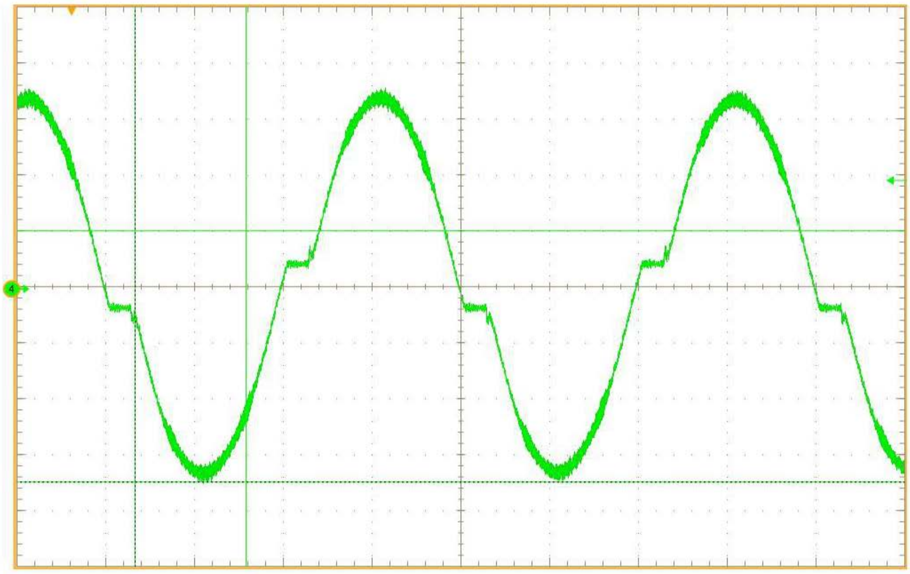


Figure 32. Input current at 220ac with THD optimizer enabled

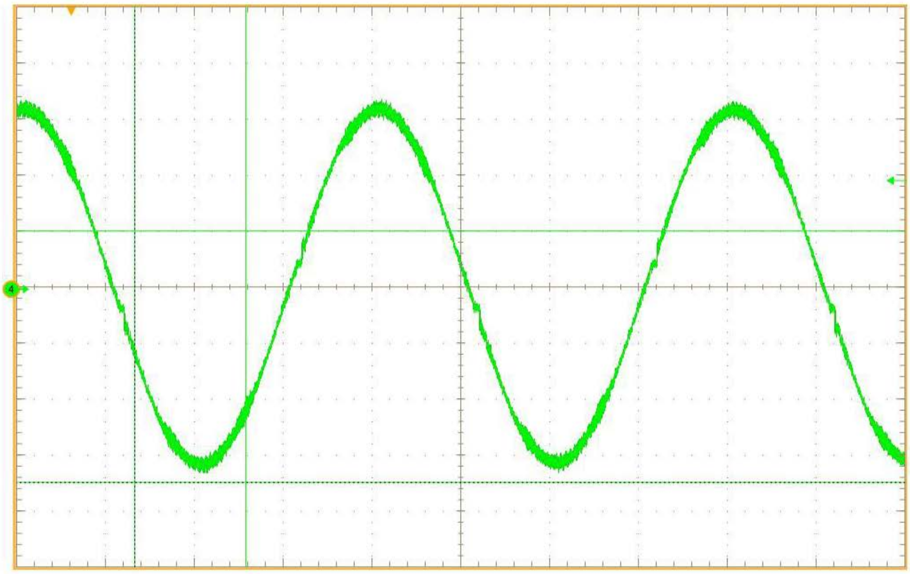


Table 20. THD harmonic detail for different loads

Request in IEC-61000-3-2 (2005)		Result in STEVAL-ILL066V2 at 220Vac Output power (%)		
Harmonic number	Limit %	100%	50%	10%
2	2	0.22	0.5	1.38
3	30 * ƛ (PF)	(30*0.948)=28 result 0.58	(30*0.834)=25 result 1.087	(30*0.327)=9.8 result 2.84
5	10	0.23	0.71	5.69
7	7	0.53	0.85	3.5
9	5	0.25	0.47	3.2

Request in IEC-61000-3-2 (2005)		Result in STEVAL-ILL066V2 at 220Vac Output power (%)		
Harmonic number	Limit %	100%	50%	10%
11 to 39 Odd only	3	less than 1	less than 1.5	maximum odd harmonic -11=2.52 remaining odd harmonics - less than 1.5

10.6 PFC startup phases

The following figures illustrate the startup signals generated by the PFC stages as different Vac input voltages are applied to the evaluation board.

The magenta lines represent the AC input line, the blue linse represent the PFC output voltage, while the green lines are the output current. The waveforms were captured with the DALI interface active.

The Iout startup time was defined by the DALI request and is between 550 ms and 650 ms.

Figure 33. PFC startup at 110 Vac

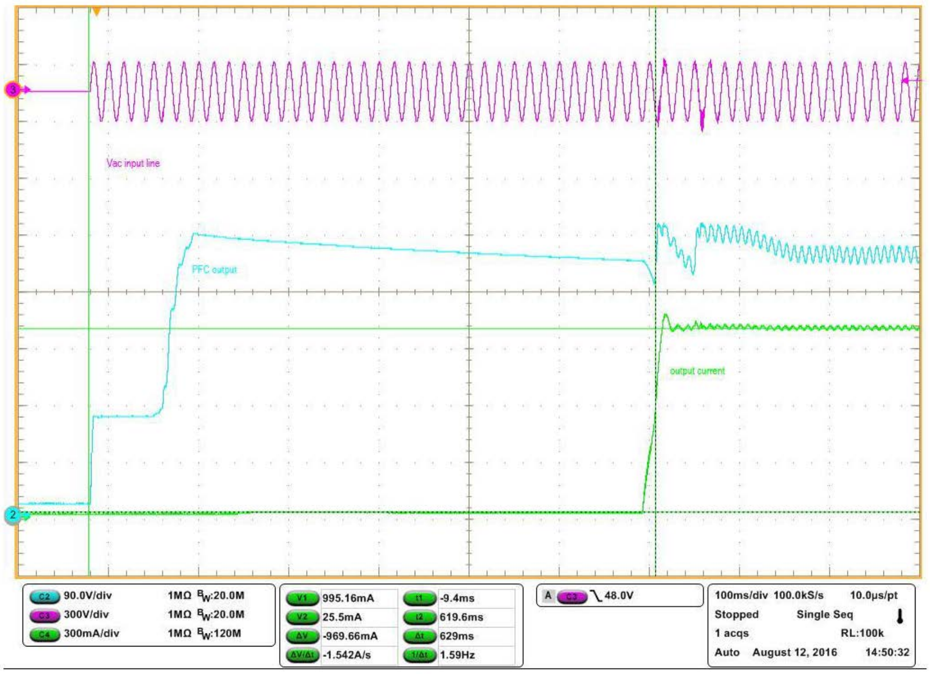
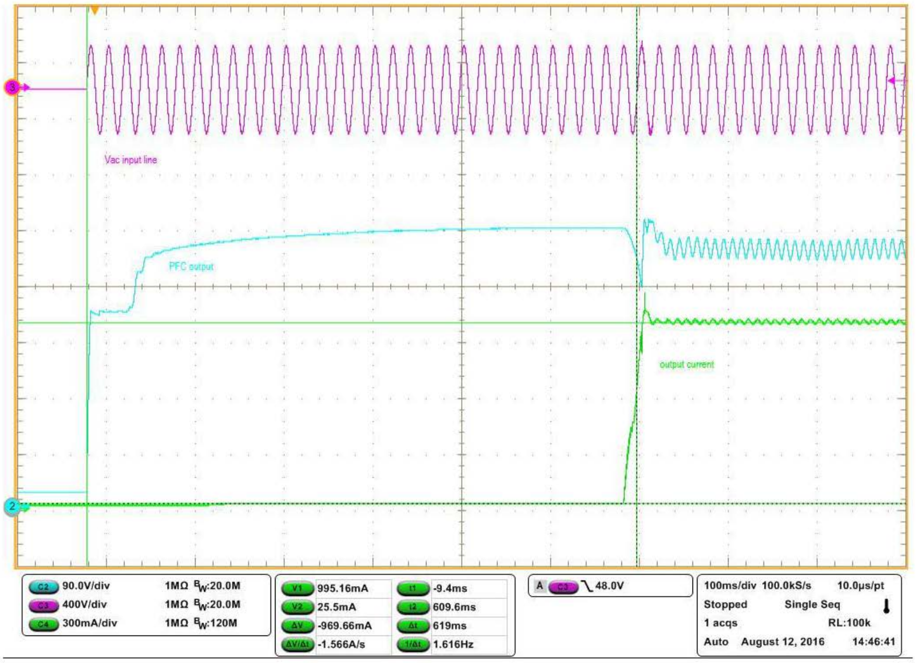


Figure 34. PFC startup at 220 Vac



10.7 Half bridge regulation

Figure 35. Half bridge - R36//R37 voltage (blue) - Detail - Iout = 1A and Figure 36. Half bridge - low side current – Iout = 600mA illustrate the sampling time during a 100 us cycles when Iout is 1 A and 600 mA respectively.

In Figure 35. Half bridge - R36//R37 voltage (blue) - Detail - Iout = 1A, Figure 36. Half bridge - low side current – Iout = 600mA and Figure 37. Half bridge - low side current – Iout = 200mA, the yellow lines represent the low side signal output from the STLUX and the blue lines represent the current on the HB shunt resistor (R36 and R27).

The HB acquisition point acquires the HB current when the CN_CNT signal triggers using the STLUX internal comparator. The ON time is smoothly incremented to compensate the delay on the external component (driver) and STLUX internal time (sampling time – 50 ns). After the acquisition point, the STLUX applies the acquired time, removing the external and internal delay.

Figure 35. **Half bridge - R36//R37 voltage (blue) - Detail - Iout = 1A**

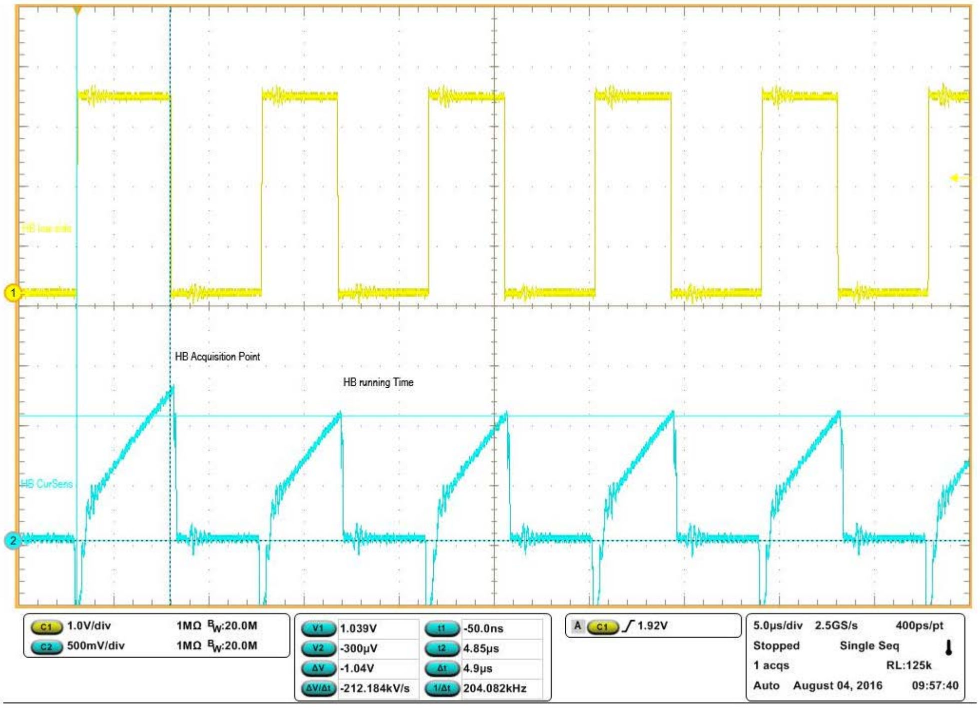


Figure 36. **Half bridge - low side current – Iout = 600mA**

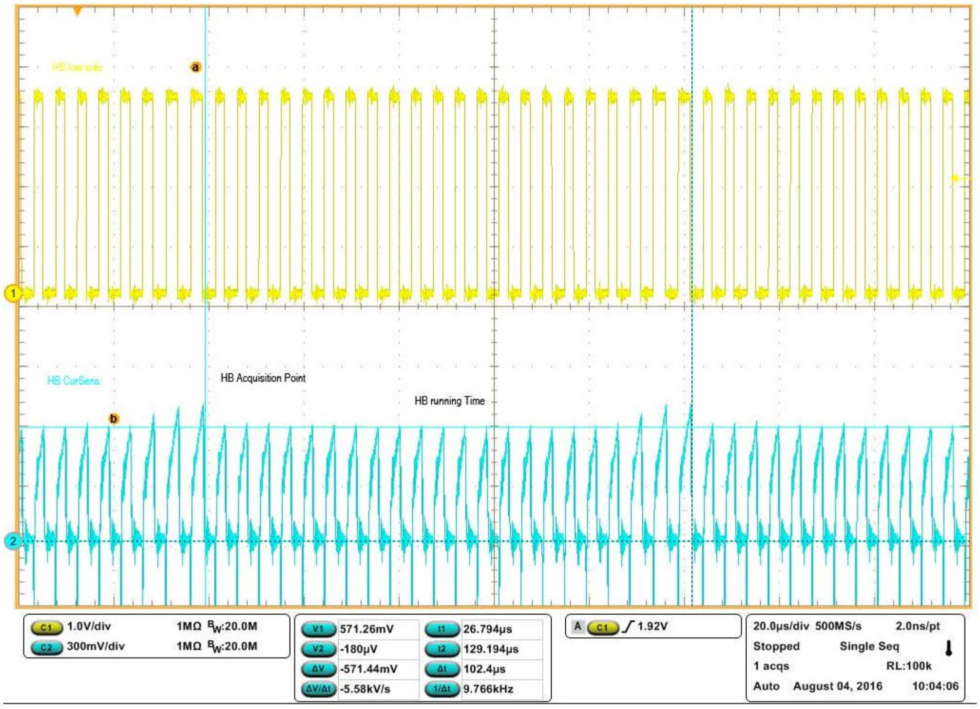
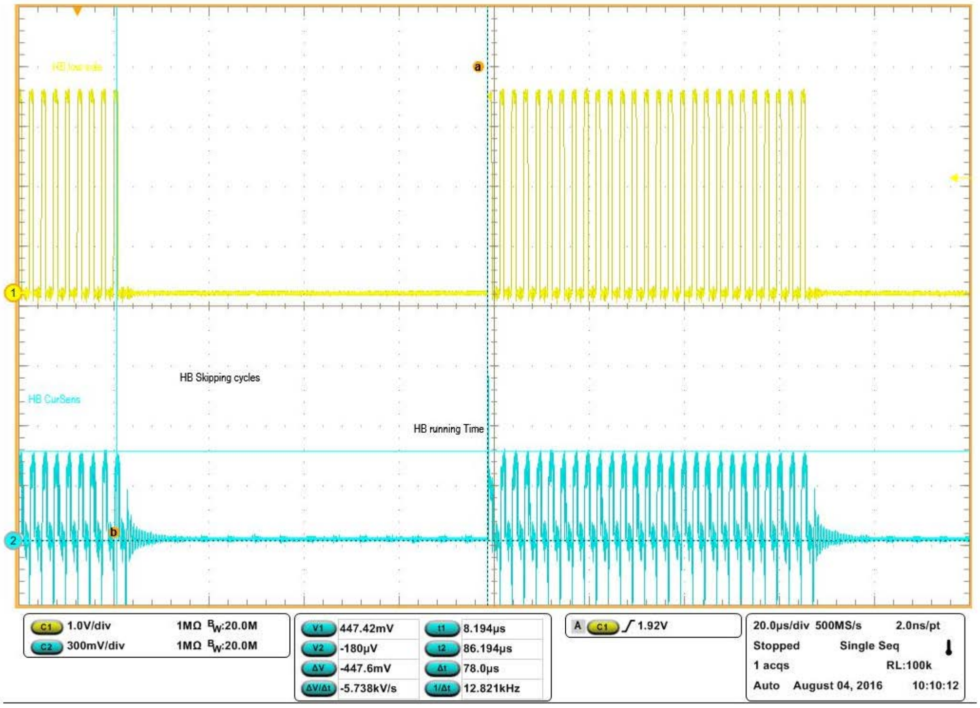


Figure 37. Half bridge - low side current – Iout = 200mA illustrates the implementation of US patent US20150003117A1. In this case the output current is 200 mA (not shown in figure).

Figure 37. **Half bridge - low side current – Iout = 200mA**



11 Firmware download procedure

Danger:

High voltage is present on the STEVAL-ILL066V2 evaluation board. Observe all relevant safety procedures before handling the board, even before initiating a firmware upgrade

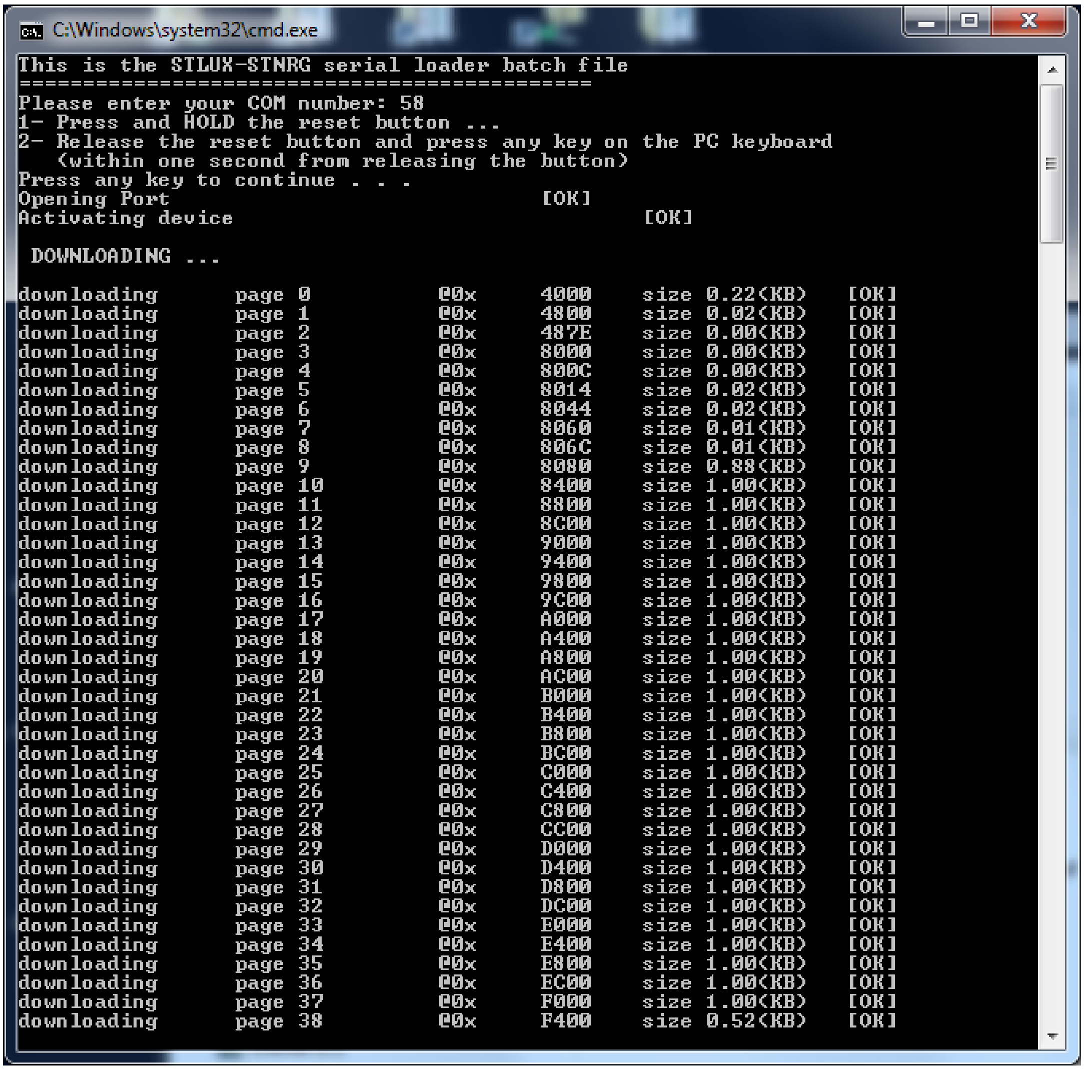
The zip file contains the programs used to download and the hex file to upload new FW to the STEVAL-ILL066V2 evaluation board. To install the firmware, extract the STSW-ILL066V2RxxB.zip (where "xx" is the release) file to a dedicated directory and perform the following steps:

1. Remove any AC power connections and set an external DC power generator to 12 Vdc.
2. Apply 12 Vdc between TP31 (positive) and TP25 (negative).
3. Using a USB-miniUSB cable, connect the PC to the evaluation board. The PC should start installing the appropriate driver (only the first time you connect a new board). If the automatic procedure cannot find the correct driver, contact your IT services.
4. Identify the COM line connected to the evaluation board see Section 11.1 Finding the COM line.
5. Using the GPGUI program, enable the serial download option by selecting “ILL066V2 board control”, then “Enable the serial loader” flag and then click the Push button.
6. Note: after this step, the evaluation board starts normal activity one second after power-on (or reset), which is not compliant with the DALI standard. After a correct download, the correct power on time is restored.
7. Close the GPGUI program.
8. Double click on “Program_UsingBL.bat”; a DOS shell will open.
9. Type the COM port number identified in step 4.
10. Push and hold the reset button on the evaluation board
11. Release the reset button and immediately type a character on the PC keyboard. These actions (release reset then type a character) must be completed in less than 1 second.
12. The download procedure will start automatically.

The result is shown in Figure 38. batch file output- download procedure. The word “OK” should appear to indicate successful completion of the download and verification procedure. At this point, the FW on the evaluation board is updated to the latest release. Type any character to close the batch window.

If there is an error during any of the initialization phases, a message will appear in the DOS window and the user should reset the device (step 9 in the above procedure). If the serial port number is invalid or busy, a different message appears and the batch file window is closed.

Figure 38. **batch file output- download procedure**



```
C:\Windows\system32\cmd.exe
This is the STLUX-STNRG serial loader batch file
================================================
Please enter your COM number: 58
1- Press and HOLD the reset button ...
2- Release the reset button and press any key on the PC keyboard
   (within one second from releasing the button)
Press any key to continue . . .
Opening Port                                    [OK]
Activating device                                       [OK]

 DOWNLOADING ...

downloading       page 0        @0x     4000    size 0.22(KB)   [OK]
downloading       page 1        @0x     4800    size 0.02(KB)   [OK]
downloading       page 2        @0x     487E    size 0.00(KB)   [OK]
downloading       page 3        @0x     8000    size 0.00(KB)   [OK]
downloading       page 4        @0x     800C    size 0.00(KB)   [OK]
downloading       page 5        @0x     8014    size 0.02(KB)   [OK]
downloading       page 6        @0x     8044    size 0.02(KB)   [OK]
downloading       page 7        @0x     8060    size 0.01(KB)   [OK]
downloading       page 8        @0x     806C    size 0.01(KB)   [OK]
downloading       page 9        @0x     8080    size 0.88(KB)   [OK]
downloading       page 10       @0x     8400    size 1.00(KB)   [OK]
downloading       page 11       @0x     8800    size 1.00(KB)   [OK]
downloading       page 12       @0x     8C00    size 1.00(KB)   [OK]
downloading       page 13       @0x     9000    size 1.00(KB)   [OK]
downloading       page 14       @0x     9400    size 1.00(KB)   [OK]
downloading       page 15       @0x     9800    size 1.00(KB)   [OK]
downloading       page 16       @0x     9C00    size 1.00(KB)   [OK]
downloading       page 17       @0x     A000    size 1.00(KB)   [OK]
downloading       page 18       @0x     A400    size 1.00(KB)   [OK]
downloading       page 19       @0x     A800    size 1.00(KB)   [OK]
downloading       page 20       @0x     AC00    size 1.00(KB)   [OK]
downloading       page 21       @0x     B000    size 1.00(KB)   [OK]
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downloading       page 30       @0x     D400    size 1.00(KB)   [OK]
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downloading       page 32       @0x     DC00    size 1.00(KB)   [OK]
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downloading       page 34       @0x     E400    size 1.00(KB)   [OK]
downloading       page 35       @0x     E800    size 1.00(KB)   [OK]
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```
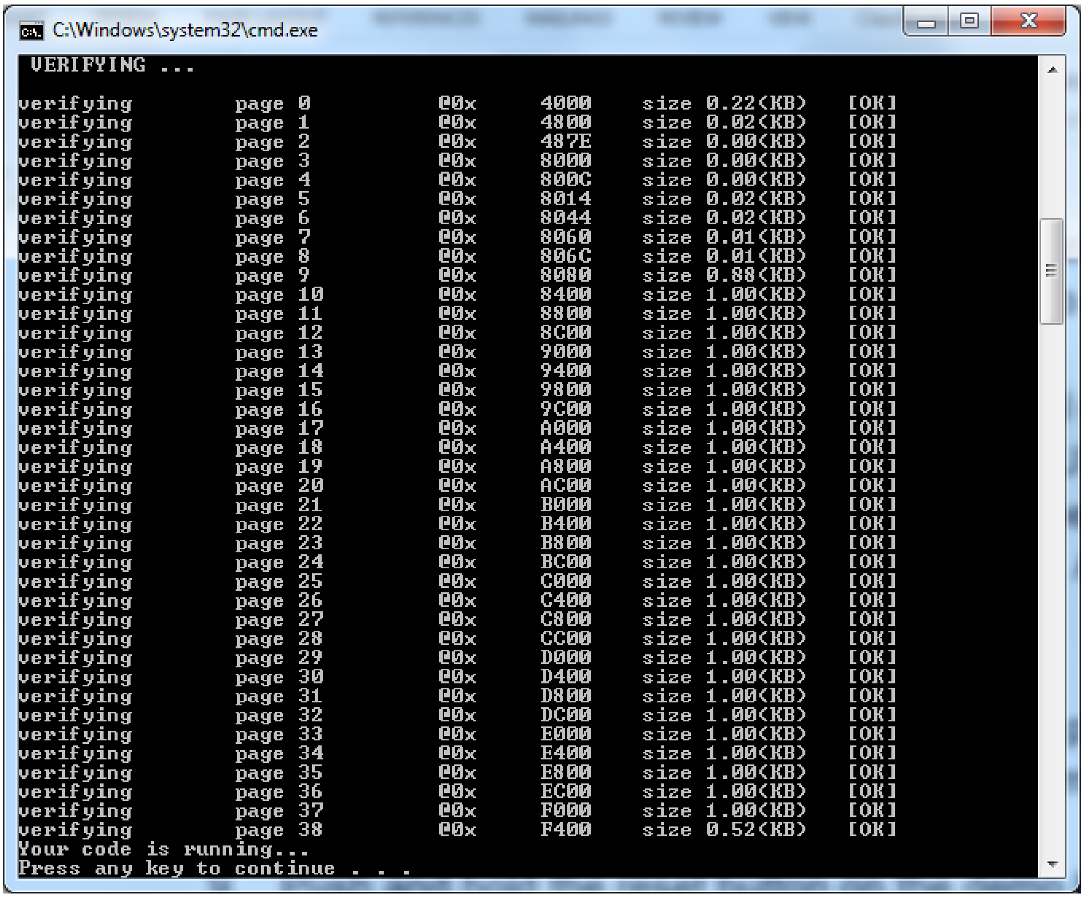

Figure 39. **batch file output- verification procedure**



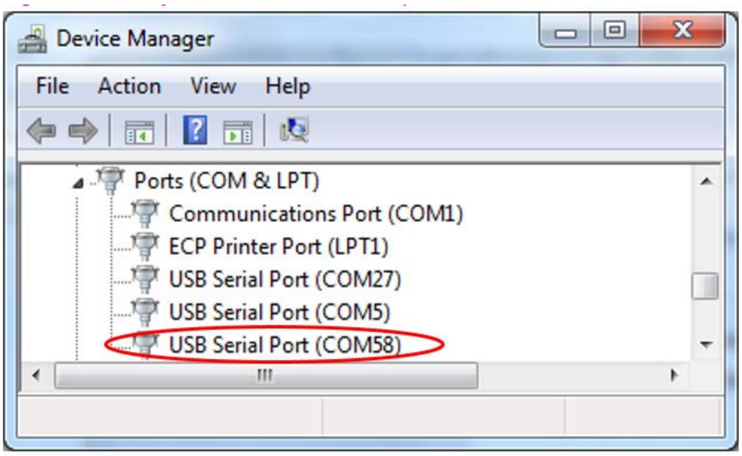
11.1 Finding the COM line

To connect the GPGUI with the evaluation board, it is necessary to determine the correct serial line. To find it, open the Control Panel→System→Device Manager→Ports and identify the new serial port that appears when the USB cable is connected to the evaluation board.

If there is more than one serial line connected on the PC, disconnect and reconnect the USB cable to determine the correct COM number (it will disappear and reappear).

In this example the correct serial line is COM58.

Figure 40. **Identify the correct serial COM port**



Revision history

Table 21. **Document revision history**

Date	Version	Changes
15-May-2014	1	Initial release.
04-Dec-2014	2	Updated: - Figure 13 on page 27 and Figure 14 on page 28 - Part number items 83 and 84 Table 5 on page 33.
08-Aug-2017	3	Throughout document: - replaced hardware information relating to STEVAL-ILL066V1 with STEVAL-ILL066V2 evaluation board - replaced firmware information relating to STEVAL-ILL066V1 with STEVAL-ILL066V2 firmware - updated content to reflect inclusion of GPGUI graphical user interface - text and formatting changes Added Figure 7: "PFC PI FW implementation" Added Section 9.2: "DALI implementation" Replaced Section 9.3: "Serial command" with Section 9.3: "GPGUI interface on STEVAL-ILL066V2 evaluation board" Updated Section 9.4: "Error codes" Added Figure 25: "Output current precision when Iout vs Vout compensation is not active" Added Figure 27: "Iout falling and rising time without DALI fading" Removed Figure 24: "Standby power vs AC input voltage" Added Figure 31: "Input current at 220ac with THD optimizer disabled", Figure 32: "Input current at 220Vac with THD optimizer enabled" and Table 20: "THD harmonic detail for different loads" Added Section 10.7: "Half bridge regulation" Replaced all content in Section 11: "Firmware download procedure"
27-Mar-2018	4	Updated Section 7 Bill of materials.

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