AN4022
Application note

TVS short pulse dynamic resistance measurement and correlation with TVS clamping voltage during ESD

Introduction

This application note is addressed to technical engineers and designers to explain how STMicroelectronics measure and specify dynamic resistance R_D in protection devices.

This parameter can be conveniently and accurately used to calculate the remaining voltage after a transient voltage suppressor or a filter including protection, especially for devices dedicated to protect against very fast transient surges such as ESD.

Market environment

Mobile phones, computers and their peripherals are sensitive electronic products. Each of these products has to be protected against electrostatic discharge using components able to clamp the high voltages generated in transients defined by each standard level such as IEC 61000-4-2. Knowing the clamping voltage level of transient voltage suppressors is a key point in the protection definition during the circuit design to get reliable and robust products.

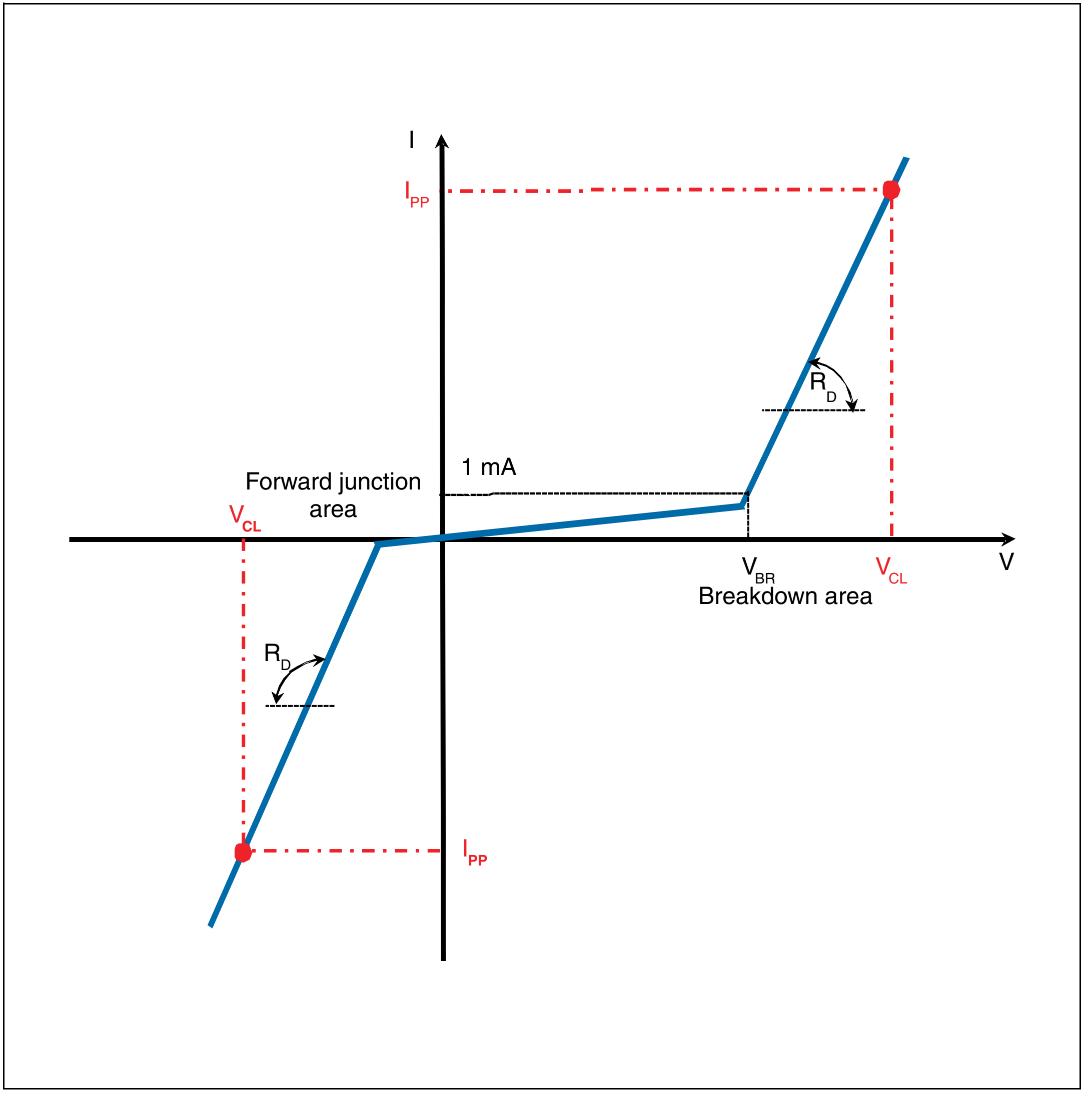
This application note describes

- The clamping characteristic
- Dynamic resistance and how to measure it
- Predicted results versus measured results
- TLP measurements

1 Clamping characteristic

The remaining voltage across a TVS device is linked to its clamping characteristic. *Figure 1* shows the voltage across a unidirectional device versus the current flowing through it.

Figure 1. Typical clamping characteristic of a unidirectional device



For a positive surge (*Figure 2*) the maximum voltage at the IC input is the clamping voltage V_{CL}, directly linked to the V_{BR} value of the device, and its dynamic resistance R_D. For a negative surge (*Figure 3*) this remaining voltage is linked to its forward characteristic and its dynamic resistance R_D.

Figure 2. Typical protection circuit, positive surge

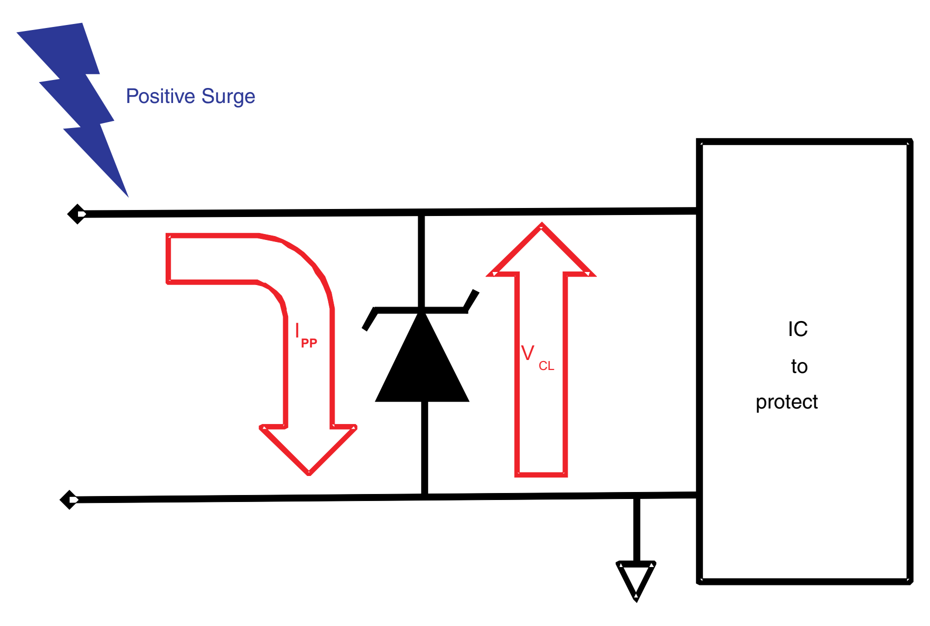
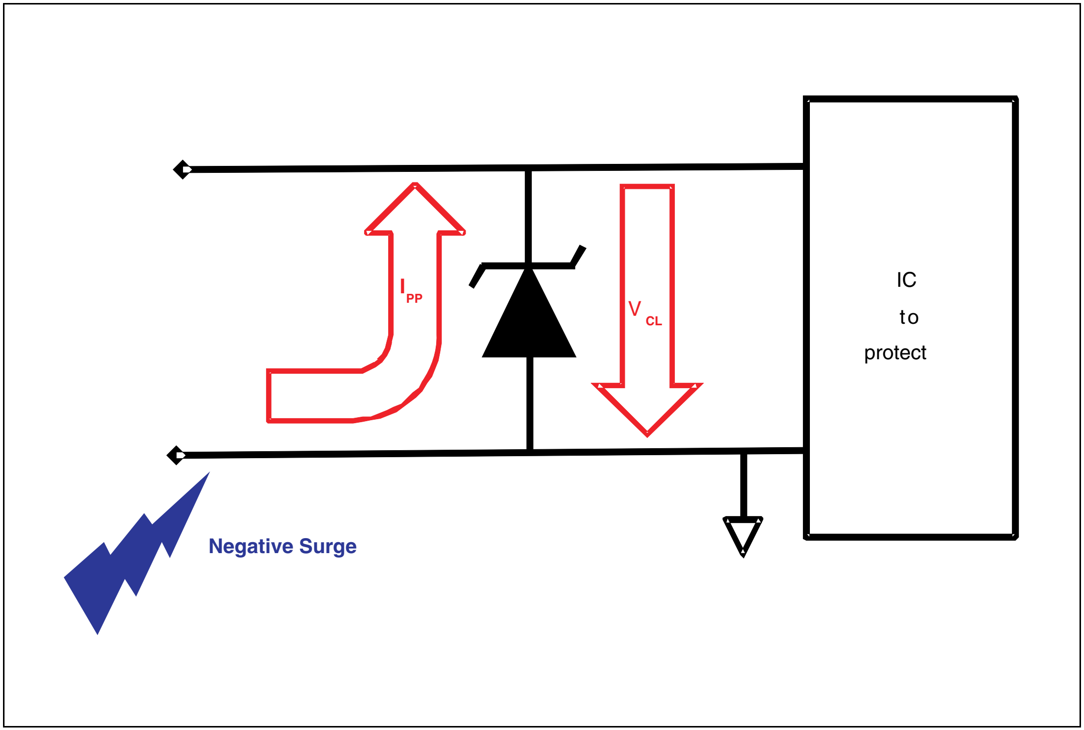
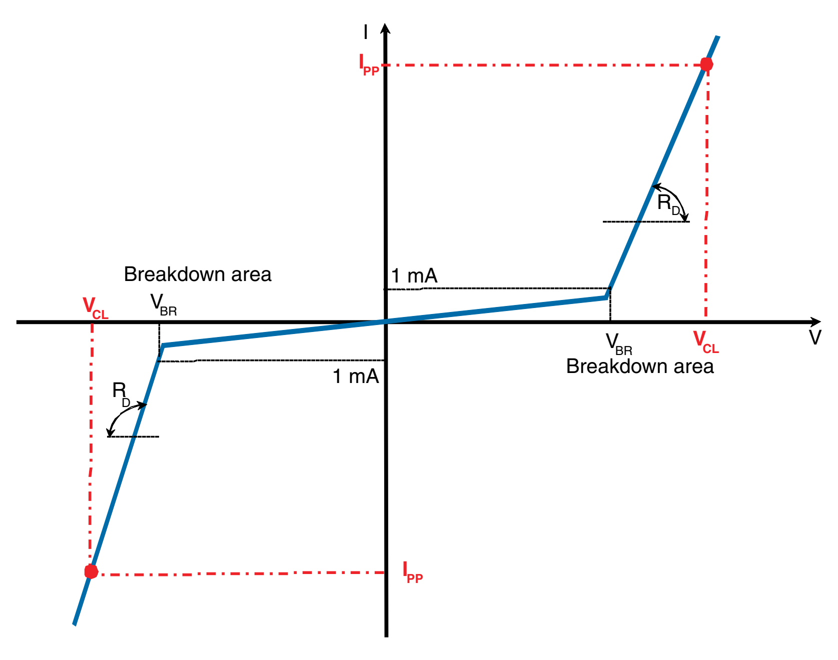


Figure 3. Typical protection circuit, negative surge



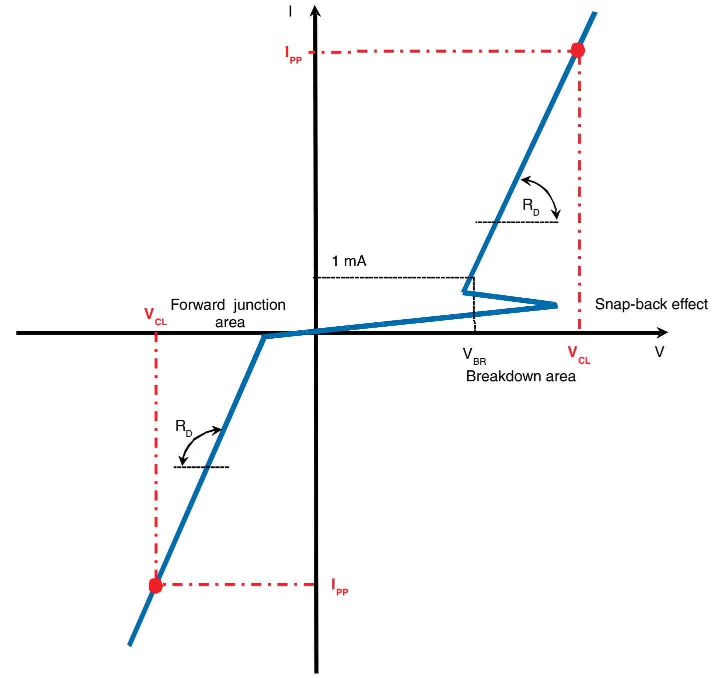
The clamping characteristic of a bidirectional TVS is shown in *Figure 4*.

Figure 4. Typical clamping characteristic bidirectional device



Some TVS devices have a breakdown characteristic with a “snap-back” effect, allowing a lower V_{BR} value in one or both polarities, or a mix of the two characteristics (*Figure 5*).

Figure 5. Typical clamping characteristic of a “snap-back” TVS



2 Dynamic resistance and how to measure it

In the previous section it was shown that the remaining voltage across a circuit to protect is closely linked to the V_{BR} of the protection device used and to its dynamic resistance R_D. The first parameter is generally well known and specified. In the past dynamic resistance has been specified but with test conditions different from real surge conditions giving pessimistic results, especially for short surges like electrostatic discharges. The pulse used had a duration of 2.5 µs.

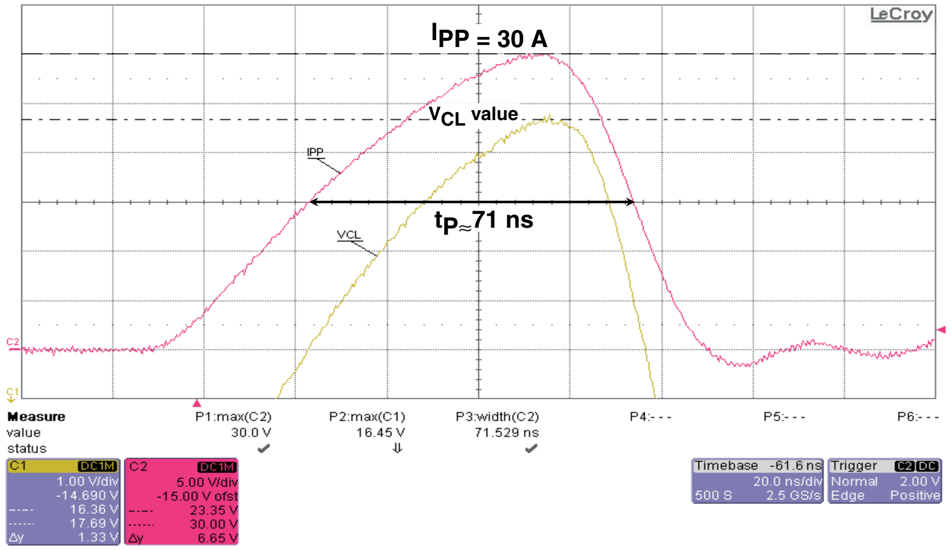
To be closer to typical ESD (defined in IEC61000-4-2), a 100 ns pulse width has been chosen.

An accurate voltage measurement is quite difficult during high rate of rise current, due to the voltage probing loop inductance, inducing parasitic voltage:

$$V_{PARASITIC} = L_{PARASITIC} \times dI/dt$$

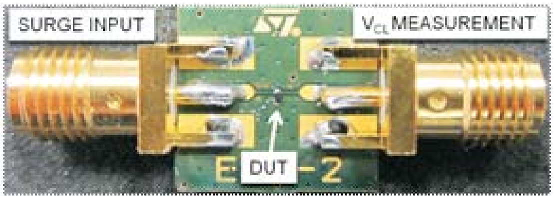
So a triangular pulse is used This is shown in *Figure 6*. No oscillations disturb the measurement.

Figure 6. Current and voltage waveforms for R_D measurement



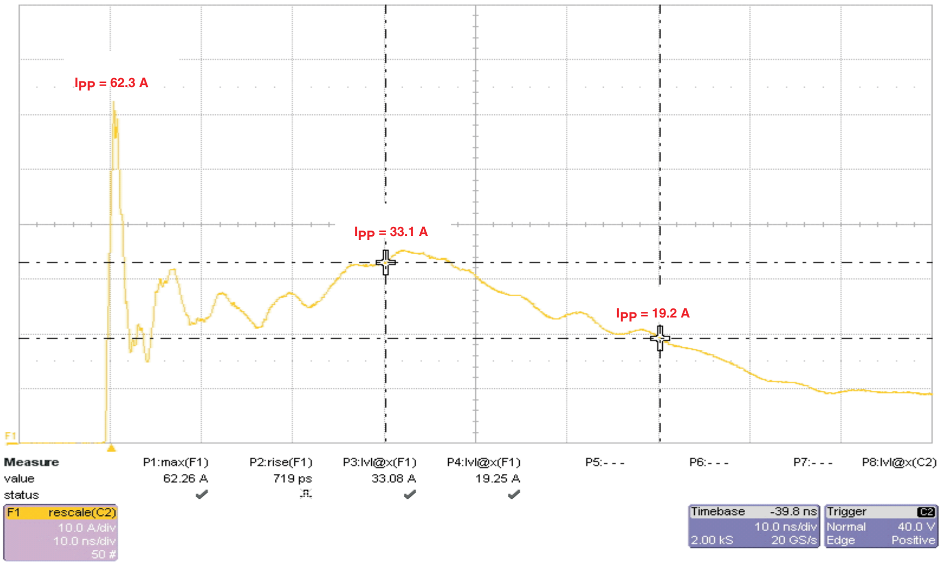
The current is measured during the test by a current monitor (Pearson Electronics). The voltage measurement is by the “Kelvin” method in coaxial configuration in order to get best accuracy (test board shown in *Figure 7*). An adequate voltage range and offset is set on the oscilloscope to get the best dynamic measurement without amplifier saturation.

Figure 7. Test board



The circuit can drive current from 500 mA up to 50 A, allowing measurements beyond the IEC61000-4-2 standard highest level. In fact, at V_{PP} = 15 kV contact, the current through the device under test is 20 A to 62 A, between the first spike up to 60 ns. (*Figure 8*)

Figure 8. IEC61000-4-2 waveform, current level at V_{PP} = 15 kV (contact discharge)



Measure	P1:max(F1)	P2:rise(F1)	P3:lvl@x(F1)	P4:lvl@x(F1)	P5:- - -	P6:- - -	P7:- - -	P8:lvl@x(C2)
value	62.26 A	719 ps	33.08 A	19.25 A				
status	✓		✓	✓				

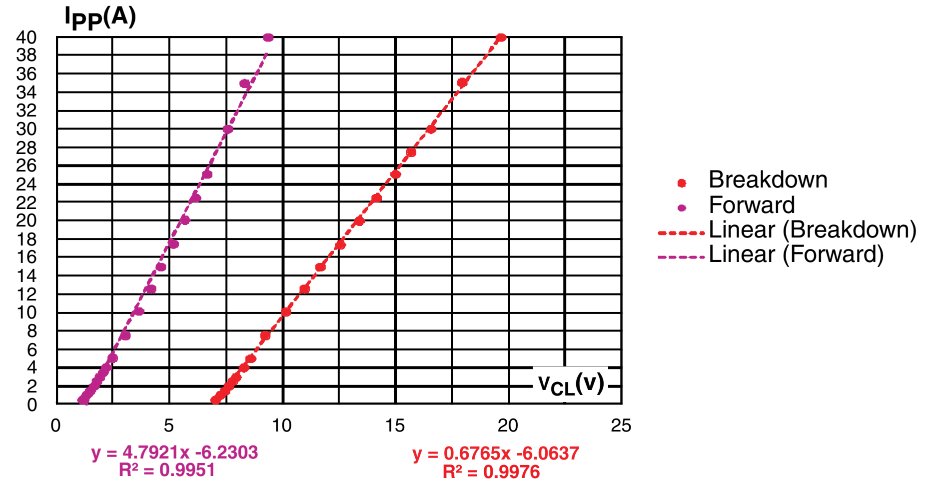
F1 rescale(C2)
10.0 A/div
10.0 ns/div
50 #

Timebase -39.8 ns
10.0 ns/div
2.00 kS 20 GS/s

Trigger C2
Normal 40.0 V
Edge Positive

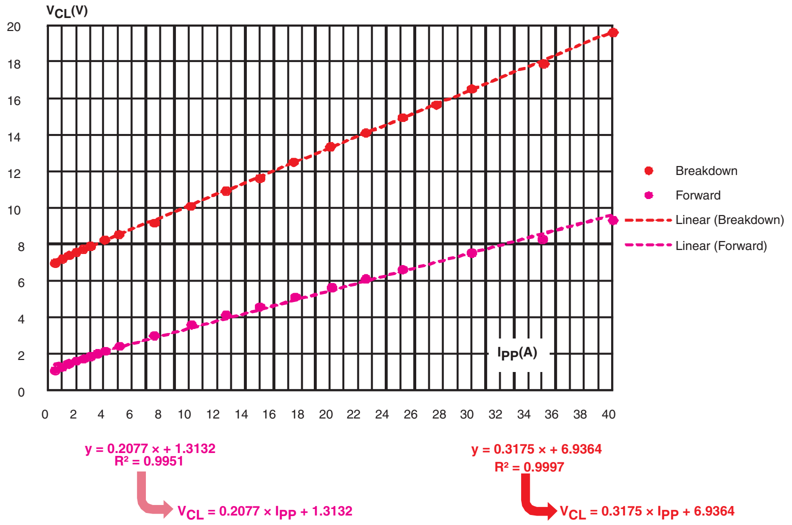
To get the dynamic clamping characteristic of the device from 0 to I_{PP} max, the current is increase step by step, and at each level, the voltage is measured. Typical results up to I_{PP} = 40 A are shown in *Figure 9*. In this example, the device is an ESDA6V1P6.

Figure 9. Dynamic clamping characteristic (unidirectional TVS)



The characteristic is linear in the interesting area and a good trend line can be extracted ($R^2 = 0.99$). A better representation can be obtained as in *Figure 10*, in order to calculate directly the clamping voltage for a known I_{PP}.

Figure 10. Clamping voltage V_{CL} versus peak pulse current I_{PP}



3 Predicted results versus measured results

With this information, we can now estimate the residual voltages remaining after the protection device and compare these results with the results obtained during ESD surge measurements. For this comparison the IEC61000-4-2 in contact mode has been selected. In the standard, the current levels are specified versus the charging voltage (*Figure 11*).

Figure 11. Extract of IEC61000-4-2 standard [page 12], current levels versus charge voltage levels [a]

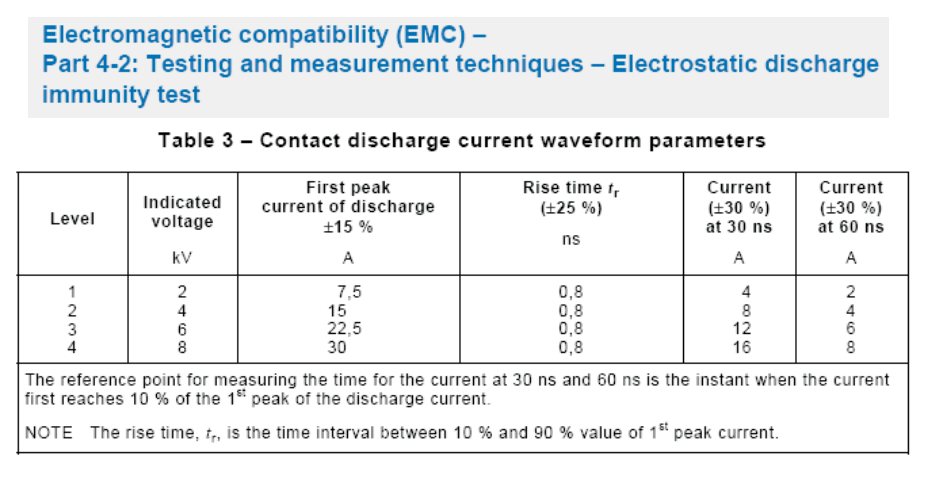


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Table 3 – Contact discharge current waveform parameters

Level	Indicated voltage kV	First peak current of discharge ±15 % A	Rise time t_r (±25 %) ns	Current (±30 %) at 30 ns A	Current (±30 %) at 60 ns A
1	2	7,5	0,8	4	2
2	4	15	0,8	8	4
3	6	22,5	0,8	12	6
4	8	30	0,8	16	8

The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10 % of the 1st peak of the discharge current.

NOTE The rise time, t_r, is the time interval between 10 % and 90 % value of 1st peak current.

From this table we can calculate the minimum and maximum current values that can be found in our circuit, based on the tolerances specified (±15% or ±30% versus typical values). The expected values are summarized in *Table 1*.

Table 1. Minimum, typical and maximum current values versus charge voltage

Level	V_{PP} (kV)	Peak current (±15%)			I_{PP}@ 30 ns (±30%)			I_{PP}@ 60 ns (±30%)		
1	2	6.37	7.5	8.62	2.8	4	5.2	1.4	2	2.6
2	4	12.75	15	17.25	5.6	8	10.4	2.8	4	5.2
3	6	19.12	22.5	25.87	8.4	12	15.6	4.2	6	7.8
4	8	25.5	30	34.5	11.2	16	20.8	5.6	8	10.4

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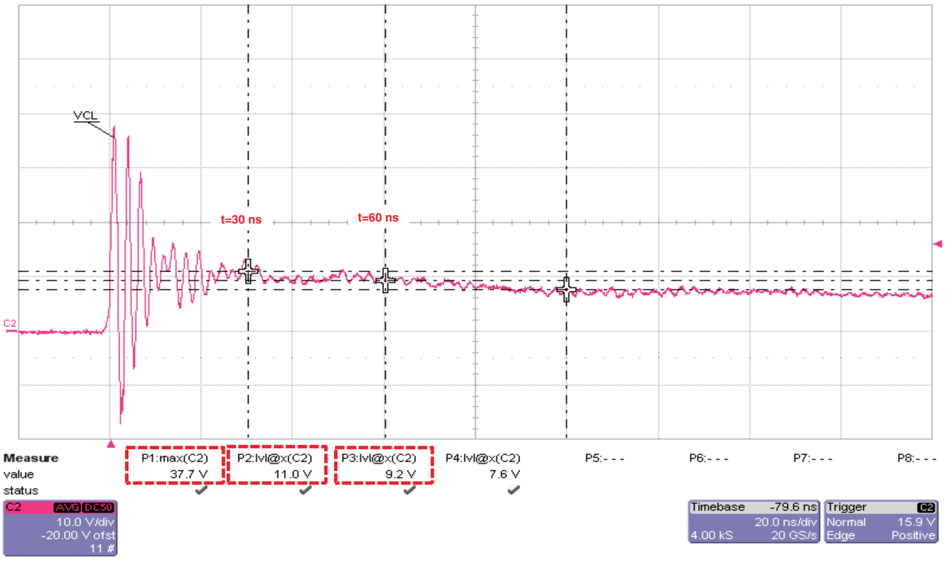
The device under test is measured in ESD clamping test at the different standard voltage levels, as in *Figure 12* (example at +8 kV). The test conditions used are described in the STMicroelectronics Application note AN3353, “IEC 61000-4-2 standard testing”.

Figure 12. Typical clamping voltage waveform with the measured values



We get from these waveforms three values: the peak clamping voltage (first spike) and the clamping voltages at t = 30 ns and t = 60 ns at peak charging voltage of ±2 kV, ±4 kV, ±6 kV and ±8 kV. The values at the add point ±15 kV was also obtained, even if this point is not specified in the standard.

We can now represent in three charts the predicted values and the real measurement results in order to compare them.

Figure 13. Measurements and predicted values for the first spike peak value

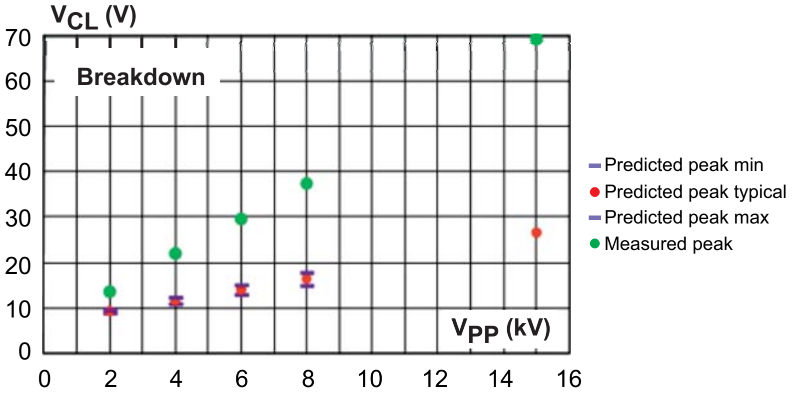


Figure 14. Measurements and predicted values for 30 ns clamping value

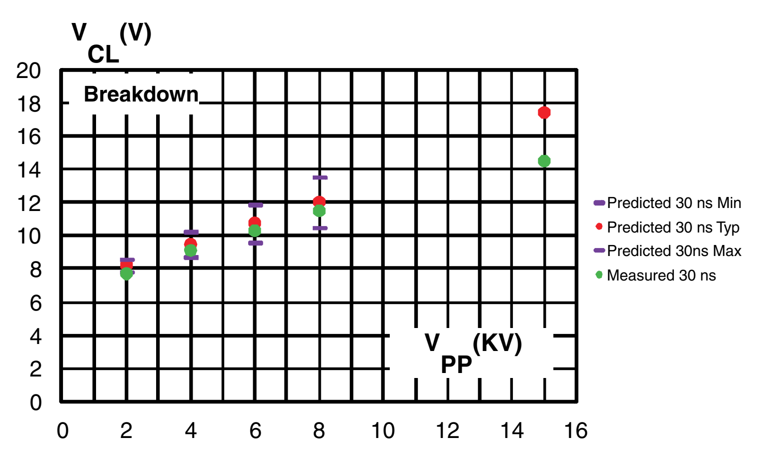


Figure 15. Measurements and predicted values for 60 ns clamping value

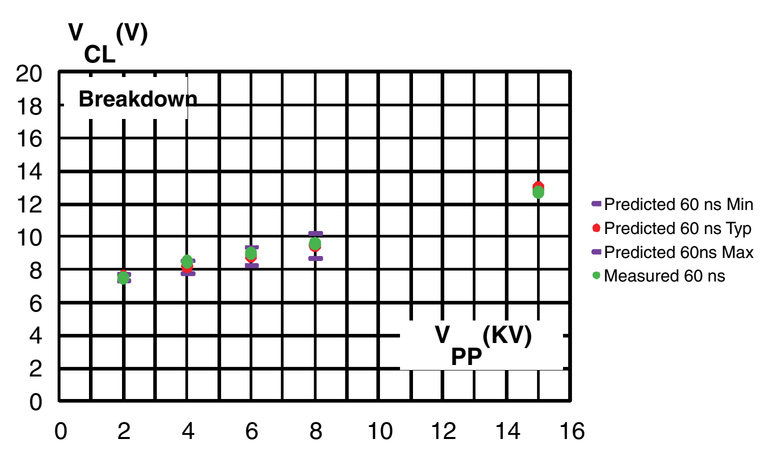


Figure 13 shows the predicted results for the first spike voltage are far from the measured values. In fact, the dI/dt during the first spike is very high, between 10 A/ns up to 80 A/ns (the current rise time is around 0.75 ns). If we represent the ΔV between the measured and the calculated $\frac{\Delta V}{dI/dt}$ values versus the dI/dt, we get the curve in *Figure 16*. From this curve, we can extract the value, shown in *Figure 17*. This value is near a constant, equal to the parasitic inductance of the measurement loop (board, ground etc), in this case around 0.5 nH.

Figure 16. Gap between measured and calculated values versus current rate of rise

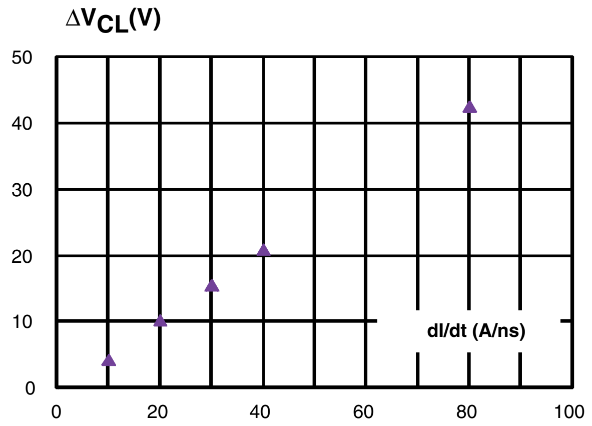
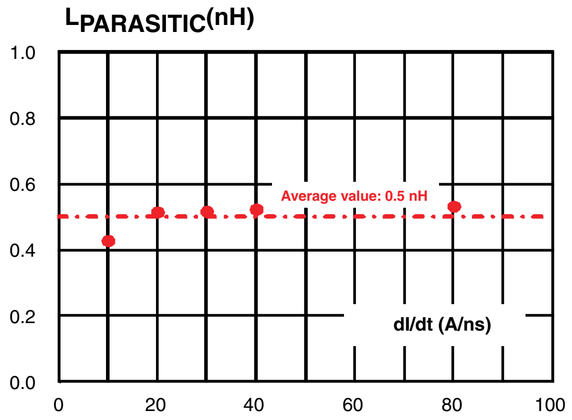


Figure 17. Parasitic inductance



There are three considerations regarding the first spike:

- This calculation of the V_{CL} for this first spike is not correct for a bidirectional device or a rail to rail plus Transil™ device (USBULC6-2F3 for example), because in this case, a parameter called V_{FP} linked to one of the junctions in forward conduction induces another added spike voltage. This V_{FP} depends on the diode technology and cannot be easily evaluated.
- We see here the importance of the parasitic inductances especially the ground inductance return pass. The lower the value of this inductance, the lower the value of this transient voltage.
- This spike is not the most critical for the device to protect against because I/O's IC circuits are dimensioned to withstand short pulses with these levels, similar to machine model ESD tests, for example.

From *Figure 14* and *Figure 15* we see the predicted values for the clamping voltages at 30 ns and 60 ns are very close to the measured results, assuming the dynamic characteristic measured in these conditions are consistent, even at high current and voltage levels.

Note: *The study in forward polarity gives the same kind of results.*

4 TLP measurements

A commonly used method to probe the dynamic characteristic of a TVS is the TLP (transmission line pulse). This uses square pulses with a duration between 75 ns to 200 ns with fast rise times of few nanoseconds. The equipment required is specific and expensive and is dedicated to the characterization of the ESD robustness of protection devices, especially for integrated circuit I/O's. The equipment is usually limited to 10 A in maximum current level (sometimes 20 A).

It is interesting to compare the results obtained by our method and the TLP method.

In *Figure 18* and *Figure 19*, TLP measurements have been made on an ESDAULC6-1U2 up to 10 A, on the breakdown and forward area. The characteristics obtained by the triangular pulse are superimposed in green. There is little difference between the two results.

Figure 18. TLP measurements compared with triangular waveform (breakdown polarity)

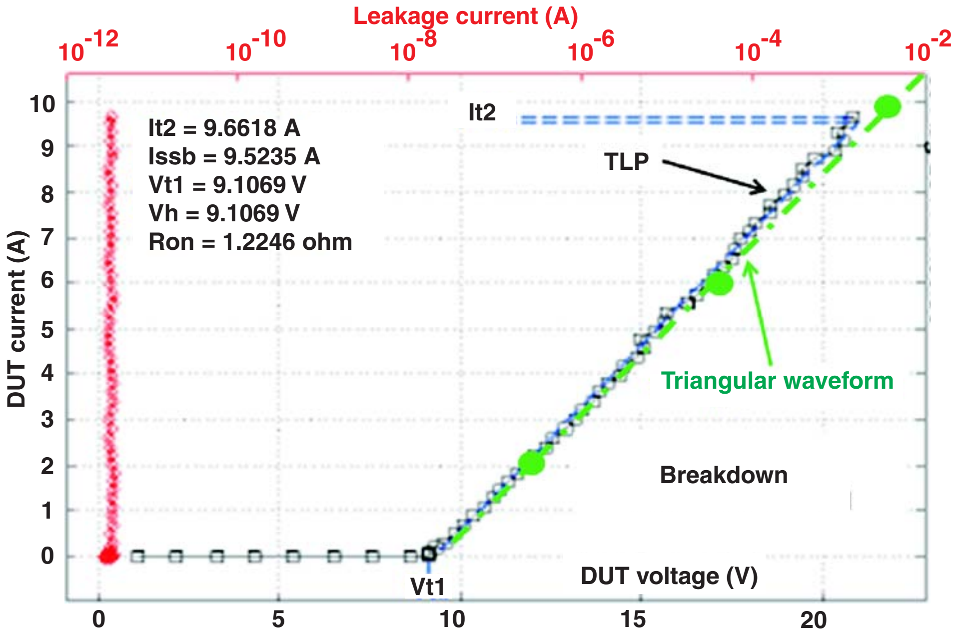
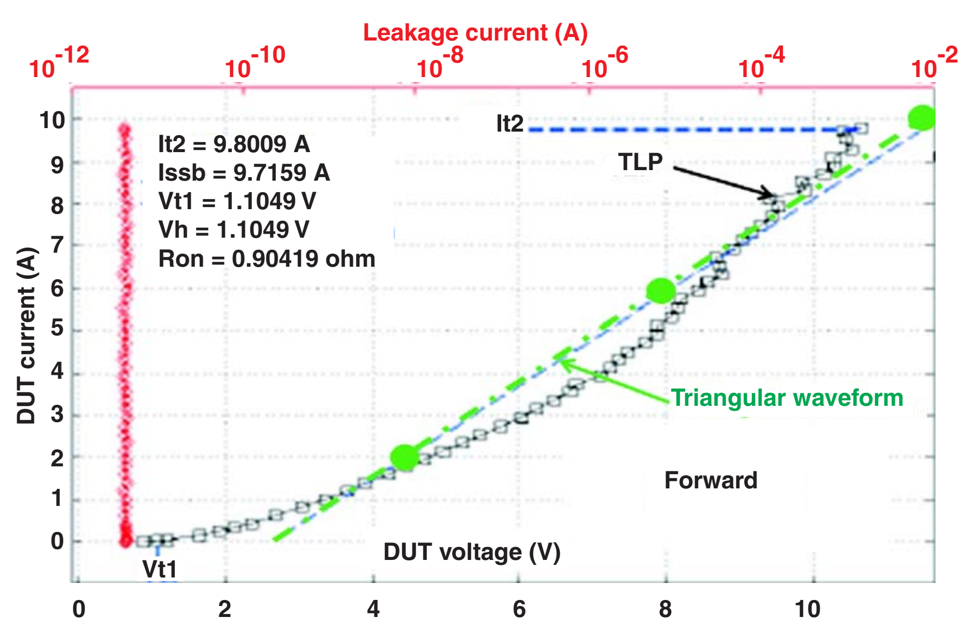


Figure 19. TLP measurements comparison with triangular waveform (forward polarity)



Conclusion

To be sure a circuit design will be robust against electrostatic discharges, it is important to anticipate the maximum voltage that can appear at the I/O’s of the sensitive circuits. Knowing the dynamic characteristic of a transient voltage suppressor used for their protection is a key point during the design.

We have shown in this note that this dynamic characteristic, measured with a short pulse, not necessarily TLP, allows accurate prediction of the remaining voltage across the TVS, especially after the first spike of a standard surge such as that defined in IEC61000-4-2, where the circuit to protect is the most sensitive.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
20-Sep-2012	1	Initial release.
30-Oct-2013	2	Updated *Figure 13*.

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