AN4946
Application note

Migration of microcontroller applications between STM32F72xxx/F73xxx and STM32F74xxx/F75xxx microcontrollers

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require to switch to smaller components and shrink the PCB area.

This application note groups all the information needed to help the user when migrating between an STM32F72xxx/F73xxx and STM32F74xxx/F75xxx device based design.

This application note provides a guideline on the hardware migration and the peripheral migration.

To fully benefit from the information inside this application note, the user should be familiar with the STM32F72xxx/F73xxx and STM32F74xxx/F75xxx microcontrollers.

For additional information, refer to the following documents available on *www.st.com*:

- *STM32F75xxx and STM32F74xxx advanced ARM®-based 32-bit MCUs* reference manual (RM0385)
- *STM32F72xxx and STM32F73xxx advanced ARM®-based 32-bit MCUs* reference manual *(RM0431)*
- *STM32F74xxx/F75xxx datasheets*
- *STM32F72xxx/F73xxx* datasheets

Table 1. Applicable products

Type	Reference	Product lines and part numbers
Microcontrollers	STM32F72xxx/F73xxx	STM32F7x2 line, STM32F7x3 line
	STM32F74xxx/F75xxx	STM32F745IE, STM32F745IG, STM32F745VE, STM32F745VG, STM32F745ZE, STM32F745ZG, STM32F7x6 line

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1 Hardware migration

1.1 Available packages

Table 2 summarizes the different packages available on each device

Table 2. Package summary (1)

Package	STM32F7x2xx	STM32F7x3xx	STM32F74xxx/F75xxx
LQFP64	X	-	-
LQFP100	X	-	X
LQFP144	X	X	X
LQFP176	X	X	X
LQFP208	-	-	X
TFBGA100	-	-	X
UFBGA144	-	X	-
UFBGA176	X	X	X
TFBGA216	-	-	X
WLCSP100	-	X	-
WLCSP143	-	-	X

1. X = available, "-" = not available.

1.2 Pinout compatibility

The STM32F74xxx/F75xxx devices are fully pin-to-pin compatible with the STM32F7x2xx devices.

Whereas, the STM32F7x3xx devices present an incompatibility due to the embedded USB OTG PHY high speed.

1.2.1 LQFP144 package

Figure 1 and *Table 3* show the LQFP144 pinout differences between the STM32F74xxx/F75xxx/F7x2xx and the STM32F7x3xx devices.

Figure 1. STM32F74xxx/F75xxx/F7x2xx versus STM32F7x3xx LQFP144 pinout

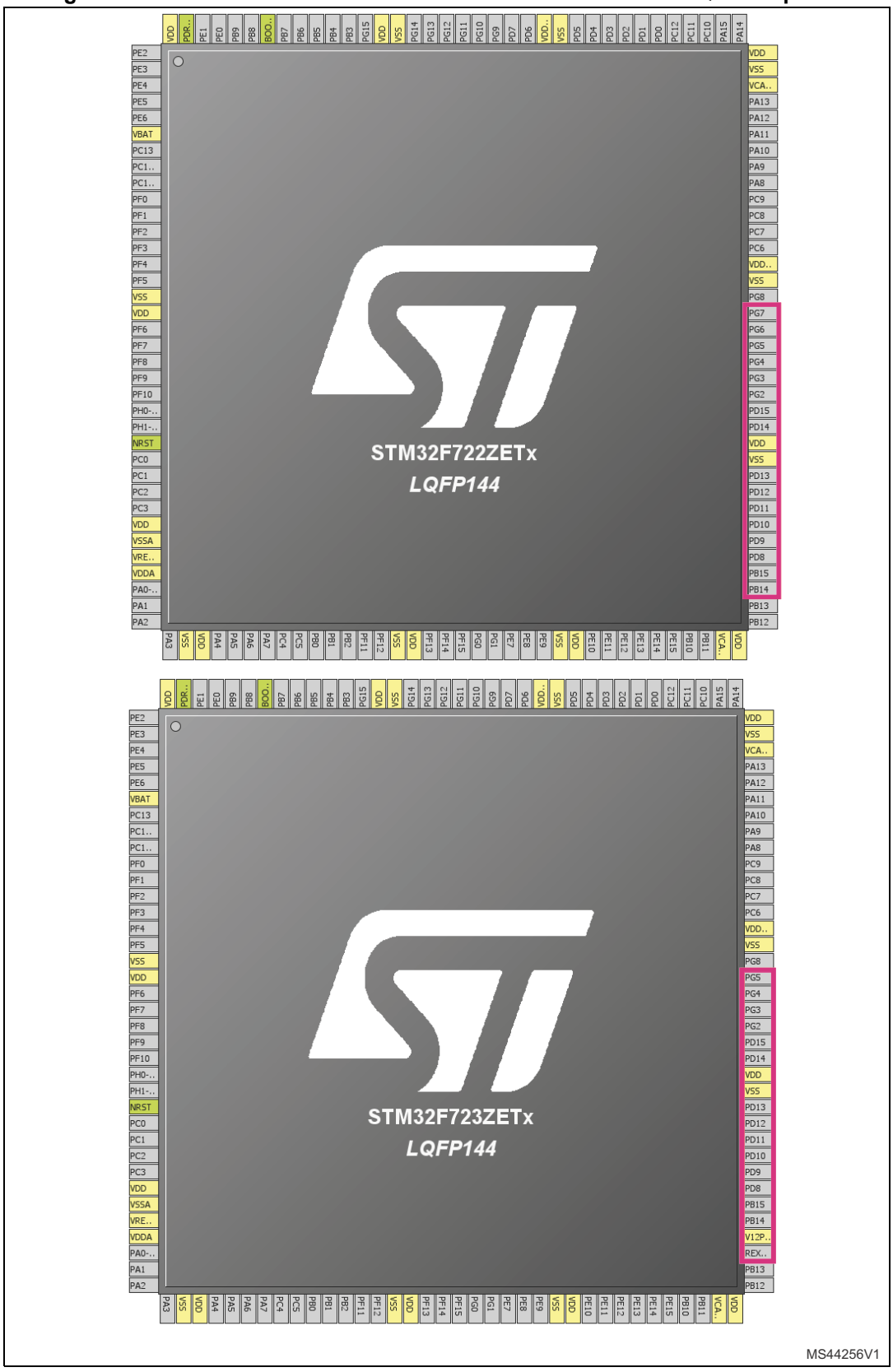


Table 3. LQFP144 pinout differences

Pin number	STM32F74xxx/F75xxx/F7x2xx	STM32F7x3xx
92	PG7(1)	PG5
91	PG6(1)	PG4
90	PG5	PG3
89	PG4	PG2
88	PG3	PD15
87	PG2	PD14
86	PD15	VDD
85	PD14	VSS
84	VDD	PD13
83	VSS	PD12
82	PD13	PD11
81	PD12	PD10
80	PD11	PD9
79	PD10	PD8
78	PD9	PB15
77	PD8	PB14
76	PB15	VDD12OTGHS
75	PB14	OTG_HS_REXT

1. PG6 and PG7 are removed in the STM32F7x3xx devices.

1.2.2 LQFP176 package

Figure 2 and *Table 4* show the LQFP176 pinout differences between the STM32F74xxx/F75xxx/F7x2xx and the STM32F7x3xx devices.

Figure 2. STM32F74xxx/F75xxx/F7x2xx versus STM32F7x3xx LQFP176 pinout

Table 4. LQFP176 pinout differences

Pin number	STM32F74xxx/F75xxx/F7x2xx	STM32F7x3xx
111	PG7(1)	PG5
110	PG6(1)	PG4
109	PG5	PG3
108	PG4	PG2
107	PG3	PD15
106	PG2	PD14
105	PD15	VDD
104	PD14	VSS
103	VDD	PD13
102	VSS	PD12
101	PD13	PD11
100	PD12	PD10
99	PD11	PD9
98	PD10	PD8
97	PD9	PB15
96	PD8	PB14
95	PB15	VDD12OTGHS
94	PB14	OTG_HS_REXT

1. PG6 and PG7 are removed in the STM32F7x3xx devices.

1.2.3 UFBGA176 package

Figure 3 and *Table 5* show the UFBGA176 ballout differences between the STM32F74xxx/F75xxx/F7x2xx and the STM32F7x3xx devices.

Figure 3. STM32F74xxx/F75xxx/F7x2xx versus STM32F7x3xx UFBGA176 pinout

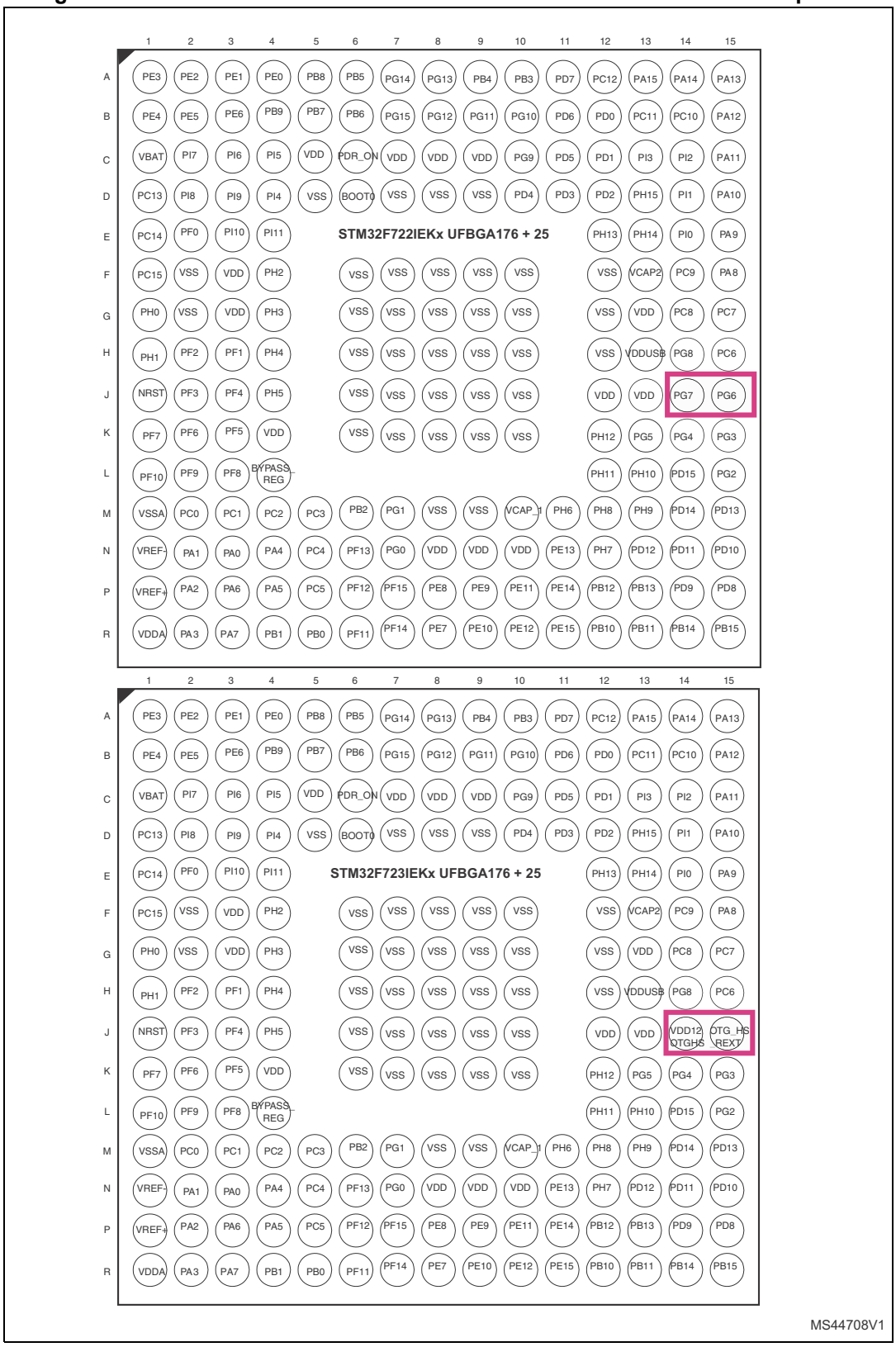


Table 5. UFBGA176 pinout differences

Pin number	STM32F74xxx/F75xxx/F7x2xx	STM32F7x3xx
J15	PG6	OTG_HS_REXT
J14	PG7	VDD12OTGHS

1.3 Bootloader interface summary

The system bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 6 shows the supported communication peripherals by the system bootloader.

Table 6. STM32F74xxx/F75xxx and STM32F72xxx/F73xxx bootloader communication peripherals

System bootloader peripherals	STM32F74xxx/F75xxx	STM32F72xxx/F73xxx
	Available on	
USB OTG FS in device mode	PA11/PA12	
USART1	PA9/PA10	
USART3	PA10/PA11 and PC10/PC11	
CAN1	-	PB8/PB9
CAN2	PB5/PB13	-
I2C1	PB6/PB9	
I2C2	PF0/PF1	
I2C3	PA8/PC9	
SPI1	PA4/PA5/PA6/PA7	
SPI2	PI0/PI1/PI2/PI3	
SPI4	PE11/PE12/PE13/PE14	

2 System architecture

The main differences between the STM32F74xxx/F75xxx and STM32F72xxx/F73xxx system architectures are highlighted in pink on *Figure 4* and *Figure 5*.

Figure 4. STM32F72xxx/F73xxx system architecture differences

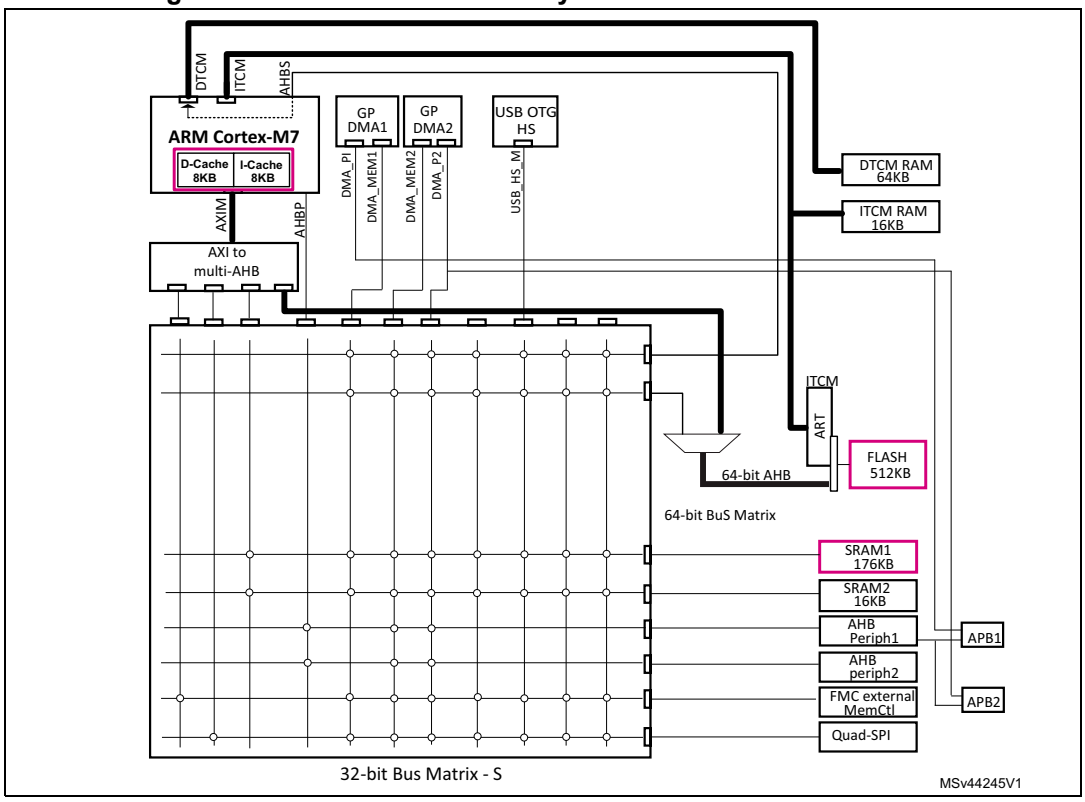


Figure 5. STM32F74xxx/F75xxx system architecture differences

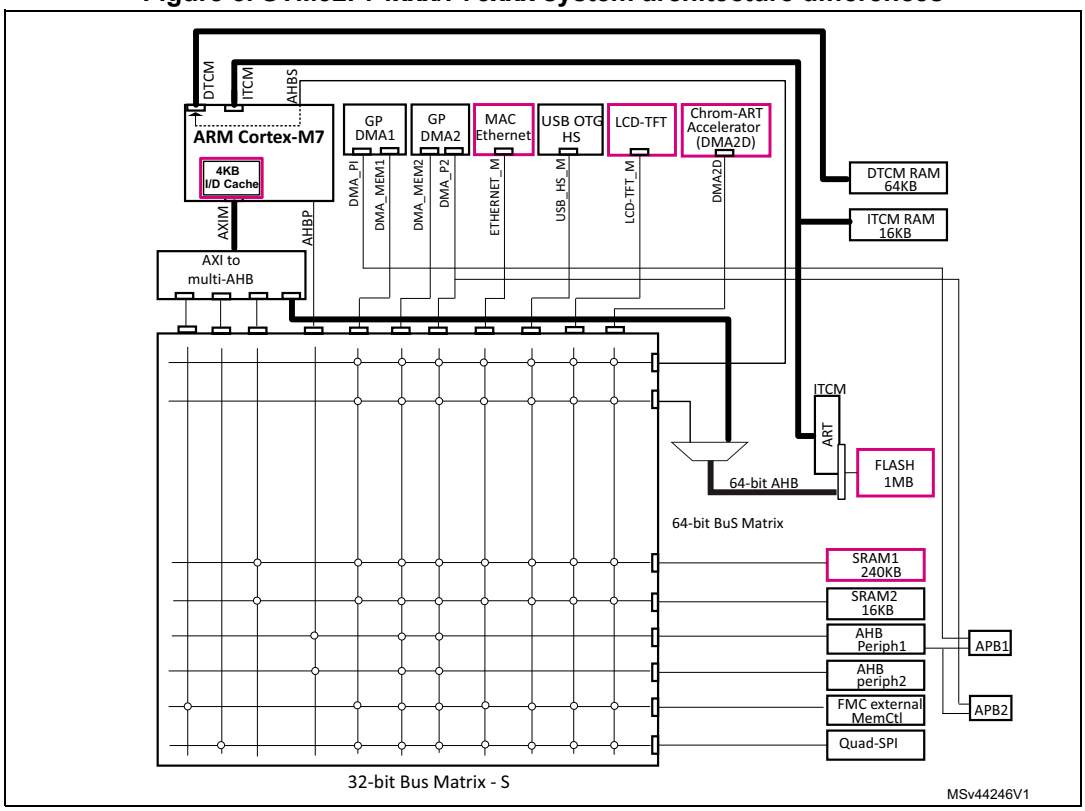


Table 7 summarizes the multi AHB bus matrix interconnection differences between the STM32F74xxx/F75xxx and the STM32F72xxx/F73xxx devices.

Table 7. Multi AHB bus matrix differences

	STM32F74xxx/ STM32F75xxx	STM32F72xxx/ STM32F73xxx
I/D cache size	4 Kbytes	8 Kbytes
Masters	3x32-bit AHB bus Cortex®-M7 AXI Master bus 64-bits, splitted 4 masters through the AXI to AHB bridge.	
	1x64-bit AHB bus connected to the embedded flash	
	Cortex® -M7 AHB Peripherals bus	
	DMA1 and DMA2 memory bus	
	DMA2 peripheral bus	
	Ethernet DMA bus	-
	USB OTG HS DMA bus	
	LCD Controller DMA-bus	-
	Chrom-Art Accelerator™ (DMA2D) memory bus	-
Slaves	The embedded Flash on AHB bus (for Flash read/write access, for code execution and data access)	
	Cortex® -M7 AHBS slave interface for DMAs data transfer on DTCM RAM only	
	Main internal SRAM1 (240 Kbytes)	Main internal SRAM1 (176 Kbytes)
	Auxiliary internal SRAM2 (16 Kbytes)	
	AHB1peripherals including AHB to APB bridges and APB peripherals	
	AHB2 peripherals including AHB to APB bridges and APB peripherals	
	FMC	
	Quad-SPI	

3 Peripherals summary

Table 8 summarizes the list of peripherals available in the STM32F74xxx/F75xxx and STM32F72xxx/F73xxx devices.

Table 8. Peripherals summary

Peripherals		STM32F74xxx/F75xxx	STM32F72xxx/F73xxx
Flash memory in Kbyte		1024	512
SRAM (Kbyte)	System	320 (240+16+64)	256 (176+16+64)
	Instruction	16	
	Backup	4	
Timers	GP	Up to 10	
	Advanced control	2	
	Basic	2	
	Low power	1	
Communication interfaces	Quad-SPI	Yes	
	SPI/I2S	Up to 6/3 (simplex)	Up to 5/3 (simplex)
	I2C	4	3
	USART/UART	Up to 4/4	
	USB OTG FS	Yes	
	USB OTG HS	Yes – Through ULPI interface in the STM32F74xxx/F75xxx/F7x2xx devices. – With embedded PHY HS in the STM32F7x3xx devices.	
	USB OTG PHY HS controller (USBPHYC)	No	– Available only on the STM32F7x3xx devices.
	CAN	2	1
	SAI	2	
	SDMMC1	Yes	
	SDMMC2	No	Yes
	SPDIFRX	Yes	No
RNG		Yes	
FMC memory controller		Yes	
Ethernet		Yes	No
HDMI-CEC		Yes	No
DCMI		Yes	No
WWDG		Yes	
IWDG		Yes	

Table 8. Peripherals summary (continued)

Peripherals		STM32F74xxx/F75xxx	STM32F72xxx/F73xxx
CRC		Yes	
LCD-TFT		Yes(1)	No
DMA		DMA1-DMA2 (8 stream each)	
Chrom-ART-Acc (DMA2D)		Yes	No
Crypto		Yes (CRYP)	Yes (AES256)
Hash		Yes	No
GPIO		Up to 168	– Up to 140 in STM32F7x2xx – Up to 138 in STM32F7x3xx
ADC	12 bits	3	
	Number of channels	16/24	
DAC	12 bits	Yes	
	Number of channels	2	
EXTI		Yes	
RCC		Yes	
RTC		Yes	
PWR		Yes	
SYSCFG		Yes	
Available packages		– LQFP100/144/176/208 – TFBGA100/216 – UFBGA176 – WLCSP143	– LQFP64/100/144/176 – UFBGA144/176 – WLCSP100

1. LCD-TFT not available on the STM32F745xx devices.

3.1 I2C Fast-mode Plus

On the STM32F7x2xx/F7x3xx devices, the I2C I/Os support the 20mA drive needed in Fast-mode Plus. For this purpose, the 20 mA drive enable control bits are added in the SYSCFG_PMC peripheral configuration register.

Furthermore, 4 I/Os (PB6/PB7/PB8/PB9) can be configured with high drive mode even if they are not used as I2C alternate functions. They can be used to drive LEDs for instance.

3.2 Universal serial bus USB

Table 9 summarizes the USB OTG implementation differences in the STM32F74xxx/F75xxx/F7x2xx and STM32F7x3xx devices.

Table 9. USB OTG implementation(1)

USB features	OTG_FS		OTG_HS		
	STM32F74xxx /F75xxx	STM32F7x2xx /F7x3xx	STM32F74xxx /F75xxx	STM32F7x2xx	STM32F7x3xx
BCD support	-	X	-		
ULPI available to primary IOs via muxing	-		X		-
Integrated PHY	FS		FS		FS+ HS

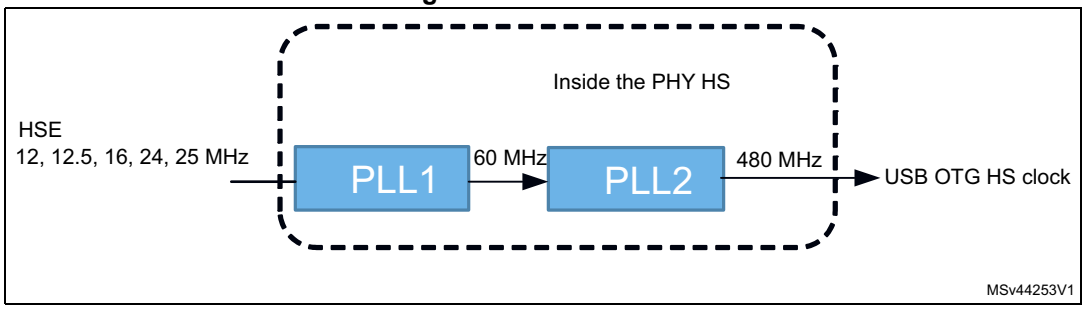
1. ”X” = supported, “-“ = not supported, “FS” = supported in FS mode, “HS” = supported in HS mode.

On the STM32F7x3xx devices, the PHY high speed embeds two PLLs:

- The PLL1 has as clock source the HSE clock. The supported HSE values are: 12, 12.5, 16, 24, 25 MHz.

  The PLL1 outputs the 60 MHz used as input for the PLL2.
- The PLL2 outputs the high speed clock 480 MHz.

Figure 6. PHY HS PLLs



4 Memory mapping

Table 10 presents the peripheral address mapping differences between the STM32F74xxx/F75xxx and STM32F72xxx/F73xxx devices.

Table 10. IP bus mapping differences

Peripheral	Bus	STM32F74xxx/F75xxx	STM32F72xxx/F73xxx
		Base address	Base address
DCMI	AHB2	0x5005 0000 - 0x5005 03FF	No
Chrom-ART (DMA2D)	AHB1	0x4002 B000 - 0x4002 BBFF	No
ETHERNET MAC		0x4002 8000 - 0x4002 93FF	No
GPIOK		0x4002 2800 - 0x4002 2BFF	No
GPIOJ		0x4002 2400 - 0x4002 27FF	No
HDMI-CEC	APB1	0x4000 6C00 - 0x4000 6FFF	No
CAN2		0x4000 6800 - 0x4000 6BFF	No
I2C4		0x4000 6000 - 0x4000 63FF	No
SPDIFRX		0x4000 4000 - 0x4000 43FF	No
LCD-TFT	APB2	0x4001 6800 - 0x4001 6BFF	No
SPI6		0x4001 5400 - 0x4001 57FF	No
USB OTG PHY HS controller		No	0x4001 7C00 - 0x4001 7FFF(1)
SDMMC2		No	0x4001 1C00 - 0x4001 1FFF

1. only for the STM32F7x3xx devices.

5 Embedded Flash memory

Table 11 highlights the differences between the Flash memory interface of the STM32F72xxx/F73xxx and STM32F74xxx/F75xxx devices.

Table 11. Flash memory differences

Flash	STM32F74xxx /F75xxx	STM32F72xxx /F73xxx
Main/program memory	0x0800 0000 - 0x080F FFFF (AXIM) 0x0020 0000 - 0x02F FFFF (ITCM)	0x0800 0000 - 0x0807 FFFF (AXIM) 0x0020 0000 - 0x027 FFFF (ITCM)
	– Up to 1 Mbyte – Split in 1 bank – 4 sectors of 32 Kbytes – 1 sectors of 128 Kbytes – 3 sectors of 256 Kbytes	– Up to 512 Kbytes – Split in 1 bank – 4 sectors of 16 Kbytes – 1 sectors of 64 Kbytes – 3 sectors of 128 Kbytes
Read access of	256 bits	128 bits
Wait State	Up to 9 (depending on the supply voltage and frequency)	
One time programmable (OTP)	1024 OTP bytes	528 OTP bytes
Protection	– Read protection (RDP) – Write protections	– Read protection (RDP) – Write protections – Proprietary code readout protection (PCROP)

The main memory and information block organization are shown in *Table 12*.

Table 12. Flash memory organization

Block	Name	Bloc base addresses on AXIM interface		Bloc base addresses on ITCM interface		Sector size	
		STM32F74xxx /F75xxx	STM32F72xx x /F73xxx	STM32F74xx x /F75xxx	STM32F72xx x /F73xxx	STM32F74xxx /F75xxx	STM32F72xxx /F73xxx
Main memory block	Sector0	0x0800 0000 - 0x0800 7FFF	0x0800 0000 - 0x0800 3FFF	0x0020 0000 - 0x0020 7FFF	0x0020 0000 - 0x0020 3FFF	32 Kbytes	16 Kbytes
	Sector1	0x0800 8000 - 0x0800 FFFF	0x0800 4000 - 0x0800 7FFF	0x0020 8000 - 0x0020 FFFF	0x0020 4000 - 0x0020 7FFF	32 Kbytes	16 Kbytes
	Sector2	0x0801 0000 - 0x0801 7FFF	0x0800 8000 - 0x0800 BFFF	0x0021 0000 - 0x0021 7FFF	0x0020 8000 - 0x0020 BFFF	32 Kbytes	16 Kbytes
	Sector3	0x0801 8000 - 0x0801 FFFF	0x0800 C000 -0x0800 FFFF	0x0021 8000 - 0x0021 FFFF	0x0020 C000 -0x0020 FFFF	32 Kbytes	16 Kbytes
	Sector4	0x0802 0000 - 0x0803 FFFF	0x0801 0000 - 0x0801 FFFF	0x0022 0000 - 0x0023 FFFF	0x0021 0000 - 0x0021 FFFF	128 Kbytes	64 Kbytes
	Sector5	0x0804 0000 - 0x0807 FFFF	0x0802 0000 - 0x0803 FFFF	0x0024 0000 - 0x0027 FFFF	0x0022 0000 - 0x0023 FFFF	256 Kbytes	128 Kbytes
	Sector6	0x0808 0000 - 0x080B FFFF	0x0804 0000 - 0x0805 FFFF	0x0028 0000- 0x002B FFFF	0x0024 0000 - 0x0025 FFFF	256 Kbytes	128 Kbytes
	Sector7	0x080C 0000 - 0x080F FFFF	0x0806 0000 - 0x0807 FFFF	0x002C 0000 - 0x02F FFFF	0x0026 0000 - 0x0027 FFFF	256 Kbytes	128 Kbytes
Information vlock	System memory	0x1FF0 F000 - 0x1FF0 EDBF	0x1FF0 7800 - 0x1FF0 76D7	0x0010 F000 - 0x0010 EDBF	0x0010 7800 - 0x0010 76D7	60 kbytes	30 kbytes
	OTP	0x1FF0 F000 - 0x1FF0 F41F	0x1FF0 7800 - 0x1FF0 7A0F	0x0010 F000 - 0x0010 F41F	0x0010 7800 - 0x0010 7A0F	1024 bytes	528 bytes
	Option bytes	0x1FFF 0000 - 0x1FFF 001F		-		32 bytes	

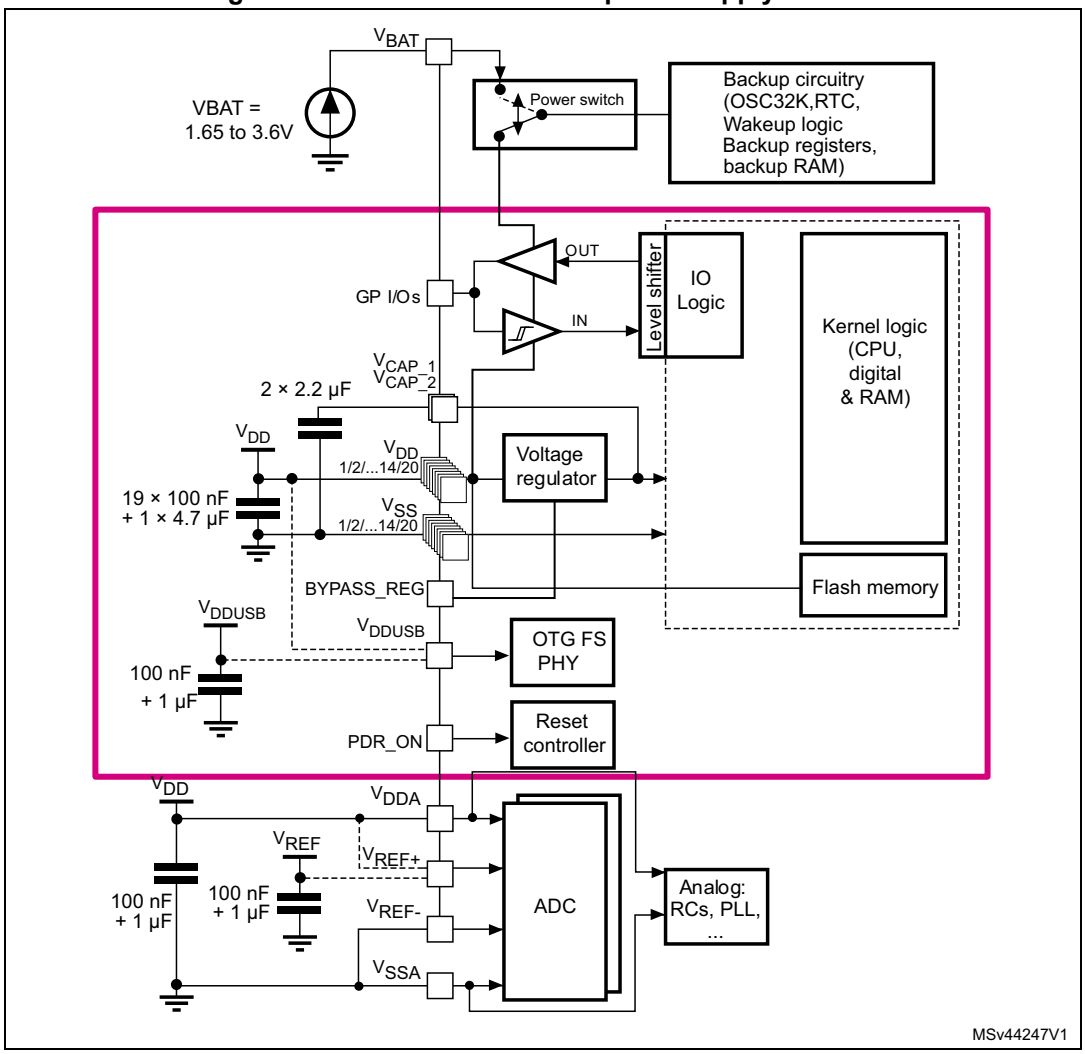
6 Power controller PWR: power supplies

All the STM32F74xxx/F75xxx devices share the same power supplies.

On the STM32F7x3xx devices, the USB PHY HS sub-system uses an additional power supply pin: The VDD12OTGHS pin is the output of the PHY HS regulator (1.2 V). An external capacitor of 2.2 µF must be connected on the VDD12OTGHS pin.

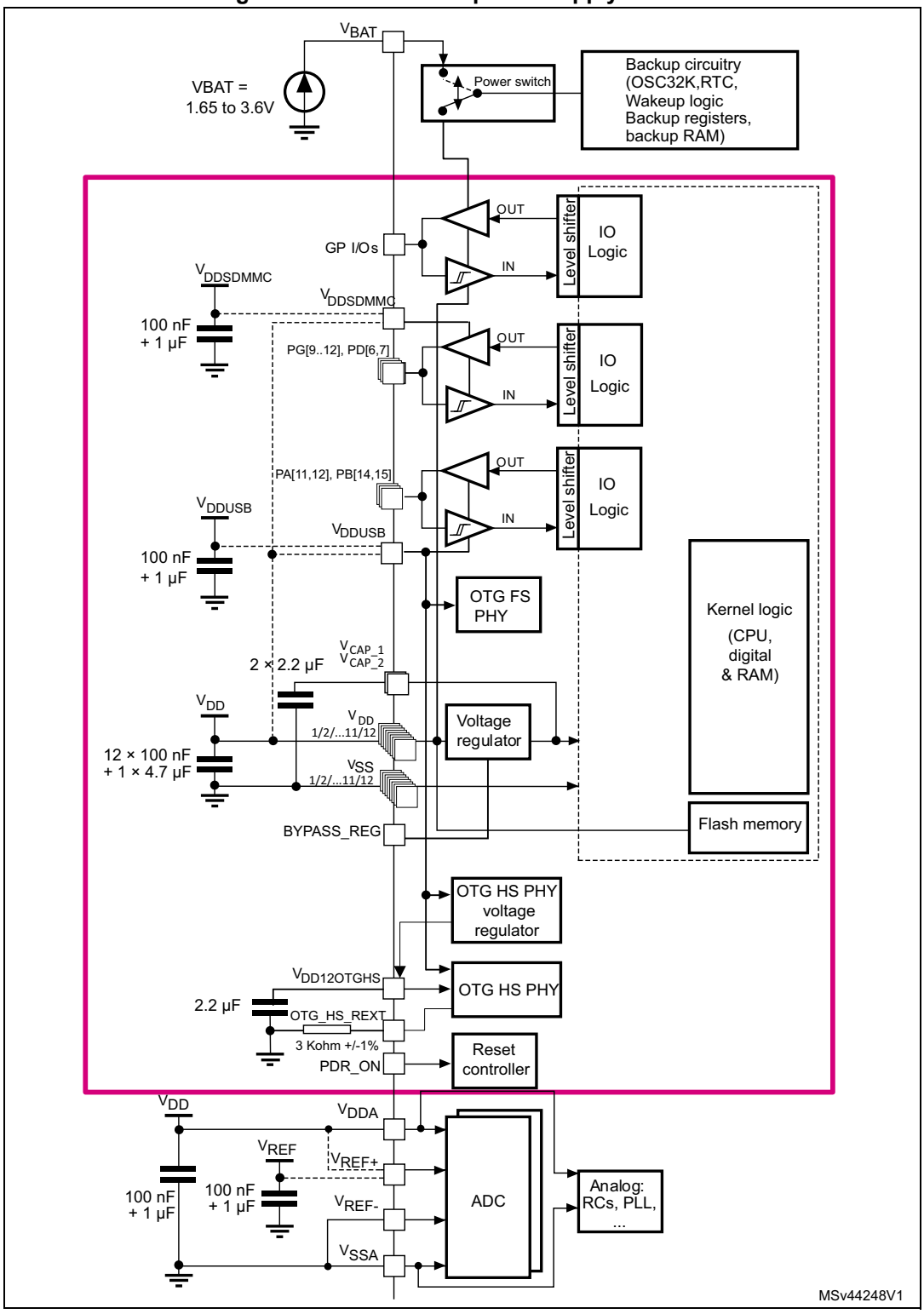
On the STM32F7x2xx/ F7x3xx devices, the SDMMC2 supports a dedicated power rail for the clock, command and data 0..4 lines. The feature is available starting from the 144-pin package. See these differences on *Figure 7*, *Figure 8* and *Figure 9* in the area highlighted in pink.

Figure 7. STM32F74xxx/F75xxx power supply scheme



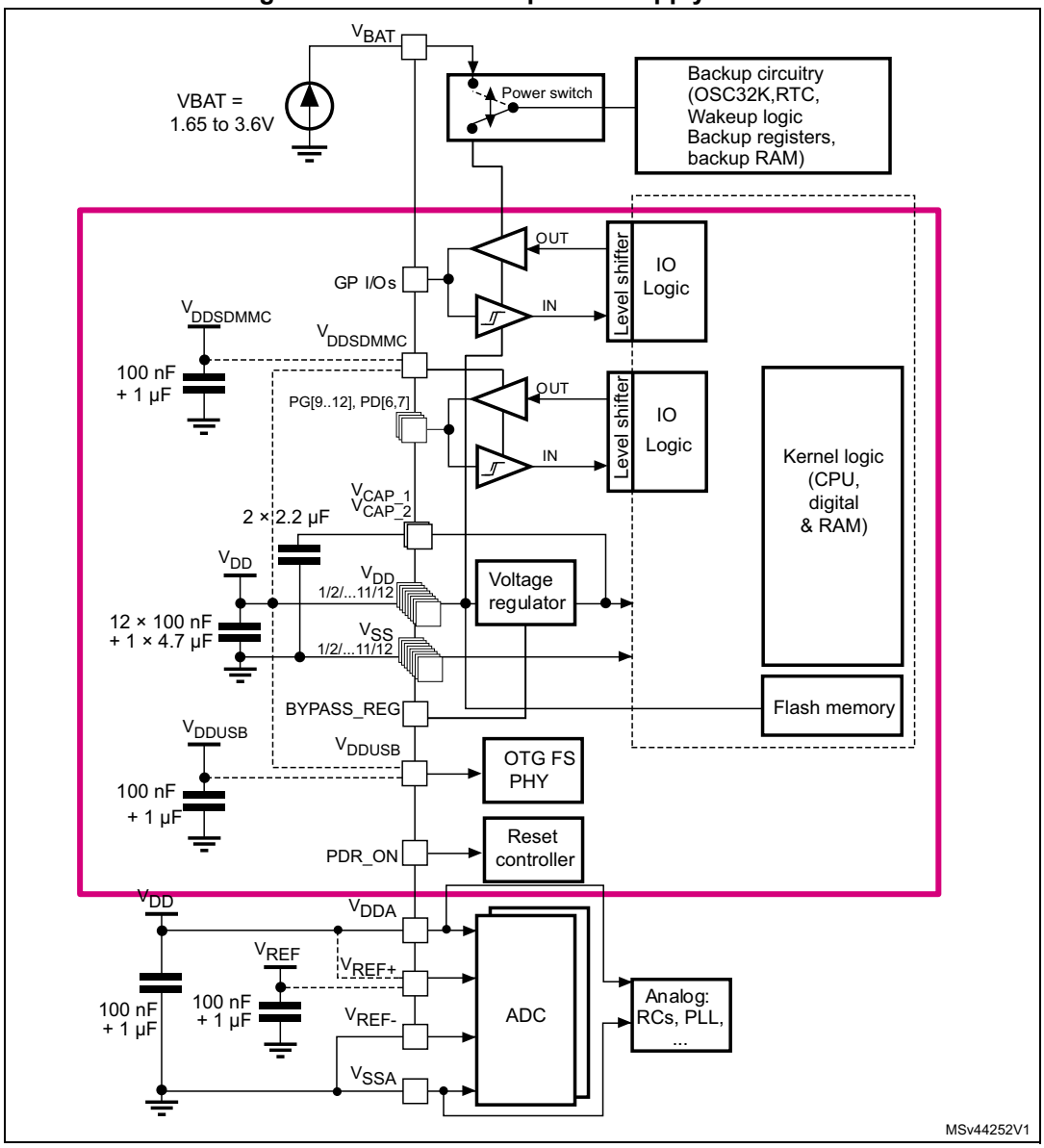
1. On the STM32F74xxx/F75xxx devices, the V_{DDUSB} allows supplying the PHY FS in PA11/PA12 and PB14/PB15.
2. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

Figure 8. STM32F7x3xx power supply scheme



1. On the STM32F7x3xx devices, the V_{DDUSB} allows supplying the PHY FS in PA11/PA12 and the PHY HS in PB14/PB15.
2. V_{DDA} and V_{SSA} must be connected to V_{DD} and VSS, respectively.

Figure 9. STM32F7x2xx powers supply scheme



1. On the STM32F7x2xx devices, the V_{DDUSB} allows supplying the PHY FS in PA11/PA12 and PB14/PB15.
2. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

7 Conclusion

This application note is a useful complement to the datasheets and the reference manuals, which gives a simple guideline to migrate a product between the STM32F72xxx/F73xxx and STM32F74xxx/F75xxx devices.

8 Revision history

Table 13. Document revision history

Date	Revision	Changes
07-Feb-2017	1	Initial release.