

Introduction

The L99SM81V is a bipolar stepper motor driver IC with micro-stepping and coil voltage measurement for stall detection.

This application note is intended to provide guidance to users on specific application-related topics.

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1 Quick motor startup

The L99SM81V does not need any specific device power-up sequence, thus VREG, VS and VDD can be applied in any order without compromising the device behavior. Whenever VS is applied last, the user might need to clear VSUV, VREGUV and CPFAIL flags.

The following steps are the minimum ones required for a quick startup of the motor:

- Power-up the application providing VS, VREG and VDD
- Pull the EN input pin high
- Wait for the tSTART time to elapse before starting any SPI communication with the driver
- If any error flag is already set, try to clear it through a Clear All Status Registers command
- Program the driver registers as desired
- Set the ME control bit to start energizing the motor phases
- Update the phase counter (PH[5:0] bits) via pulses over the CTRL1 pin (MX=1) or via SPI (MX1=0) to make the motor spin

If any fault condition that disables the gate drivers is still present, before setting the ME control bit, all the fault conditions affecting the gate drivers should be removed and afterwards the related flags should be cleared. For instance, in case of a power supply slow ramp-up, once out of power-on reset, the L99SM81V is running but detecting a temporary VSUV condition, which disables the gate drivers. To overcome this situation, the microcontroller should continuously send “clear all status registers” commands until the VSUV failure is no longer detected. Only then, it is possible to set the ME control bit and drive the load.

2 Diagnostics

Diagnostic information is classified in different categories: Functional Errors (FE), Device Errors (DE) and Global Warnings (GW). The device supports bitwise read&clear operations for the global status register (GSR). This means that the clear operation can be addressed to specific status flags through a mask. All the fault/warning events detected by the device latch the related flags; only the global status byte RSTB flag and SPIE flag are automatically cleared by the first valid SPI frame. SPI operations performed at unknown memory addresses do not generate any sort of errors. Trying to write either on read-only registers or on read&clear registers or even trying to perform any read&clear operation on any other register than GSR does not generate any errors.

During the zero current steps, regardless of the CVE control bit value, just one MOSFET of the H-Bridge driving zero current is turned on according to Table 2 in the datasheet (see [Section Appendix A: Document reference](#)). This configuration speeds up the motor phase demagnetization through fast decay and allow sampling the coil voltage with the proper polarity in case CVE=1. During these steps, the overcurrent feature is ensured only by the turned-on MOSFET. When the current is rising, the current regulation is always performed by the HS MOSFETs.

In case any of the output is shorted to GND or in case the motor terminals are shorted together, the nature of the short circuit (i.e. its resistance and inductance) can affect the device over-current detection.

Specifically – in order for the device to detect the over-current and to set the proper OCxLS or OCxHS (x=A, B; n=1,2) bit of the MSR register - it has to be ensured that the sum of the time required for the current to exceed the IOCxn threshold and the over-current comparator reaction time is always smaller than Tonmin ,being Tonmin the sum of tB and tFT.

An application work-around to ensure the over-current detection could then be – for instance – to extend periodically (e.g, every 10ms or 100ms) and for 1PWM cycle the programmed PWM Tonmin by setting the TBE control bit and programming FT[1:0] bit with a value equal or higher than 1. This way, – in fact – the PWM Tonmin is at least equal to 5µs which is generally enough to detect most common terminal short to GND, load short to GND and short between motor terminals.

The ERRor signal (ERR) is the logic OR of any error/warning flag belonging to the following categories: Functional Errors (FE), Device Errors (DE) and Global Warnings (GW). The ERR signal is not affected by any SPIE and RSTB event. The ERR signal is low whenever none of the flags belonging to the three foresaid categories are set. When the failure condition is no longer present, any error/warning flag and hence its contribution to ERR can be promptly cleared by a read&clear operation or by a “clear all status registers” operation. However, there are some exceptions whenever the fault condition is still present (see next paragraph).

The Error Change signal (EC) reflects any new event detection related to any error/warning flag belonging to the same foresaid three categories (regardless of the flag status), whose flag has not yet been read through the global status register (GSR), read&cleared through the GSR or cleared through the “clear all status registers” command since the occurrence of the new event. Once the triggered flag related to the new error/warning event is read (via GSR) or cleared, the EC signal is usually pulled low except in case of permanent error conditions, where there are some exceptions (see next paragraph). EC going low does not necessary mean that the related error/warning flag that pulled EC high in the first place has been canceled.

ERR exceptions in case of permanent failure conditions

VSOV/VREGOV/VSUV/VREGUV/ V5VUVW/TSD: in case of permanent failure condition, any read&clear operation of the GSR corresponding flag or any “clear all status registers” command never pulls ERR low.

TW: in case of permanent TW condition, any read&clear operation of the GSR:TW flag or any “clear all status registers” command could either never pull down ERR or pull it down for tens of us ($0\mu\text{s} \leq \text{low_pulse_width} < 100\mu\text{s}$).

CPFAIL: in case of permanent CPFAIL condition, any read&clear operation of the GSR:CPFAIL flag or any “clear all status registers” command pulls ERR low for about $640\mu\text{s}$ and then back high.

V5VUV/V5VOV: in case of permanent V5V short-circuit condition, any read&clear operation of the corresponding flag or any “clear all status registers” command pulls ERR low for about 4ms and then back high.

OL: in case of permanent open-load condition, any read&clear operation of the GSR: OL flag clears the OL flags, pulling ERR low until the OL flags are set back to one after the programmed open-load detection delay time, which pull ERR high again. In case of permanent OL condition, any “clear all status registers” command pulls ERR low for only about 100ns and then back high.

EC exceptions in case of permanent failure conditions

VSOV/VREGOV/VSUV/VREGUV/V5VUVW/TSD: in case of permanent failure condition, any “clear all status registers” command never pulls EC low. In case of permanent failure condition, any read&clear operation of the GSR corresponding flag or any read operation of the GSR pull EC low. EC stays low even if the corresponding flag was not cleared by the read&clear operation.

TW: in case of permanent TW/TSD condition, any read, read&clear operation of the GSR:TW/TSD flag or any “clear all status registers” command pull EC low and then back high ($25\mu\text{s} \leq \text{low_pulse_width} \leq 150\mu\text{s}$).

CPFAIL: in case of permanent CPFAIL condition, any read&clear operation of the GSR corresponding flag or any “clear all status registers” command pulls EC low for about $640\mu\text{s}$ and then back high. Instead, by just reading the GSR, the EC goes low and stay so despite the ongoing CP fault condition.

V5VUV/V5VOV: in case of permanent V5V short condition, any read&clear operation of the GSR corresponding flag or any “clear all status registers” command pulls EC low for about 4ms and then back high. Instead, by just reading the GSR, the EC goes down and stay so despite the ongoing V5V fault condition.

OL: in case of permanent open-load condition, any read&clear operation of the GSR: OL flag clears the OL flags, pulling EC low until the OL flags are set back to one after the programmed open load detection delay time, which pulls EC high again. In case of permanent OL condition, any “clear all status registers” command pulls EC low for only about 100ns and then back high. Instead, by just reading the GSR, the EC goes low and stay so despite the ongoing OL condition.

In order to simplify application diagnostic management, it's recommended to read the GSR as soon as the EC signal goes high to read out any new error/warning event that has occurred and read the MSR to have more details about the error itself in case of OL error or OC error. Be aware that any access to the MSR does not affect EC at all.

In HOLD mode, when the programmed current reference value is very low (value set by the combination of low HC[3:0] value and phase counter value), the current spikes charging the parasitic output capacitance are detected by the OL detector, thus not allowing open load condition detection.

For instance:

- in HOLD mode for HC[3:0]=0000b the OL condition of PHASE A (open) might not be detected for PH=62,63,0,1,31,32,33,34
- in HOLD mode for HC[3:0]=0001b/0010b the OL condition of PHASE A (open) might not be detected for PH=63,0,1,31,32,33
- in HOLD mode for HC[3:0]=0011b/0100b/0101b the OL condition of PHASE A (open) might not be detected for PH=63,0,32,33

3 Unused pins

[Table 1](#) shows the recommended connections for the unused pins of the device.

Table 1. Unused pins connection

Block/Feature not used	Pin	Control bits	Connection
Analog output	AOUT	AOUT[1:0]=00b	Floating. The 100pF output capacitor can be removed
5 V Voltage Regulator output	V5V	V5VE=0	Floating. The output capacitor can be removed
Digital outputs	DOUT1	DOUT1[1:0]=00b	Floating
	DOUT2	DOUT2[1:0]=00b	Floating
Control inputs	EN	-	Tied to VDD
	CTRL1	MX1=0	Floating
	CTRL2	MX2=0	Floating
	CTRL3	MX3[1:0]=00b	Floating

4 External components

Active reverse battery protection (using a MOSFET driven by the charge pump output) is a viable option for protecting the application against battery reversal. In this case, it is recommended to put a 100kΩ resistor between the CP output pin and the gate of the reverse battery protection MOSFET to minimize the current flowing through this path in case of battery reversal (*Figure 1* Application block diagram).

VS and VREG must be reverse polarity protected; besides, VS should have a 100nF ceramic capacitor placed close to the pin, with the other terminal connected to GND and also an electrolytic capacitor to be sized depending on application, whereas the VREG should have a 4.7 uF electrolytic capacitor to be placed close to the pin, with the other terminal connected to GND.

V5V must have at least a 220nF capacitor, with $ESR \leq 200m\Omega$ connected between V5V and GND, close to V5V. The capacitance between CP+ and CP- should be of 100nF, as well as the capacitance between CP and VS.

V3V must have a capacitor in the range between 100nF (included) and 220nF (included), connected between V3V and GND, close to the V3V pin. VDD should have a 100nF capacitor connected between VDD and GND, close to the VDD pin. The AOUT must have a 100pF capacitor connected between AOUT and GND, close to the pin, only if the band-gap voltage reference were selected as analog output not to affect the band-gap stability. In all the other cases the 100pF capacitor can be omitted. Anyhow, it is always recommended filtering the AOUT before feeding the signal to the Analog to Digital converter.

Filtering capacitors greater than 15nF at the driver outputs might require longer blanking(t_B)/filtering (t_{FT}) time that can be extended by setting dedicated SPI control bits (FTOCE, TBE) in order to avoid detecting false overcurrent events.

PSSO Package

Pin VSA supplies the charge pump.

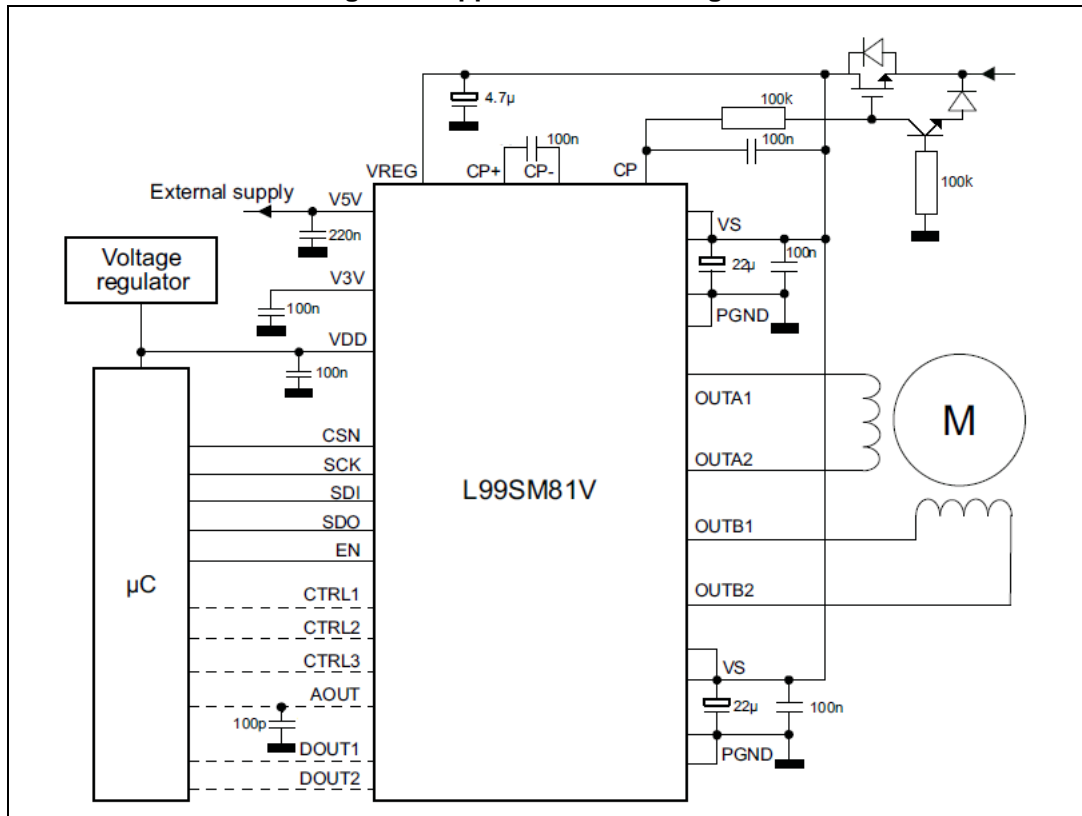
Pin #1 is connected to the slug. The slug is connected to GND. All the NC pins, except PIN #1, are floating.

QFN package

Pin VSA1 and pin VSA2 supply the charge pump.

All the NC pins are floating and not connected to the slug. The slug is connected to GND.

Figure 1. Application block diagram



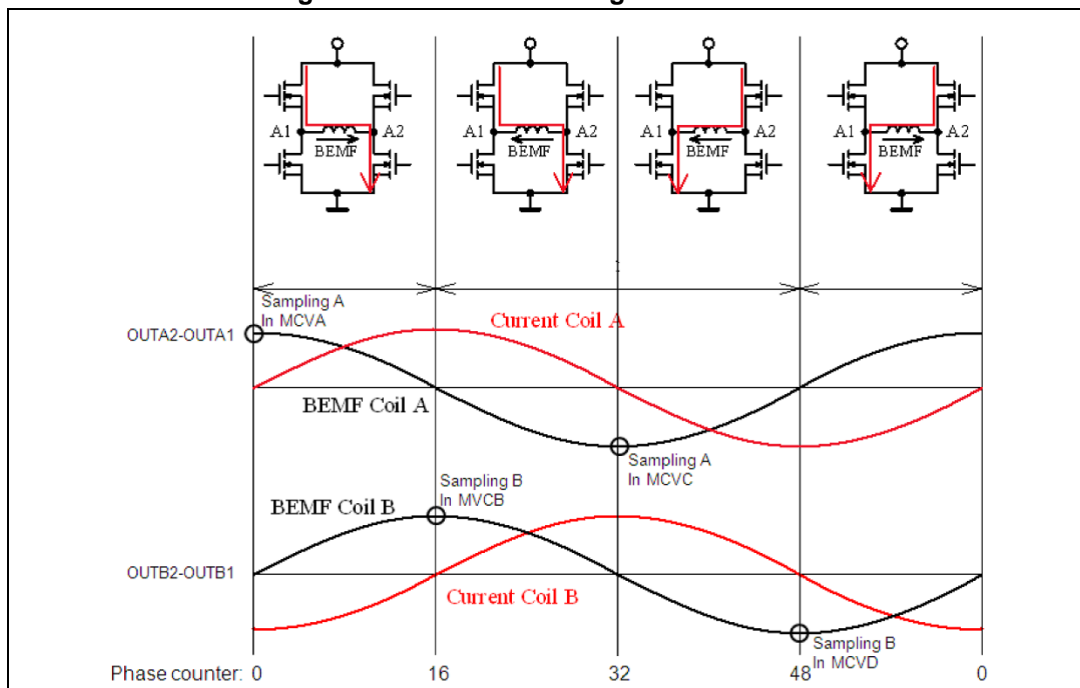
5 HOLD mode

In HOLD mode, the phase counter (PH[5:0] bits) can still be updated, either via SPI (MX1=0) or via CTRL1 (MX1=1), thus providing a lower amplitude current profile than the one that can be achieved in RUN mode. The HOLD mode can be used to hold the motor in place as well by merely stopping updating the phase counter. The phase counter can be updated in HOLD mode as long as AHMSD and SDF bits are not both set to one. In fact, whenever AHMSD and SDF are both set to one, the HOLD mode bit is automatically set, sending the device in HOLD mode and preventing, the phase counter from being updated. If already in HOLD mode, the phase counter update is stopped as soon as both AHMSD and SDF bits are set to one. The programmed HOLD mode full scale current multiplication factor is active, replacing the programmed RUN mode full scale current multiplication factor, as soon as the HOLD mode is entered. On the other hand, the programmed RUN mode full scale current multiplication factor is active, replacing the programmed HOLD mode full scale current multiplication factor, as soon as the RUN mode is entered.

6 Coil voltage measurements

If enabled through the CVE control bit, during each zero current step (phase counter equal to 0,16,32,48) the voltage of the un-driven motor phase is sampled at the programmed time (coil voltage measurement triggering) and stored in one of the dedicated registers, (MCVA,MCVB,MCVC,MCVD) in order to be read by the microcontroller and/or compared by the device itself to programmable thresholds. This feature cannot be used either in full step mode or in combination with the current regulation PWM frequency wobbling feature (MWBE=1). The coil voltage measurement feature is always active as soon as CVE=1, regardless of the ME control bit value. Since the phase counter can still be updated via SPI in case MX1=0 and ME=0, this means that the coil voltage measurements could still be active and running even if the motor is not spinning.

Figure 2. Motor Coils Voltage Measurement



There are three thresholds that can be set through control registers MCVLLA, MCVLLB and MCVUL to detect whether the latest stored coil voltage measurement, indicated by CVLUR bits, falls below or above each programmed threshold. Even though the flags CVLLAF, CVLLBF and CVULF are just information flags and hence are not reported as device warnings/errors, the lower threshold B (MCVLLB) can be used as warning through information flag CVLLBF to detect whether the latest coil voltage acquisition falls below the programmed threshold value MCVLLB. The upper threshold U (MCVUL) can be used as warning or stall detection through, respectively, information flag CVULF or SDF flag, to detect whether the latest coil voltage acquisition falls above the programmed threshold value MCVUL. Finally, lower threshold A (MCVLLA) can be used as warning or stall detection, through information flag CVLLAF or SDF flag respectively. The CVLLAF is set whenever the latest coil voltage acquisition falls below the programmed threshold value MCVLLA. The SDF flag, classified as FE, is set as soon as the programmed number of consecutive coil voltage measurements falls outside the programmed range defined by the thresholds MCVLLA (lower threshold) and MCVUL (upper threshold). When the coil voltage

measurement is enabled (CVE=1), the information flags CVLLAF, CVLLBF, CVULF and CVLUR[1:0] are updated at the end of each coil voltage measurement, in particular the first three information bits (CVLLAF, CVLLBF, CVULF) are updated according to the outcome of the comparison between the latest acquired coil voltage measurement and the related programmed threshold. There is no way to clear any foresaid information bit together with any of the coil voltage measurement registers (MCVA, MCVB, MCVC, MCVD) but through a POR event or through a transition HIGH-LOW-HIGH of the EN input pin. The content of the MCV registers, storing the coil voltage measurement values, can be read at any time via SPI. The content of the registers can be converted in a voltage value through the following formula:

$$\text{Motor Coil Voltage register value} = \frac{\text{10bit Register (decimal)}}{1023} \times 28\text{V}$$

7 Current regulation

The current sensing needed for the current regulation is normally performed by the HS MOSFETs. A minimum PWM ON time $T_{ON,min}$ equal to $t_B + t_{FT}$ (t_B is the blanking time and t_{FT} is the filter time of the current comparators) is always applied when a motor phase is energized. When mixed decay is used, an additional $T_{ON,min}$ is applied during fast decay and the current sensing is performed by the LS MOSFETs in order to determine when a transition from fast decay to slow decay has to occur. Depending on the application parameters (such as motor supply voltage or inductance), the duration of $T_{ON,min}$ can potentially affect current regulation because the motor phase current may significantly exceed the desired target current during this time. Therefore care must be taken in order to select blanking time, filter time and decay modes properly.

During the programmed blanking time, the output of both the current regulation comparator and the overcurrent comparator are neglected. Once the blanking time t_B has elapsed, the outputs of both comparators are taken into account. In particular, if the output of the current regulation comparator is high (i.e. the measured current is above the programmed reference value), the selected decay mode is started as soon as the programmed filter time t_{FT} has elapsed.

7.1 Auto Decay Mode 2 versus Auto Decay Mode 1

Auto Decay Mode 1 (ADM1) and Auto Decay Mode 2 (ADM2) apply mixed decay during the OFF time of the output stage (current freewheeling), depending on phase counter value and motor rotation direction. Unlike ADM1, ADM2 uses only slow decay once the target current is reached, thus minimizing current ripple. Therefore ADM2 is usually the best choice among the available decay modes, unless the selected $t_{ON,min}$ does not allow the regulation of the target current without using fast decay.

[Table 1](#), [Table 2](#) and [Table 3](#) show the current ripple values in ADM1 and ADM2 for two values of $t_{ON,min}$ and two different target currents when driving a stepper motor having $L = 50$ mH and $R = 39$ Ω .

- Driver settings: phase counter value=28, PWM=20KHz, PWM $t_{ON,min} = 1.5\mu s$, full-scale current in run mode = 396 mA.

Table 2. Current ripple ADM1 versus ADM2 for IFSR = 396mA and $t_{ON,min} = 1.5\mu s$ example

Decay mode	Current ripple	Target current
ADM1	13.8 mA	181 mA
ADM2	11.8 mA	

- Driver settings: phase counter value = 28, PWM = 20 KHz, PWM $t_{ON,min} = 4.5\mu s$, full-scale current in run mode = 679 mA.

Table 3. Current ripple ADM1 versus ADM2 for IFSR = 679 mA and $t_{ON,min} = 1.5\mu s$ example

Decay mode	Current ripple	Target current
ADM1	16.6 mA	276 mA
ADM2	13.8 mA	

- Driver settings: phase counter value = 28, PWM = 20KHz, PWM $t_{ON,min} = 4.5\mu s$, full-scale current in run mode = 679mA.

Table 4. Current ripple ADM1 versus ADM2 for IFSR = 679 mA and $t_{ON,min} = 1.5\mu s$ example

Decay mode	Current ripple	Target current
ADM1	26 mA	276 mA
ADM2	13.4 mA	

8 Phase counter update and step mode change

Whenever the phase counter is updated by rising edges over the CTRL1 pin for MX1=1, the pulses must have a minimum width of 400ns. However, we recommend a minimum pulse width of 1µs. Any pulse train of 100 KHz still guarantees the proper phase counter update.

In PIN mode (MX1=1), the phase counter bits are updated by any rising edge over CTRL1 input pin, depending on selected step mode and programmed DIR control bit, together with the new reference current value, both becoming effective only at the beginning of the next PWM cycle. In SPI mode (MX1=0), the phase counter bits are not immediately updated by any SPI write event, likewise in PIN mode, but only together with the new reference current value that becomes effective only at the beginning of the next PWM cycle. This means that reading the phase counter value just updated via SPI, but prior to the beginning of the next PWM cycle, returns the old phase counter value. In SPI mode, the selected step mode does not have any effect on the output reference current except in fullstep mode, where the output reference current is set to the one corresponding to PH=8,24,40,56, as defined by the spinning direction continuity principle.

Whenever the step mode is changed we can distinguish two cases:

- In PIN mode (MX1=1), the phase counter value, together with the new current reference value, is updated with the new one according to the new selected step mode and DIR control bit value at the first rising edge over CTRL1 following the step mode change command.
- In SPI mode (MX1=0), when entering/exiting the fullstep mode the phase counter value together with the new current reference value is updated with the new one written via SPI frame, following the step mode change command (when entering into fullstep mode, the spinning direction continuity principle must be taken into account. In this case, to avoid any unexpected current profile change, we recommend, entering full step mode whenever the phase counter is equal to any of the following values: 8,24,40,56).

[Table 5](#) shows the phase counter increment (DIR=0) /decrement (DIR=1) and related values whenever it is updated via CTRL1 pin (MX1=1) according to the selected step mode (SM[2:0]/ASM[2:0]):

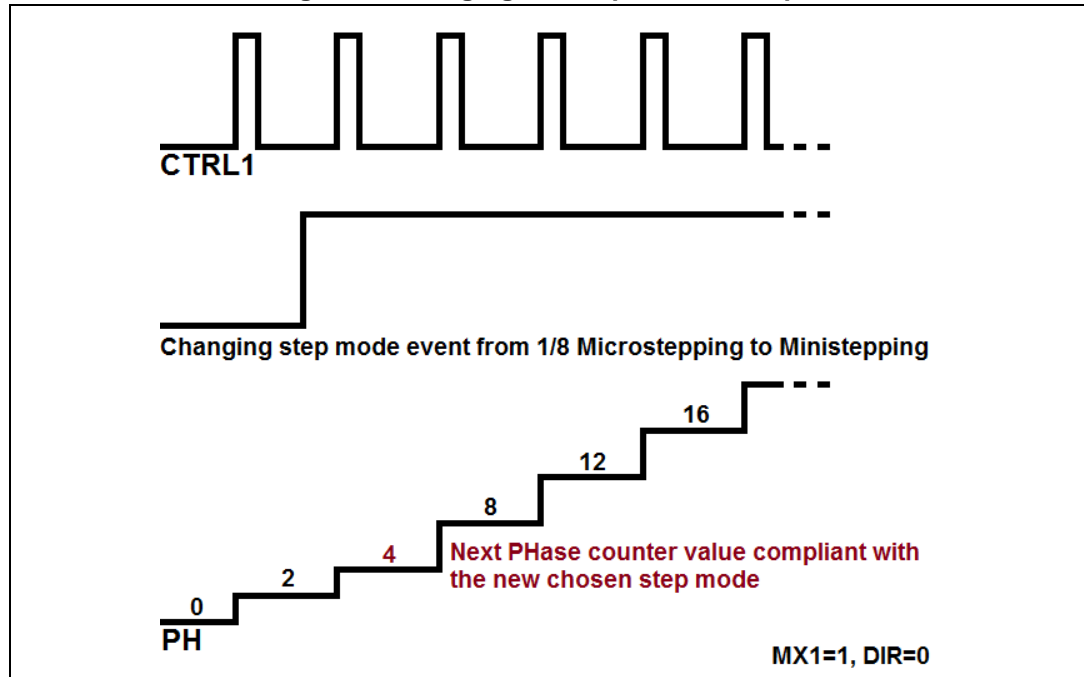
Table 5. Phase counter in CTRL1 update mode (MX1=1)

Step mode	Increments/Decrements	Phase counter values
1/16 Micro-stepping	±1	0,1,2,3,4,...,59,60,61,62,63
1/8 Micro-stepping	±2	0,2,4,6,8,...,54,56,58,60,62
Mini-stepping	±4	0,4,8,12,16,...,44,48,52,56,60
Half-stepping	±8	0,8,16,24,32,40,48,56
Full-stepping	±16	8,24,40,56

As a general rule for MX1=1, regardless of the DIR control bit value, whenever the step mode is changed from higher resolution to lower resolution, the first phase counter increment/decrement could be less than the one corresponding to the new selected step mode. Basically, the first phase counter update event following a step mode change to a lower resolution step mode would set the phase counter to the next new step mode compliant phase counter value.

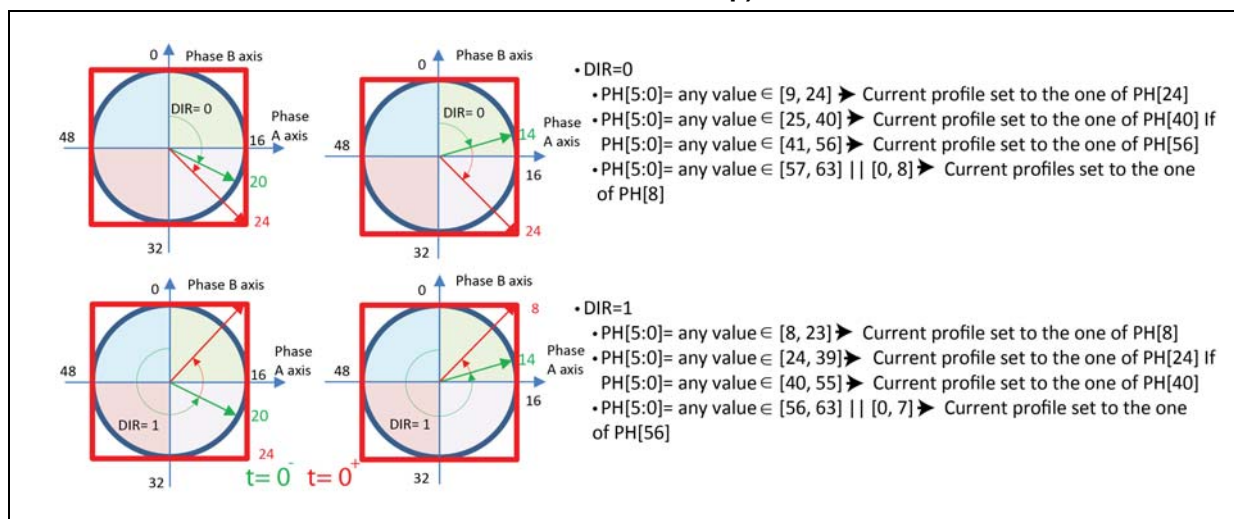
For instance, changing from 1/8 Micro-stepping mode with PH=2 and DIR=0 to Mini-stepping mode would affect the phase counter as shown by the following [Figure 3](#):

Figure 3. Changing the Step Mode Example



The phase counter can be updated in SPI mode (MX1=0) even if ME=0. On the other hand, the phase counter cannot be updated via CTRL1 input pin (MX1=1) when ME=0. To avoid any current profile deviation/variation when changing step mode for MX1=1 to one with lower resolution or moving from SPI update mode of the phase counter to PIN update mode, any change should be made, during phase counter values that belong to both step modes.

Figure 4. Spinning direction continuity principle (example given for any step mode to full-step)



Appendix A Document reference

Programmable stepper motor driver for automotive applications with micro-stepping and stall detection (DataSheet, DocID027599).

Revision history

Table 6. Document revision history

Date	Revision	Changes
26-Sep-2017	1	Initial release.
22-Nov-2017	2	Updated: - <i>Section 4: External components</i> - <i>: PSSO Package</i> - <i>: QFN package</i> - <i>Figure 1: Application block diagram</i>

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