Application note

Signal conditioning for resolver

Introduction

This application note deals with the analog signal conditioning circuit used to drive a resolver and receive information from it.

Some hints are given to use simple schematics to apply the right signal to the resolver and get back the analogic results before a digital treatment.

The simplicity of the resolver makes it reliable in many standard and extreme applications such as: servo motors, factory automation, steel and paper mills, oil and gas production, jet engine fuel systems and aircraft flight.

The main concern is how to drive it, as much part of the time it needs a typical input voltage in the range from 1 to 26 VAC and the frequency can vary in the range from 40 Hz to 10 kHz.

The maximum current flowing in the reference winding is generally less than 100 mA. The TSX564 at 16 V op-amp family is a perfect choice to drive a resolver.

1 How does it work?

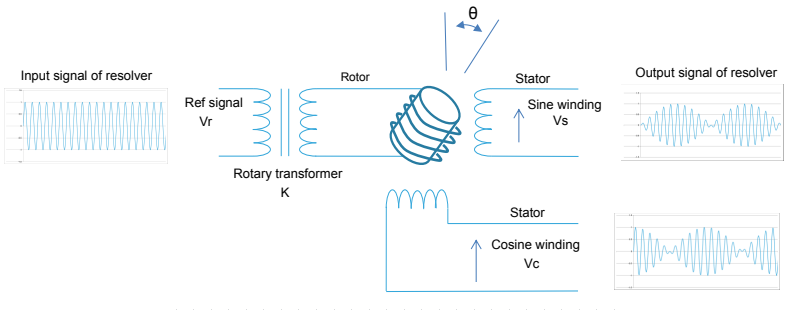
Basically the resolver is a rotary transformer with one rotating winding (supplied by V_r) and two stator windings. The reference winding is fixed on the rotor, and therefore, it rotates jointly with the shaft passing the output windings as described in Figure 1. Resolver principle.

Resolver hardware can be viewed as two inductive position sensors, which, upon a supplied sinusoidal shaped signal on the input, generate two sinusoidal signals on the output. The amplitude of one signal is proportional to the sine. The amplitude of the other is proportional to the cosine of the shaft angle position.

Both windings further refer to as output windings.

The ratio of these two signals is then analyzed and determines the absolute position.

Figure 1. Resolver principle



The frequency of the generated voltages V_s and V_c, equals the frequency of the reference voltage V_r, and their amplitudes vary according to the sine and cosine of the shaft angle θ.

The input reference signal can be described by the following formula:

$$V_r = A0.\sin\omega t \quad (1)$$

with A0 is the amplitude of the input signal and ω is the resolver driving frequency

$$V_C = K * V_r * \cos\theta \quad (2)$$

With K is the transformation ratio and θ the rotor angle.

$$V_S = K * V_r * \sin\theta \quad (3)$$

With K is the transformation ratio and θ the rotor angle.

As Eq. (2) and Eq. (3) are expressed the sine and cosine for the rotor angle, it is quite easy to get the shaft angle thanks to the Atan function. And by ignoring imperfections, the shaft angle would be expressed by the equation below.

$$\theta = \mathrm{Atan}\left(\frac{Vs}{Vc}\right) \quad (4)$$

2 Signal conditioning to drive the reference winding

Most part of the time, a high voltage (generally >= 10 V) is necessary to drive a resolver.

A simple gain voltage amplifier schematic can be used with a 16 V amplifier as the TSX family.

However, should a larger amplitude be needed, this kind of schematics does not work anymore.

So, to drive correctly a resolver with higher amplitude for a given power supply, the schematic described in Figure 2. Schematic to drive a resolver can be used. This is a two stage configuration; the first stage is used to amplify the input signal with a gain of R2/R1 and drive the first input of the resolver Vo1.

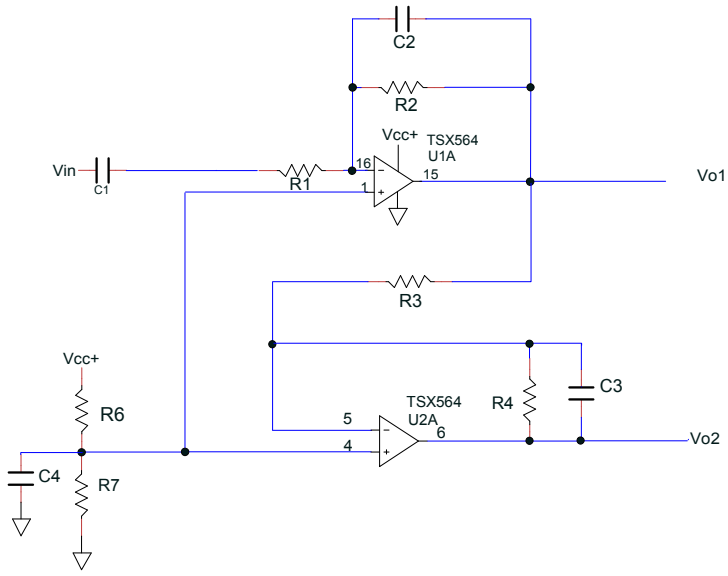
Vo1 signal is also connected to the second stage with a gain of -1(by considering R3=R4) in order to get a Vo2 signal, which is the opposite of Vo1 signal.

Vo2 signal is thus connected to the second input of the resolver.

At the end the differential signal Vo2-Vo1, seen by the resolver, has amplitude two times higher than the input signal V_{in}.

It can be demonstrated by the Eq. (7), describing the AC transfer function of the schematic below:

Figure 2. Schematic to drive a resolver



2.1 Transfer function

The schematic showed in Figure 2. Schematic to drive a resolver is a single-to-differential output.

Output 1 Vo1, can be described in AC as the following equation:

$$Vo1 = -\frac{Vin.jR2.C1.\omega}{(1+jR1.C1.\omega)(1+jR2.C2.\omega)} \quad (5)$$

Output 2 Vo2, can be described in AC as the equation below:

$$Vo2 = -\frac{Vo1}{(1+jR3.C3.\omega)} \quad (6)$$

Eq. (6) shows that for frequency lower than $\frac{1}{2\pi R3C3}$, the signal on Vo2 has the same amplitude of Vo1, but with a phase shift of 90°.

The resolver is driven in differential, so the transfer function of the whole system can be described by the equation as follows

$$Vo2 - Vo1 = \frac{2.Vin.jR2.C1.\omega\left(1+\frac{jR3.C3.\omega}{2}\right)}{(1+jR1.C1.\omega)(1+jR2.C2.\omega)(1+jR3.C3.\omega)} \quad (7)$$

Eq. (7) demonstrates that the differential voltage applied on the input of the resolver is twice higher than the input signal. Let us detail the Eq. (7) and explain the role of the capacitance C1, C2 and C3.

The C1 capacitance is a coupling capacitor. C1 is for sure calculated depending of the frequency of the input signal and resistance R1. As demonstrated by the Eq. (7), C1 capacitor with the R1 act as a high pass filter, with a cut-off frequency (3dB) at $fpH = \frac{1}{2\pi R1C1}$.

The capacitance C2 and C3 combined with R2 and R3 respectively, act as low pass filter which can be a second-order depending of the value of C2, C3 and R2, R3.

$$fpL1 = \frac{1}{2\pi R2C2} \quad (8)$$

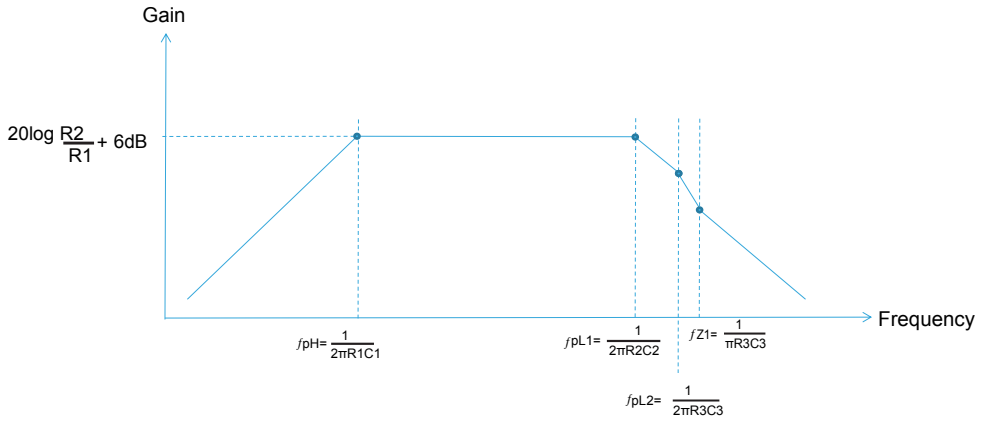
$$fpL2 = \frac{1}{2\pi R3C3} \quad (9)$$

This low pass filter can be necessary in order to filter unwanted parasitic high frequency signal, but for sure it adds some phase shifting on the signal.

Thanks to Eq. (7), a zero appears at the frequency $Fz1 = \frac{1}{\pi R3C3}$.

Eq. (7) can be also shown as a bode diagram described in the figure below.

Figure 3. Bode diagram of the transfer function equation 7



Note: C4 capacitance is important to avoid any ripple on the reference voltage.

2.2 Phase shift

The phase shift is an important point to take into consideration, as it is a source of inaccuracy introduced by the application schematic.

Actually the signal applied on the reference winding cannot really be considered as described by the Eq. (1) but rather as:

$$V_r = A0.\sin(\omega t + \varphi 1) \quad (10)$$

Where φ1 is the phase shift introduced by the op-amps and external components.

The phase shift φ1 represents in degree the difference between the time phase of the input sinusoid signal and the time phase of the signal apply on the reference winding.

Note that resolvers have also their own phase shift φ2 (which is the time phase difference between primary voltage and secondary voltage when the resolver works with maximum magnetic coupling), that must also be taken into consideration in the whole signal chain. The equation below expresses in degree the phase shifting φ1 introduced by Figure 2. Schematic to drive a resolver

$$\varphi 1 = 90° + Atan\left(\frac{R3.C3.\omega}{2}\right) - Atan(R1.C1.\omega) - Atan(R2.C2.\omega) - Atan(R3.C3.\omega) \quad (11)$$

The Figure 3. Bode diagram of the transfer function equation 7, shows 3 poles and 1 zero. Each pole adds a -20 dB/decade slope to the plot (pole) and 45° phase shift accumulates at each poles at the cutoff frequency and closes to 90° far from the cutoff frequency.

So this point must be taken into consideration when an application to drive a resolver is designed. Due to process and temperature variation, resistances and capacitor values might change. And so the pole described by Figure 3. Bode diagram of the transfer function equation 7 might vary and the theoretical phase shift as well.

By selecting FpH and FpL1 poles with more than 1 decade around the input frequency necessary to drive the resolver, this phase shifting error can be limited.

FpL2 has to be better chosen far above FpL1 not to introduce extra phase shift to the one already added by FpL1.

This kind of architecture forms a band pass filter for the undesired frequency. The best filtering is to have the sharpest filter around the working frequency. This means having for example two poles FpH and FpL1 as closer as possible, which is not good for φ1.

A good compromise, between the phase shifting error and the right filter, must be found.

2.3 Maximum amplitude error on the reference winding

From an AC point of view, the gain of the schematic Figure 2. Schematic to drive a resolver can be written as described by the equation below:

$$Gain = \frac{R2}{R1} + \frac{R4}{R3} \cdot \frac{R2}{R1} \quad (12)$$

The equation above gives a result of gain by considering that the used resistances match perfectly. Unfortunately it is not the case, as the resistances have their own precision.

The error on the gain, due to the mismatch of the resistances is given by the following formula:

$$Gain = \frac{2R2}{R1}\left(1 + 3\varepsilon\right) \quad (13)$$

Where ε is the precision of any of resistances.

If resistances are chosen with a precision of 1%, the maximum gain error due to the mismatch is 3%. For a better accuracy 0.1% resistances should be chosen, in this case the gain error is 0.3%.

2.4 Power dissipation and junction temperature

The impedance of the resolver is quite low and this kind of device is generally driven with a high voltage. So the op-amps, used to drive the reference winding, should be able to source high current. Therefore, the power dissipation must be taken into consideration in order to be sure that the maximum junction temperature of the op-amp is not overpassed.

The junction temperature can be calculated by the equation:

$$Tj = Pwd^{*}Rthja + Ta \quad (14)$$

Where Pwd is the power dissipation of the amplifier expressed in W.

Rthja is considered as the junction-to-ambient thermal resistance (°C/W). It represents the difference between the junction and ambient temperature when the power dissipated by the op-amp= 1 W, and Ta, the ambient temperature, is expressed in °C.

Let's calculate the power dissipation of the amplifiers in order to have an idea of the junction temperature.

The power dissipation in the amplifiers is the difference between the total power dissipation at the power supply level and the power dissipated in the resolver itself.

$$Pwd = Ptot - Pres \quad (15)$$

The resolver impedance is generally expressed in rectangular form as R+jLω where R is the resistance and Lω is the inductive reactance.

The magnitude of the impedance is given below:

$$|Z| = \sqrt{R^2 + L^2\omega^2} \quad (16)$$

Let's first calculate the total power dissipation Ptot. During half time the current is sourced through one op-amp and during the second half it is sourced through the second channel.

$$Ptot(t) = Vcc^{*}|I(t)| \quad (17)$$

The signal applied on the resolver is a sine signal so:

$$\left|I(t)\right| = \frac{2Vp \cdot |sin\omega t|}{|Z|} \quad (18)$$

Where Vp is Vpeak signal of the output of each op-amp, Vcc the power supply voltage of the op-amp. We can then deduce the average total power dissipation by a simple integration. As each amplifier supplies a half wave rectified current to the resolver load, the integration can be done on a half period (T/2).

$$Ptot = \frac{1}{T/2} \cdot \int_0^{T/2} \frac{2.Vcc.Vp}{|Z|} sin\omega t \, dt \quad (19)$$

$$Ptot = \frac{4.Vcc.Vp}{\pi.|Z|} \quad (20)$$

Now let's calculate the power dissipation into the load:

$$Pres(t) = R^{*}Iin^{2}(t) \quad (21)$$

With

$$Iin = \frac{2.Vp}{|Z|} \quad (22)$$

$$Pres = \frac{2.R.Vp^{2}}{|Z|^{2}} \quad (23)$$

With reference to the Eq. (15), the power dissipated in the op-amps can be written as follows:

$$Pwd = \frac{4.Vcc.Vp}{\pi.|Z|} - \frac{2.R.Vp^{2}}{|Z|^{2}} \quad (24)$$

Note that power consumption (Icc) of the op-amp has not been considered.

2.5 Application example

In this application example, a resolver is driven with the following features:

input voltage of 7.5 Vrms with frequency of 4 kHz. The input current max. is 16 mArms.

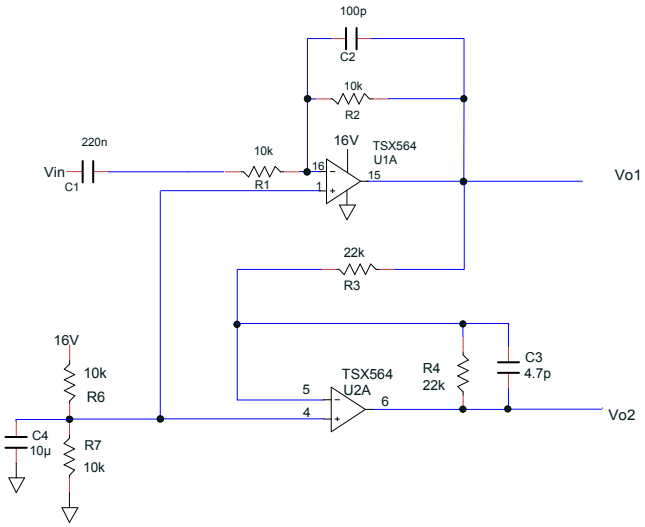
The TSX564 op-amp is chosen because of its wide voltage range supply 16 V and its capability to source high current (90 mA typical).

The FpH is fixed to 70 Hz in order to filter 50 Hz. R1 is fixed to 10 kΩ. So C1= 220 nF.

The Flp1 is fixed to 160 kHz. R2 is also set to 10 kΩ. So C2 = 100 pF.

In order to have Flp2 far enough from Flp1, 1 decade is set above, so Flp2= 1.6 MHz. R3=22 k so C3=4.7 pF.

Figure 4. Application schematic to drive a resolver



The following picture shows a scope of the input signal amplitude, which has been multiplied by two thanks to the architecture presented in Figure 2. Schematic to drive a resolver. An error of 1.6% can be observed on Vo2-Vo1 signal compared to the theoretical value, mainly due to the matching of the resistance (resistance tolerance1%) see Eq. (13).

Figure 5. Probe scope of input and reference voltage signal

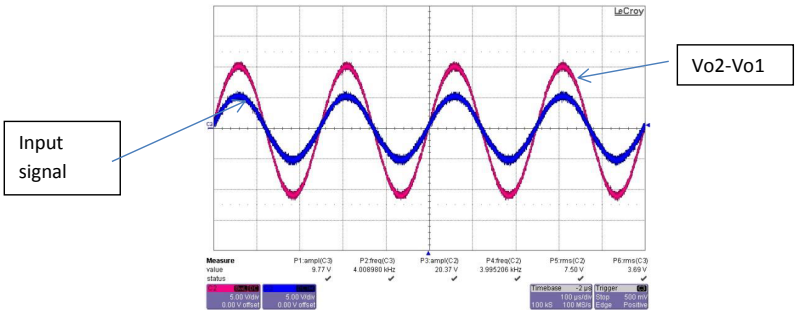
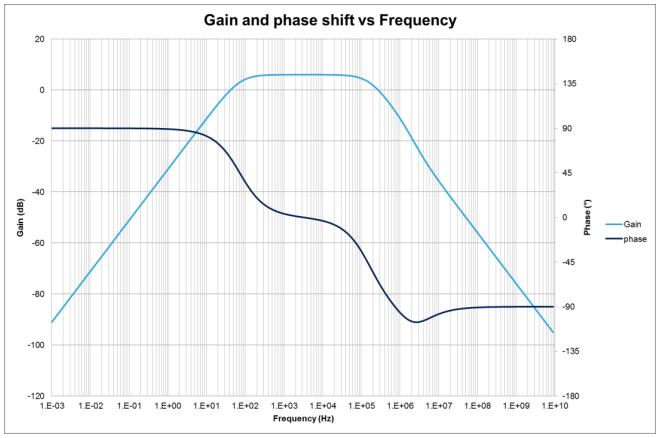


Figure 6. Gain and phase shift vs frequency shows the gain and the phase shift vs frequency corresponding to the application schematic detailed in Figure 4. Application schematic to drive a resolver.

The bandwidth of the band pass filter is from 70 Hz to 160 kHz allowing having a minimum phase shifting at the working frequency of 4 kHz. Actually the phase shifting at 4 kHz is 0.4°. As it is shown by the graph below, the phase shifting is quite flat in the region of 4 kHz, allowing small variation of the external component value, without a big change of the phase shift.

Figure 6. Gain and phase shift vs frequency



In order to save space on the PCB, the TSX564 can be chosen in QFN16 package. The Rthja of this package is 80 °C/W. Following to Eq. (14) and Eq. (24), we can deduce firstly the power dissipation of the op-amps.

$$Pwd = \frac{4*16*5.3}{\pi.\sqrt{220^2+206^2}} - \frac{2*220*5.3^2}{\left(220^2+206^2\right)} = 222\ mW \quad (25)$$

and then the temperature junction:

$$Tj = 0.222*80 + 25 = 43\ ^{o}C \quad (26)$$

It means there is an elevation of temperature of 18 °C compare to the ambient temperature.

By using the TSX564 in QFN package, this kind of application can also reach the 125 °C.

The TSX564 is a quad op-amp; the two added op-amps is used as active filtering for the resolver SIN/COS receiver circuit.

3 Signal conditioning for SIN/COS windings

The resolver SIN/COS receiver circuit can be fulfilled with a simple differential-to-single op-amp as described by Figure 7. Schematic resolver sine receiver circuit and Figure 8. Schematic resolver cosine receiver circuit. The voltage gain is defined thanks to the ratio of the resistances R9/ R8 for sine receiver circuit, and R13/ R12 for cosine receiver circuit. So the signal can be adjusted to fit the acceptable range of the ADC. Moreover a DC bias must be added and it can be adjusted thanks to a reference voltage, in order to shift the signal to the middle of the ADC range. Figure 7. Schematic resolver sine receiver circuit describes the analog chain to address the sine part of the resolver. The same kind of architecture has to be used for the cos part as shown by Figure 8. Schematic resolver cosine receiver circuit.

The capacitors C5 C6, add low pass filter in order to suppress unwanted high frequency. The cut-off frequency of this filter must be chosen largely higher than the working frequency in order not to affect a resolver signal and not to introduce a significant phase shifting.

In order to balance the gain and the low pass filter we can consider the resistances R9 = R11 and R10= R8 and the capacitances C5=C6.

The transfer function can be simplified and described in the equation as follows:

$$Vout = \frac{R9}{R8}(Vb - Va) . \frac{1}{1 + j\omega R9 . C5} \quad (27)$$

The capacitance C5 combined with R9 acts as low pass filter with a cut-off frequency fpLp as described in the equation below:

$$fpLp = \frac{1}{2\pi . R9 . C5} \quad (28)$$

Figure 7. Schematic resolver sine receiver circuit

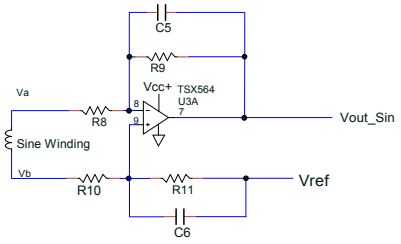
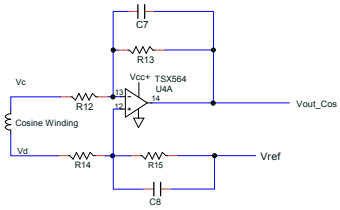


Figure 8. Schematic resolver cosine receiver circuit



In a perfect world the amplitude K.Vr (see Eq. (2) and Eq. (3)) from the sine and cosine path should be equal. This does not count on the following different error terms.

3.1 DC error

The amplitude between the cosine and sine path can be affected by the mismatch of the gain resistance

$$Gain_{error\_sin} = \frac{R9}{R8}(1 \pm 2\varepsilon) \quad (29)$$

ε is the tolerance of the resistance.

Besides, it is important to take into account the fact that Vio of each TSX564 can be different. The maximum possible Vio for the TSX564 is 2.2 mV overtemperature. The DC error is described by the following equation:

$$DC_{error} = \pm Vio\left(1 + \frac{R9}{R8}\right) \quad (30)$$

Please, note that even if in the equation above the null voltage of the resolver and the precision of the Vref are not expressed, in DC error they should be taken into account.

The sine equation can be written as follows, by taking into account the DC error only:

$$Vout_{Sin} = K . A0 . sin\omega t . \frac{R9}{R8} . (1 \pm 2\varepsilon) . sin\theta \pm Vio1\left(1 + \frac{R9}{R8}\right) \quad (31)$$

The cosine equation can be written as follows, by taking into account the DC error only:

$$Vout_{Cos} = K \,.\, A0 \,.\, sin\omega t \,.\, \frac{R13}{R12} \,.\, (1 \pm 2\varepsilon) \,.\, cos\theta \pm Vio2\left(1 + \frac{R13}{R12}\right) \quad (32)$$

3.2 Phase shift error

Another source of error is the phase shift. In the Section 2 Signal conditioning to drive the reference winding we can notice that a phase shift φ1 is introduced by the signal conditioning circuitry. We also understand that the resolver itself can introduce a phase shift φ2 between the reference excitation signal and the sine and cosine signal.

The signal conditioning circuitry for sine winding introduce a phase shift φ3 as well. The same behavior affects the cosine path by including a phase shift φ4.

The sine equation can be written as follows, by taking into account the phase shift error only.

$$Vout_{Sin} = K \,.\, A0 \,.\, \frac{R9}{R8} \,.\, \sin\left(\omega t + \varphi 1 + \varphi 2 + \varphi 3\right) \,.\, sin\theta \quad (33)$$

with

$$\varphi 3 = \; - Atan\,(R9 \,.\, C5 \,.\, \omega) \quad (34)$$

Due to the mismatch of external component (capacitor and resistance) the cosine equation can be written as follows, by taking into account the phase shift error only.

$$Vout_{cos} = K \,.\, A0 \,.\, \frac{R13}{R12} \,.\, \sin\left(\omega t + \varphi 1 + \varphi 2 + \varphi 4\right) \,.\, cos\theta \quad (35)$$

with

$$\varphi 4 = \; - Atan\,(R13 \,.\, C7 \,.\, \omega) \quad (36)$$

The used resolver has a transformation ratio K of 0.54. As the reference winding is driven with 7.5 Vrms (10.6 Vp), it means that the signal on the sin and cos winding is equal to 4.05 Vrms (5.73 Vp).

The goal of the receiver circuit in our application is to adapt this signal from the sin/cos winding for digital analysis done by an ADC. The signal on the Vout must be in the range of 5 V.

Due to the Eq. (27) we can first divide the signal, thanks to R9, R8 (R10 , R11 as well). In order to take margin and avoid any saturation when we work close to the rail, take a full range of 4.5 Vpp.

So, apply a division factor of 2.55. By considering R8=R10=10 kΩ, the R9=R11=3.9 kΩ

The working frequency is still fixed at 4 kHz; in order not to add too much phase shifting, apply the same cut-off frequency than the driver circuit 160 kHz

Thanks to the Eq. (28) C6=C5=255 pF.

The Vref voltage can be set to 2.6 V in order to have a Vout in the range of [350 mV: 4.85 V].

Figure 9. Application schematic for sine receiver circuit

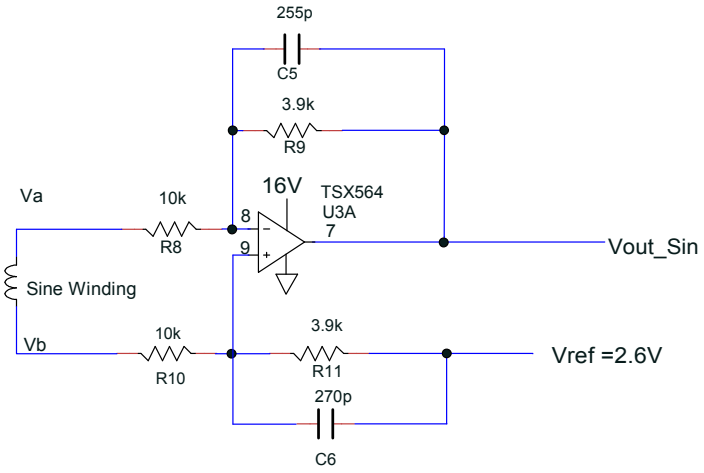
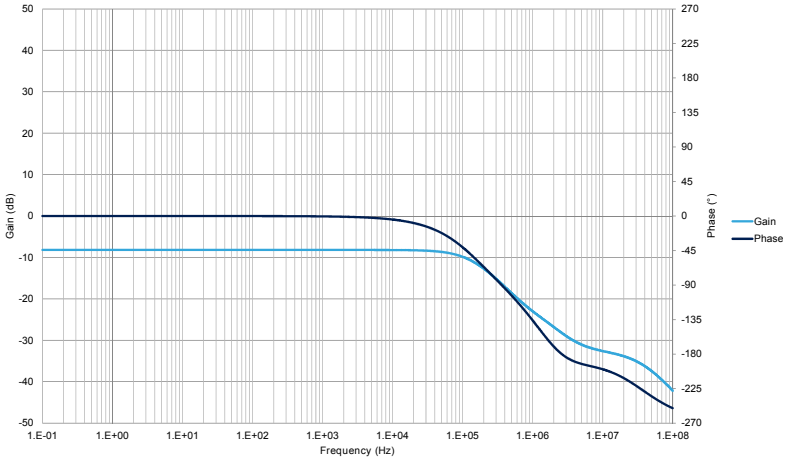


Figure 10. Gain and phase shift vs frequency of receiver circuit

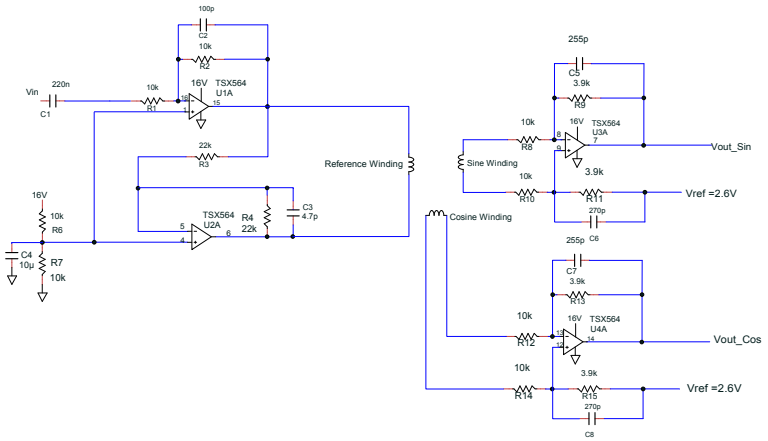


With a cut-off frequency of 160 kHz, it introduces a phase shifting of 2° at 4 kHz (theoretical value -Atan (R9.C5.ω) is 1.5°).

4 Conclusion

The overall application of a system using a resolver can be described in the figure below, where the TSX564 op-amp is used to drive sin/cos signal conditioning.

Figure 11. Application schematic of driver and receiver circuit



The overall equation of such a system can be written by taking into account both the error DC and phase shift.

From Eq. (31) and Eq. (33), the Vout_sin can be written as follows:

$$Vout_{Sin} = K \,.\, A0 \,.\, \frac{R9}{R8} \,.\, (1 \pm 2\varepsilon) \,.\, \sin(\omega t + \varphi 1 + \varphi 2 + \varphi 3) \,.\, sin\theta \pm Vio1\left(1 + \frac{R9}{R8}\right) \quad (37)$$

From Eq. (32) and Eq. (35), the Vout_cos can be written in the following manner:

$$Vout_{cos} = K \,.\, A0 \,.\, \frac{R13}{R12} \,.\, (1 \pm 2\varepsilon) \,.\, \sin(\omega t + \varphi 1 + \varphi 2 + \varphi 4) \,.\, cos\theta \pm Vio2\left(1 + \frac{R13}{R12}\right) \quad (38)$$

In the previous equation the null offset of the resolver is not mentioned and the error due to DC offset can be minimized by choosing a resolver with a small residual offset. The phase shifting φ1 and φ2 introduced by the analog driving circuit and resolver respectively can be corrected by software by advancing the phase of the reference signal.

Thanks to its current capability and high Vcc supply the TSX564 is a good candidate to drive resolver and condition the signal from the sine and cosine winding.

In its quad version it is able to sustain high power dissipation

Revision history

Table 1. **Document revision history**

Date	Version	Changes
10-May-2018	1	Initial release.

Contents

List of figures