AN4898
Application note

Self–test performances

Introduction

This application note compares self–test performances of some 32 bit – automotive microcontrollers designed for Chassis&Safety, PowerTrain and Body applications for different ASIL systems.

The devices mentioned in this document are:

- SPC58NE84xx (40 nm – Power Train – ASIL D)
- SPC584Cxx (40 nm – Body – ASIL B)
- SPC582Bxx (40 nm – Body – ASIL B)
- SPC574K72xx (55 nm – Power Train – ASIL D)
- SPC570S50Ex (55 nm – Chassis&Safety ASIL D)
- SPC574S60xx (55 nm – Chassis&Safety ASIL D)

For each device, this document describes which self–tests are implemented and the recommended configuration.

The reader has clear understanding about the usage of self–tests. For this purpose, specific literatures, such as AN4551 and the reference manuals may help.

Note: ST can change the performance parameters stated in this document, including timing and coverage without informing the customer. The user shall consider as official values the ones described in the RM or DS.

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1 Acronyms

Table 1. Acronyms

Acronym	Meaning
STCU	Self–Test Control Unit
SSCM	System Status and Configuration Module
Seq. mode	Sequential mode
Par. mode	Parallel mode
RGM	Reset Generation Module
SSCM	System Status and Configuration Module

2 Overview

In order to cope with the numerous risks inside a vehicle and then to guarantee its functional safety, STMicroelectronics has developed for the latest generation of SPCxx family some dedicated Built–In Self–Test (BIST).

BISTs are periodic tests used to detect latent faults in the device and to guarantee the integrity of the safety mechanisms according to the ISO26262 standard.

These microcontrollers embed two different types of BISTs:

- Memory BIST (MBIST) for all volatile memories
- Logic BIST (LBIST) for digital logic

STCU is the module that runs the self–test and report their result.

In the previous generation of microcontroller, the hardware starts the execution of the self–test during the boot phase.

55 nm and 40 nm devices, however, provide additional configuration to satisfy the used needs in terms of different parameters (for example diagnostic coverage, execution time and consumption). In these devices the software – and not only the hardware – can trigger the BIST execution.

In such a way, the user can develop complex self–test strategy in which some BISTs run during the key–on and others during the key–off.

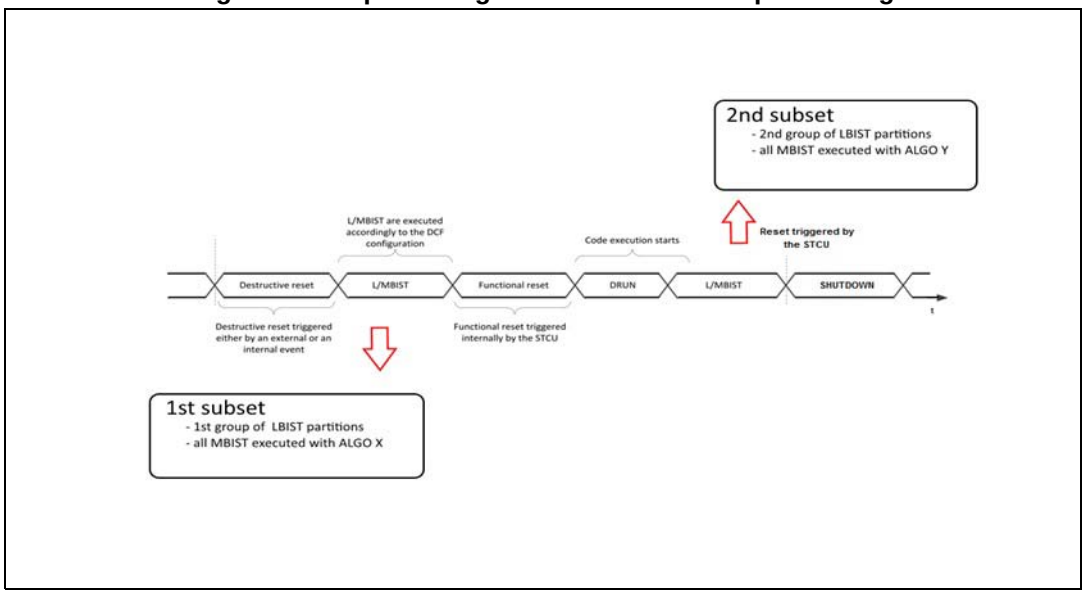
If a self–test runs during both boot phases, it is an off–line test; if it runs during run time it is an online test.

User can split self–tests in two different temporal windows in order not to compromise the requirement of the maximum duration of the start–up phase. For example, some BIST partitions can run during the boot phase and the remaining ones by software during run time before the power–off event.

Of course this methodology increases the complexity of the software architecture.

Figure 1 shows an example about how the BIST (LBIST + MBIST) can be split in 2 subsets:

Figure 1. Temporal diagram about L/MBISTs performing



In this case, the STCU runs the MBIST twice, but with different algorithms. LBIST are split in two groups that STCU executes in two different moments.

The user can customize:

1. when BIST can run
   - during the Booth phase and/or
   - run time
2. how BIST can run
   - concurrent (parallel) or
   - sequential mode

In the first case the current consumption is huge, against a lower execution time (Vice versa in the second case).

In practice, a good trade–off between time execution, and consumption has to be reached.

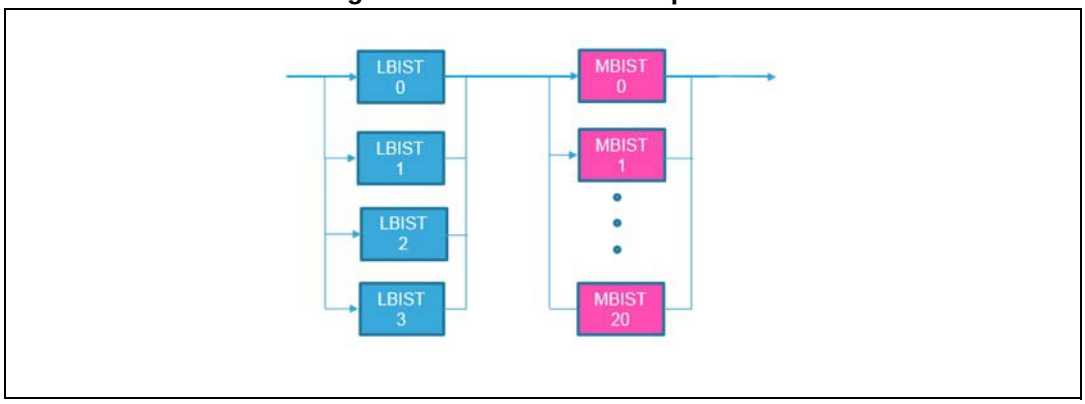
3. at which frequency

User can increase or decrease the frequency of the clock during the BIST depending on the max current provided by the voltage regulator.

Figure 2 and *Figure 3* show some example about how the BIST can run.

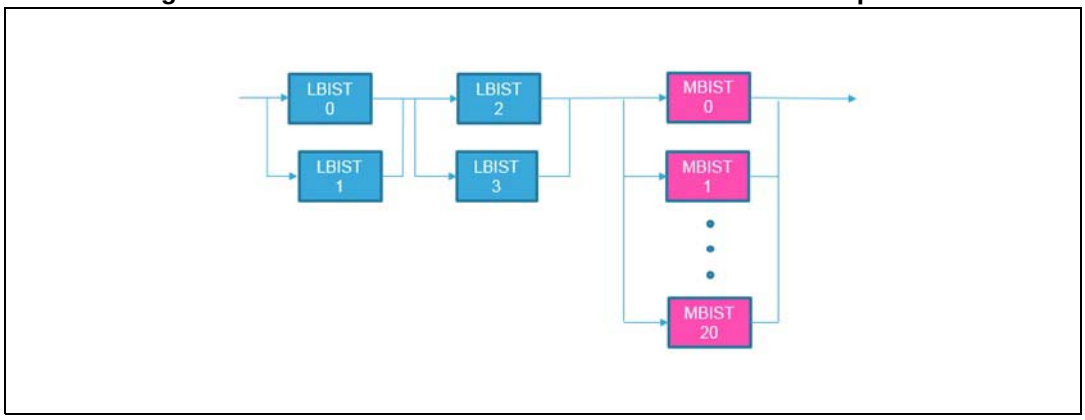
In *Figure 2*, all LBIST and all MBIST run in parallel mode.

Figure 2. LBIST + MBIST in parallel



In *Figure 3* LBIST are performed in parallel in group of two, while the whole MBIST are performed in parallel.

Figure 3. LBIST0 // LBIST1 + LBIST2 //LBIST3 + MBIST in parallel



The next paragraphs list the main parameters and characteristics of self–test for different devices (for example memories size, cores and so on…).

Considered devices are:

- SPC58NE84xx (40 nm – Power Train – ASIL D)
- SPC584Cxx (40 nm – Body – ASIL B)
- SPC582Bxx (40 nm – Body – ASIL B)
- SPC574K72xx (55 nm – Power Train – ASIL D)
- SPC570S50Ex (55 nm – Chassis&Safety ASIL D)
- SPC574S60xx (55 nm – Chassis&Safety ASIL D)

Before entering in details of each device discussed in this document, this table shows the main differences in terms of LBIST/MIST partition, offline and online test and frequency setup.

Table 2. LBIST/MBIST comparison

		LBIST		MBIST	Offline			Online		
Family	**Device**	**N. partition**	**Max N. patterns(1)**	**N. partition**	**Max MBIST freq**	**Max LBIST freq**	**PLL**	**Max MBIST freq**	**Max LBIST freq**	**PLL (sys_clock)**
40 nm	SPC58NE84xx	7	5000	101	100 Mhz	100 Mhz (LBIST0 only)	PLL0	180 Mhz	50 Mhz	PLL0
	SPC582Bxx	n.a	n.a	9	16 Mhz	n.a	PLL0	n.a	n.a	n.a
	SPC584Cx	n.a	n.a	57	170 Mhz	n.a	PLL0	n.a	n.a	n.a
55 nm	SPC574K72xx	8	4000	42	40 Mhz	20 Mhz	PLL0	160 Mhz	20 Mhz	PLL1
	SPC570S50Ex	3	2000	9	16 Mhz	80 Mhz	PLL1	n.a	n.a	n.a
	SPC574S60xx	4	5000	21	128 Mhz	35 Mhz	PLL1	35 Mhz	35 Mhz	PLL1

1. Typical value guaranteed by designer

All devices do not have both LBIST and MBIST.

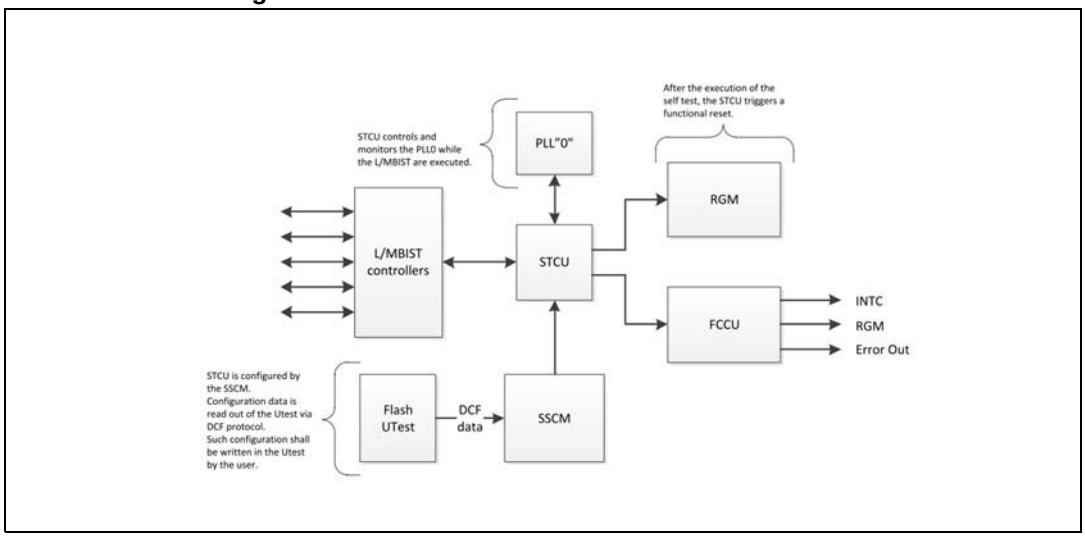
3 Offline and online setup

3.1 Offline setup

This is the general scheme related to modules involved in self–test execution configured in off–line mode

PLL and max frequency are device dependent (see *Figure 4*).

Figure 4. Module interconnections in offline mode



Offline self–test runs at the start–up driven by the STCU whose configuration is loaded by the SCCM from UTest sector.

The PLL0 (or PLL1, this is hardware design) provides the clock during the execution of the offline self–test. The STCU configures it.

The STCU forwards any LBIST/MBIST failure to the FCCU which takes the proper action.

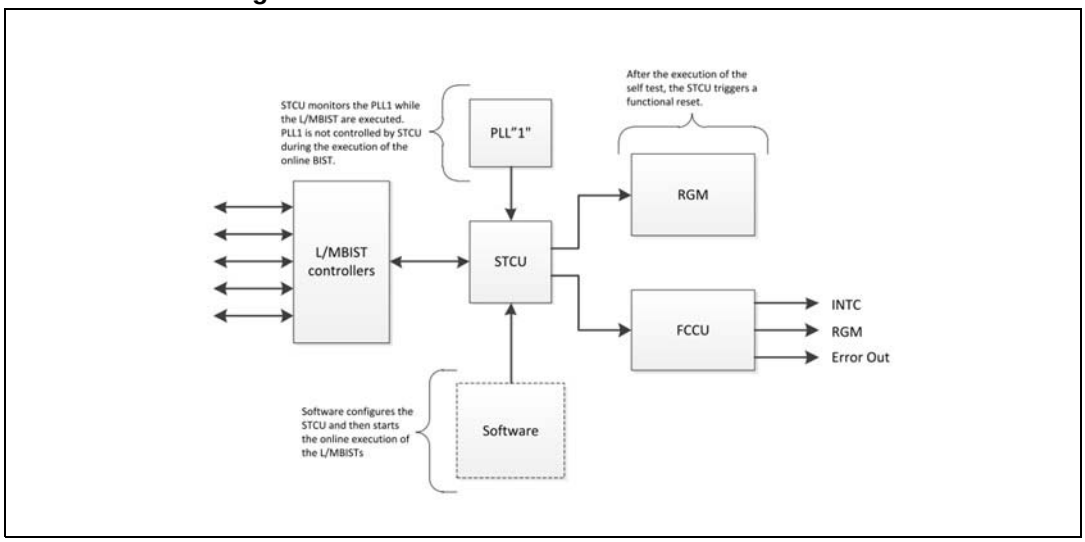
STCU is also connected to the RGM. After the LBIST execution a functional reset is triggered.

3.2 Online setup

In this case the involved modules are:

- the Reset Generation Module (RGM)
- the Self–Test Control Unit (STCU2)
- the Fault Collection and Control Unit (FCCU)
- L/MBIST controllers
- PLL"1" or PLL"0" as sys_clock

Figure 5. Module interconnections in online mode



The online self–test is initiated by the software code which provides the proper commands to the STCU via IPS interface.

In online mode, the action of STCU is limited to PLL lock signal monitoring[a]. In this case, reference clock for self–test execution is the system clock, which means the same used by the application.

Depending on the CGM configuration, either the PLL0 or the PLL1 can drive the LBIST/MBIST[b]. *Figure 5* assumes PLL1 has been selected.

STCU reports BIST errors to the RGM and the FCCU modules.

a. During the online self–test, the STCU monitors the lock signals of the PLL1/0 which in a standard use case drives the system clock.

b. In offline mode only PLL0 can be used.

4 Self–test for device

This chapter describes what self–tests are available in the 55 nm and 40 nm of microcontrollers listed below. In addition it provides the typical self–test configuration.

4.1 SPC584Cxx

It belongs to 40 nm's family for ASILB application.

The volatile memories of this device are split in partitions. User can decide which partition to test according to the number associated to it.

In this device only the self–test on the memories (MBIST) is available.

On cut 1.0 version, there are 57 MBIST that can run in offline mode.

4.1.1 MBIST partitions

Table 3. MBIST partitions

M_BIST partition	Memory mapped	M_BIST partition	Memory mapped
0	rom_bar	29	ram_zxa_dcache_2
1	rom_mpflash	30	ram_zxa_dcache_3
2	ram_mpflash	31	ram_zxa_dtag
3	ram_fec_rx_0_even	32	hsm_pram_0
4	ram_zxc_dmem_0	33	hsm_pram_1_0
5	ram_zxc_dmem_1	34	hsm_pram_1_1
6	ram_zxc_icache_0	35	ram_hsm_icache_0
7	ram_zxc_icache_1	36	ram_hsm_icache_1
8	ram_zxc_icache_2	37	ram_hsm_itag_0
9	ram_zxc_icache_3	38	ram_hsm_itag_1
10	ram_zxc_itag	39	ram_hsm_c3
11	ram_dma_1	40	ram_flexray_dram_0
12	ram_sram_2_0_0	41	ram_flexray_lram_0
13	ram_sram_2_0_1	42	ram_fec_rx_0_odd
14	ram_sram_2_1	43	ram_fec_tx_0_odd
15	ram_sram_2_2	44	ram_sram_2_4
16	ram_sram_2_3	45	ram_sram_2_5
17	ram_can_0	46	ram_sram_2_6
18	ram_can_1	47	ram_sram_2_7
19	ram_fec_tx_0_even	48	ram_sram_3_0
20	ram_zxa_dmem_0	49	ram_sram_3_1
21	ram_zxa_dmem_1	50	ram_sram_3_2

Table 3. MBIST partitions (continued)

M_BIST partition	Memory mapped	M_BIST partition	Memory mapped
22	ram_zxa_icache_0	51	ram_sram_3_3
23	ram_zxa_icache_1	52	ram_zxc_dcache_0
24	ram_zxa_icache_2	53	ram_zxc_dcache_1
25	ram_zxa_icache_3	54	ram_zxc_dcache_2
26	ram_zxa_itag	55	ram_zxc_dcache_3
27	ram_zxa_dcache_0	56	ram_zxc_dtag
28	ram_zxa_dcache_1		

4.1.2 Typical self–test configurations

Table 4. SPC584Cxx typical self–test configurations

Configuration	Offline/Online	Freq. setup	Time [ms]
all MBIST in parallel (Auto test 18N algorithm)	Offline	50 Mhz	6.59 msec
all MBIST in parallel (Full algorithm)	Offline	180 Mhz	5.9 msec

See AN 4684 for further details.

In this case, although the online self–test runs at frequency much higher than in offline case, the timing of the two cases of *Table 4* is practically the same. Below, the details for MBIST algorithm:

- Autotest 18N algorithm:

it verifies the presence of multi bit errors in the RAM arrays

- Full algorithm:

it verifies the integrity of the RAM address logic and check also for the presence of the multi bit errors in the RAM (autotest algorithm).

4.2 SPC58NE84xx

It belongs to 40 nm's family for ASILD application.

In the last version of the device, (cut 2.0) 7 LBIST and 101 MBIST are available in both offline and online modes.

4.2.1 MBIST partitions

Table 5. MBIST partitions

M_BIST partition	Memory Mapped	M_BIST partition	Memory Mapped	M_BIST partition	Memory Mapped
19	ram_zxa_imem	32	hsm_pram_0	40	ram_flexray _dram_0
21	ram_zxa_dmem_0	34	hsm_pram_1_0	41	ram_flexray _lram_0
20	ram_zxa_dmem_1	33	hsm_pram_1_1	18	ram_can_0
25	ram_zxa_icache_0	36	ram_hsm_icache_0	17	ram_can_1
24	ram_zxa_icache_1	35	ram_hsm_icache_1	86	ram_gtm_fifo
23	ram_zxa_icache_2	38	ram_hsm_itag_0	89	ram_gtm _ram0_0
22	ram_zxa_icache_3	37	ram_hsm_itag_1	88	ram_gtm _ram0_1
30	ram_zxa_dcache_0	39	ram_hsm_c3	87	ram_gtm _ram0_2
29	ram_zxa_dcache_1	60	ram_sram_0_0	91	ram_gtm _ram0_3
28	ram_zxa_dcache_2	59	ram_sram_0_1	90	ram_gtm _ram0_4
27	ram_zxa_dcache_3	58	ram_sram_0_2	94	ram_gtm _ram1_0
26	ram_zxa_itag	57	ram_sram_0_3	93	ram_gtm _ram1_1
31	ram_zxa_dtag	53	ram_sram_1_0	92	ram_gtm _ram1_2
61	ram_zxb_imem	52	ram_sram_1_1	96	ram_gtm _ram1_3
63	ram_zxb_dmem_0	51	ram_sram_1_2	95	ram_gtm _ram1_4
62	ram_zxb_dmem_1	50	ram_sram_1_3	97	ram_gtm_dpll _ram1a
67	ram_zxb_icache_0	54	ram_sram_1_4	98	ram_gtm_dpll _ram1b
66	ram_zxb_icache_1	12	ram_sram_2_0_0	99	ram_gtm_dpll _ram2
65	ram_zxb_icache_2	13	ram_sram_2_0_1	85	ram_nexus _nar_0
64	ram_zxb_icache_3	16	ram_sram_2_1	84	ram_nexus _nar_1

Table 5. MBIST partitions (continued)

M_BIST partition	Memory Mapped	M_BIST partition	Memory Mapped	M_BIST partition	Memory Mapped
72	ram_zxb_dcache_0	15	ram_sram_2_2	83	ram_nexus _nar_2
71	ram_zxb_dcache_1	14	ram_sram_2_3	82	ram_nexus _nar_3
70	ram_zxb_dcache_2	49	ram_sram_2_4	81	ram_amu
69	ram_zxb_dcache_3	48	ram_sram_2_5	2	ram_mpflash
68	ram_zxb_itag	47	ram_sram_2_6	0	rom_bar
73	ram_zxb_dtag	46	ram_sram_2_7	1	rom_mpflash
3	ram_zxc_imem	56	ram_sram_3_0	42	ram_dwc_eth0 _tx_odd
5	ram_zxc_dmem_0	55	ram_sram_3_1	43	ram_dwc_eth0 _tx_even
4	ram_zxc_dmem_1	80	ram_overlay_0_0	44	ram_dwc_eth0 _rx_odd
9	ram_zxc_icache_0	79	ram_overlay_0_1	45	ram_dwc_eth0 _rx_even
8	ram_zxc_icache_1	101	ram_overlay_1_0	76	ram_dwc_eth1 _tx_even
7	ram_zxc_icache_2	100	ram_overlay_1_1	75	ram_dwc_eth1 _tx_odd
6	ram_zxc_icache_3	74	ram_dma_0	78	ram_dwc_eth1 _rx_even
10	ram_zxc_itag	11	ram_dma_1	77	ram_dwc_eth1 _rx_odd

4.2.2 LBIST partitions

Table 6. LBIST partitions

lbist_partition_0	lbist_ partition _1	lbist_ partition _2	lbist_ partition _3	lbist_ partition _4	lbist_ partition _5	lbist_ partition _6
acp_comp_bridge_ S6_lmem	gtm	hsm	cansubsys _1	psi5_1	platform	cansubsys_0
acp_comp_bridge_ S7_lmem	–	flash_0	flexray_0	ethernet_0	–	dma_ch_mux_ 1_checker
acp_comp_bridge_ dma_m4	–	sent_0	memu	adcsar_dig_2	–	dma_ch_mux_ 0_checker

Table 6. LBIST partitions (continued)

lbist_partition_0	lbist_partition_1	lbist_partition_2	lbist_partition_3	lbist_partition_4	lbist_partition_5	lbist_partition_6
acp_comp_bridge_sipi_m5	–	sent_1	emios_1	linflex_0	–	dma_ch_mux_2_checker
acp_comp_iahb_gskt_aips0	–	emios_0	psi5_s_0	adcsar_dig_3	–	dma_ch_mux_3_checker
acp_periph_bridge_concentr8tor_0	–	psi5_0	fccu	adcsar_seq_1	–	dma_ch_mux_4_checker
acp_periph_bridge_concentr8tor_1	–	dspi_4	ethernet_1	adcsar_seq_2	–	dma_ch_mux_5_checker
acp_periph_bridge_concentr8tor_2	–	dspi_5	adcsd_ana_1	adcsar_seq_b	–	dma_ch_mux_0
acp_periph_bridge_m5	–	–	adcsd_ana_3	adcsar_seq_0	–	dma_ch_mux_1
acp_periph_bridge_s6	–	–	adcsd_ana_2	adcsar_seq_3	–	dma_ch_mux_2
acp_periph_bridge_s7_tcm_gskt	–	–	adcsd_ana_5	iic_0	–	dma_ch_mux_3
acp_periph_iahb_gskt_aips1	–	–	adcsd_ana_4	dspi_0	–	dma_ch_mux_4
acp_periph_iahb_gskt_aips2	–	–	adcsd_ana_0	dspi_9	–	dma_ch_mux_5
ahb_edc_after_ecc_mstr_gskt_sipi	–	–	crc_0	dspi_1	–	–
ahb_smpu2_mon	–	–	crc_1	dspi_2	–	–
ahb_smpu2_mon_0	–	–	body_ctu_0	dspi_3	–	–
aic0	–	–	fosu	dspi_8	–	–
aic1	–	–	cmu_2_hpbm	dspi_7	–	–
aic2	–	–	cmu_13_pfbridge	dspi_6	–	–
comp_checker_rccu_intc_or_glue_1	–	–	cmu_7_sent	adcsar_dig_1	–	–
comp_checker_rccu_intc_or_glue_2	–	–	cmu_11_fbridge	linflex_13	–	–
comp_chka_mirq_checker_delay	–	–	bam	linflex_10	–	–
comp_chkc_mirq_checker_delay	–	–	adcsd_dig_2	linflex_4	–	–
dmc_zxb_dbus	–	–	adcsd_dig_4	linflex_6	–	–

Table 6. LBIST partitions (continued)

lbist_partition_0	lbist_partition_1	lbist_partition_2	lbist_partition_3	lbist_partition_4	lbist_partition_5	lbist_partition_6
ips_e2e_edc_slv_gskt_aips0	–	–	adcsd_dig_5	linflex_1	–	–
ips_e2e_edc_slv_gskt_aips1	–	–	adcsd_dig_1	linflex_14	–	–
ips_e2e_edc_slv_gskt_aips2	–	–	adcsd_dig_0	linflex_15	–	–
lb0_interface_dummy	–	–	adcsd_dig_3	linflex_16	–	–
periph_shell_xbic_ahb	–	–	–	linflex_17	–	–
pflash_cal_overlay	–	–	–	linflex_7	–	–
pflash_cal_overlay_0	–	–	–	linflex_5	–	–
pflash_fl_ecc	–	–	–	linflex_3	–	–
pflash_fl_ecc_0	–	–	–	inflex_9	–	–
pram_e2e_ecc_edc	–	–	–	linflex_12	–	–
pram_e2e_ecc_edc_0	–	–	–	linflex_11	–	–
pram_e2e_ecc_edc_1	–	–	–	linflex_2	–	–
pram_e2e_ecc_edc_2	–	–	–	linflex_8	–	–
pram_e2e_ecc_safety_mon	–	–	–	adcsar_dig_0	–	–
pram_e2e_ecc_safety_mon_0	–	–	–	adcsar10_dig_0	–	–
pram_e2e_ecc_safety_mon_1	–	–	–	adcsar10_dig_1	–	–
pram_e2e_ecc_safety_mon_2	–	–	–	pit_rti_0	–	–
rccu_aips0_ecc	–	–	–	fr_rom_1	–	–
rccu_aips1_ecc	–	–	–	fr_rom_0	–	–
rccu_aips2_ecc	–	–	–	ips_read_mux_2	–	–
rccu_dma0	–	–	–	adcsar_10bit_seq_0	–	–
rccu_dma1	–	–	–	adcsar_10bit_seq_1	–	–

Table 6. LBIST partitions (continued)

lbist_partition_0	lbist_partition_1	lbist_partition_2	lbist_partition_3	lbist_partition_4	lbist_partition_5	lbist_partition_6
rccu_dma_ch_mux_0	–	–	–	ima	–	–
rccu_dma_ch_mux_1	–	–	–	ips_read_mux_1	–	–
rccu_dma_ch_mux_2	–	–	–	intg_ima_read mux_top	–	–
rccu_dma_ch_mux_3	–	–	–	pit_rti_1	–	–
rccu_dma_ch_mux_4	–	–	–	cmu_0_pll0_xoc_ircosc	–	–
rccu_dma_ch_mux_5	–	–	–	cmu_4_gtm	–	–
rccu_dmc_zxa	–	–	–	cmu_12_emios	–	–
rccu_dmc_zxc	–	–	–	cmu_10_psi5_1us	–	–
rccu_intc	–	–	–	cmu_5_sdadc	–	–
rccu_zxd	–	–	–	cmu_3_pbridge	–	–
rccu_zxd_dtcm	–	–	–	cmu_9_psi5_f125	–	–
rccu_zxd_intc_if	–	–	–	cmu_8_psi5_f189	–	–
rccu_zxf	–	–	–	cmu_6_saradc	–	–
rccu_zxf_dtcm	–	–	–	cmu_1_core_xbar_bd	–	–
rccu_zxf_intc_if	–	–	–	adcsar_ana_wrap_2	–	–
u_zxb_dahb_masterid_mon	–	–	–	adcsar_ana_wrap_3	–	–
u_zxb_iahb_masterid_mon	–	–	–	adcsar_ana_wrap_0	–	–
xbic_ahb_comp	–	–	–	adcsar_ana_wrap_1	–	–
zxa_dc_data0_fb_chk	–	–	–	adcsar_ana_wrap_b	–	–
zxa_dc_data1_fb_chk	–	–	–	adcsar_ana_wrap_comp_0	–	–
zxa_dc_data2_fb_chk	–	–	–	adcsar_ana_wrap_comp_1	–	–

Table 6. LBIST partitions (continued)

lbist_partition_0	lbist_ partition _1	lbist_ partition _2	lbist_ partition _3	lbist_ partition _4	lbist_ partition _5	lbist_ partition _6
zxa_dc_data3 _fb_chk	–	–	–	adcsar_bias	–	–
zxa_dc_tag_fb_chk	–	–	–	adcsd_bias	–	–
zxa_dtcm0_fb_chk	–	–	–	adcsar_dig_b	–	–
zxa_dtcm1_fb_chk	–	–	–	–	–	–
zxa_ic_data0 _fb_chk	–	–	–	–	–	–
zxa_ic_data1 _fb_chk	–	–	–	–	–	–
zxa_ic_data2 _fb_chk	–	–	–	–	–	–
zxa_ic_data3 _fb_chk	–	–	–	–	–	–
zxa_ic_tag_fb_chk	–	–	–	–	–	–
zxa_itcm_fb_chk	–	–	–	–	–	–
zxb_dc_data0 _fb_chk	–	–	–	–	–	–
zxb_dc_data1 _fb_chk	–	–	–	–	–	–
zxb_dc_data2 _fb_chk	–	–	–	–	–	–
zxb_dc_data3 _fb_chk	–	–	–	–	–	–
zxb_dc_tag_fb_chk	–	–	–	–	–	–
zxb_dtcm0_fb_chk	–	–	–	–	–	–
zxb_dtcm1_fb_chk	–	–	–	–	–	–
zxb_ic_data0 _fb_chk	–	–	–	–	–	–
zxb_ic_data1 _fb_chk	–	–	–	–	–	–
zxb_ic_data2 _fb_chk	–	–	–	–	–	–
zxb_ic_data3 _fb_chk	–	–	–	–	–	–
zxb_ic_tag_fb_chk	–	–	–	–	–	–
zxb_itcm_fb_chk	–	–	–	–	–	–
zxc_dtcm0_fb_chk	–	–	–	–	–	–
zxc_dtcm1_fb_chk	–	–	–	–	–	–

Table 6. LBIST partitions (continued)

lbist_partition_0	lbist_ partition _1	lbist_ partition _2	lbist_ partition _3	lbist_ partition _4	lbist_ partition _5	lbist_ partition _6
zxc_ic_data0 _fb_chk	–	–	–	–	–	–
zxc_ic_data1 _fb_chk	–	–	–	–	–	–
zxc_ic_data2 _fb_chk	–	–	–	–	–	–
zxc_ic_data3 _fb_chk	–	–	–	–	–	–
zxc_ic_tag_fb_chk	–	–	–	–	–	–
zxc_itcm_fb_chk	–	–	–	–	–	–

4.2.3 Typical self–test configurations

Table 7. SPC58NE84xx self–test configurations

Configuration	Offline/ Online	Freq. setup	N. Patterns	Time [ms]
L0 + all MBIST in parallel	Offline	100 Mhz	5000	16.7
all MBIST in parallel (full algorithm)	Online	180 Mhz	–	6.2
L1 + L2 + L3 + L4 + L5 + L6 (sequential mode)	Online	35 Mhz	5000	2.3

In online mode, it suggests to run the logic BIST in sequential mode.

4.3 SPC582Bxx

It belongs to 40 nm's family for ASILB application.

In the last version of the device (cut 1.0), 10 MBIST are available in offline mode only.

4.3.1 MBIST partitions

Table 8. MBIST partitions

M_BIST partition	Memory mapped
0	ram_sram_2_0_0
1	ram_sram_2_0_1
2	ram_sram_2_1
3	ram_sram_2_2
4	ram_dma_0
5	ram_cansubsys_0

Table 8. MBIST partitions (continued)

M_BIST partition	Memory mapped
6	ram_cansubsys_1
7	ram_mpflash
8	rom_bam
9	rom_mpflash

4.3.2 Typical self–test configuration

Table 9. SPC582Bxx typical self–test configurations

Configuration	Offline/Online	Freq. setup	Time [ms]
all MBIST in parallel	Offline	IRC	1.91

4.4 SPC574K72xx

It belongs to 55 nm's family for ASILD application. For self–test, logic and memory part of the device are divided in partition. User can decide which partition to test according to the number associated to it.

On cut 2.3 version, 8 LBIST and 41 MBIST are available in both offline and online modes.

4.4.1 LBIST partitions

Table 10. LBIST partitions

LBIST partition	Instance name
LBIST0 – checker core	Checker core (Core 0 – checker)
	RCCU and delay logic
LBIST1 – IOP core	IOP core (Core 2)
	INTC
	STM
	SWT
LBIST2 – Peripheral shell	AHB–MPU
	PBRIDGE_A
	PBRIDGE_B
	PIT_0
	PIT_1
	CAN RAM
	CAN
	FCCU

Table 10. LBIST partitions (continued)

LBIST partition	Instance name
LBIST3 – Computational shell	AHB–MPU
	PRAMC
	RAM
	PFLASHC
	Flash memory
	RAM overlay
	MEMU
LBIST4 – Peripheral shell masters	eDMA
	DMACHMUX
	DMA TCD RAM
	FEC
	RAM FEC
	FlexRay
	SIPI
LBIST5 – Peripherals	SDADC
	SARADC
	BAM ROM
	CRC
	DSPI
	IIC
	PSI5
	SENT
	REG_PROT
LBIST6 – GTM	GTM
	GTM RAM
LBIST7 – Safety core	Master core (Core0)
	Instruction cache
	Data cache
	INTC
	STM
	SWT

4.4.2 MBIST partitions

Table 11. MBIST partitions

MBIST partition	Memory mapped
MBIST0	Main Core I–MEM
MBIST1	Main Core D–MEM
MBIST2	–
MBIST3	Main Core I–CACHE
MBIST4	–
MBIST5	–
MBIST6	–
MBIST7	Main Core D–CACHE
MBIST8	–
MBIST9	–
MBIST10	–
MBIST11	Main Core I–TAG
MBIST12	Main Core D–TAG
MBIST13	Overlay RAM
MBIST14	–
MBIST15	IOP Core I–MEM
MBIST16	–
MBIST17	IOP Core D–MEM
MBIST18	–
MBIST19	DMA RAM
MBIST20	FLEXRAY D–RAM
MBIST21	FLEXRAY L–RAM
MBIST22	TTCAN RAM
MBIST23	GTM FIFO
MBIST24	GTM (MCS2)–RAM0
MBIST25	GTM (MCS1)–RAM0
MBIST26	GTM (MCS0)–RAM0
MBIST27	GTM (MCS2)–RAM1
MBIST28	GTM (MCS1)–RAM1
MBIST29	GTM (MCS0)–RAM1
MBIST30	GTM DPLL–1A
MBIST31	GTM DPLL–1B
MBIST32	GTM DPLL–2

Table 11. MBIST partitions (continued)

MBIST partition	Memory mapped
MBIST33	SRAM
MBIST34	NAR
MBIST35	–
MBIST36	–
MBIST37	–
MBIST38	FEC FIFO
MBIST39	FEC MIB
MBIST40	FLASH KRYPTON RAM
MBIST41	BAM ROM

4.5 Typical self–test configurations

For this device the self–test configuration is split in two rounds:

1st group during offline (key ON)

2nd group during online (key OFF)

Table 12. SPC574K72xx typical self–test configurations

Configuration	Offline/ Online	Freq. set up	N. patterns	Time [ms]
LBIST1 + LBIST2 + LBIST3 + all MBIST (Auto test 18N algorithm)	Offline	40 Mhz	5000	20.38
LBIST0 + LBIST4 + LBIST5+ LBIST6+LBIST 7 + all MBIST (Full algorithm)	Online	160 Mhz	5000	26.33

4.6 SPC570S50Ex

It belongs to 55 nm's family for ASILD application (Chassis&Safety).

In the last version of the device (cut 2.0), 3 LBIST and 9 MBIST are available only in offline mode.

4.6.1 LBIST partitions

Table 13. LBIST partitions

L_BIST partition	Instance name
LBIST 0	acp_mirq2
	acp_velvety_axbs
	aic1
	aips1
	dma0_ecc
	dma_ch_mux_0
	flash_ctl
	intc_ipi
	pram_ctl
	bist_sram
	ram_sram_0
	ram_sram_1
	spp_dma2
	bist_dma
	ram_dma_0
	stm_ips_2
	swt_ips_2
	zx_core_a
	etimer_2
	etimer_3
	flexcan_1
	linflex_1
	fccu
	fosu
	cmu_1
	cmu_2
	cmu_3
	dspi_2

Table 13. LBIST partitions (continued)

L_BIST partition	Instance name
LBIST1	acp_mirq2_checker
	dma_ch_mux_0_checker
	rccu_dma_ch_mux_0
	intc_ipi_checker
	rccu_dma
	rccu_intc
	rccu_z0
	rccu_z0_ahb
	spp_dma2_checker
	zx_core_d
	dma0_ecc_checker
	rccu_eim_ecc
LBIST2	aips0
	aic0
	flash_0
	etimer_0
	etimer_1
	ctu_0
	adcsar_dig_0
	adcsar_dig_b
	cmu_pll
	linflex_0
	flexcan_0
	dspi_0
	dspi_1
	crc_0
	pit_rti_0
	bam
	bam_rom
	wkpu
	memu

4.6.2 MBIST partitions

Table 14. MBIST partitions

M_BIST partition	Memory mapped
0	ram_sram_1
1	ram_sram_10
2	ram_dma
3	ram_can_rxim_1
4	ram_can_rxim_0
5	ram_can_mb_1
6	ram_can_mb_0
7	ram_mpflash
8	bam_rom

4.6.3 Typical self–test configuration

Table 15. SPC570S50Ex typical self–test configurations

Configuration	Offline/ Online	Freq. set up	N. patterns	Time [ms]
LBIST Only	Offline	16 Mhz	2000	23.7
MBIST Only	Offline	80 Mhz	–	10.4
all LBIST (seq. mode) + all MBIST (par. mode)	Offline	16 Mhz + 80 Mhz	2000	38

4.7 SPC574S60xx

It belongs to 55 nm's family for ASILD application (Chassis&Safety).

In the last version of the device (cut 2.0), 4 LBIST and 21 MBIST are available in both online and offline mode.

4.7.1 LBIST partitions

Table 16. LBIST partitions

LBIST partition	Instance name
LBIST0	CPU 0
	XBAR
	XBIC
	INTC0
	SWT
	FlexRay
	DMA0
	DMA_MUX 0–1
	STM
LBIST1	CPU0_Checker
	INTC0_checker
	DMA0_checkert
	RCCUx
	DMAMUX0–1–checker

Table 16. LBIST partitions (continued)

LBIST partition	Instance name
LBIST2	MCAN0–1
	DSPI
	ADC DIG 0–1–2–3
	CRC
	SWG_PWM1
	FlexPWM0
	ADC SEQ 0–1–2–3
	PSIS5
	MEMU
	AIPS0
	ETMr0–1
	SWG0
	MBIST
	FCCU
	PIT
	AIC0
	CTU0
	SENT0
	MBIST–Collars
	CMU0

Table 16. LBIST partitions (continued)

LBIST partition	Instance name
LBIST3	MCAN 2
	DSPI 1–2–3
	ADC DIG 4–5–6–7
	SWG PWM 3
	SRAM C
	FLexPWM2
	LinFLex1
	ADC SEQ 4–5–6–7
	CMU 1–2–3
	Flashdig
	AIPS1
	ETMR2–3
	SWG1
	MBIST
	Flashc
	AIC1
	CTU1
	SENT 1
	MBIST– Collars

4.7.2 MBIST partitions

Table 17. LBIST partitions

MBIST partition	Memory mapped
0	dmem_0
1	dmem_1
2	icache_0
3	icache_1
4	icache_2
5	icache_3
6	itag
7	dma_ram
8	fray_dram
9	fray_lram–0
10	fray_lram–1

Table 17. LBIST partitions (continued)

MBIST partition	Memory mapped
11	mcan_0
12	mcan_1
13	sram
14	ram_mpflash
15	dcache–0
16	dcache–1
17	dcache–2
18	dcache–3
19	dtag
20	bam_rom

4.7.3 Typical self–test configuration

Table 18. SPC570S60xx typical self–test configurations

Configuration	Offline/Online	Freq. set up	N. patterns	Time [ms]
all MIBIST + all LBIST in parallel	Offline/Online	35 Mhz	5000	17.55
L0//L1 + L2//L3 + MBIST in parallel(1)	Offline/Online	128 Mhz + 16 Mhz	5000	66.35
All LBIST in parallel – 1st half of MBIST parallel + 2nd half of MIST parallel	Offline/Online	128 Mhz + 16 Mhz	5000	42.11
all MIBIST + all LBIST in parallel	Offline/Online	128 Mhz + 16 Mhz	5000	38.06
all MIBIST + all LBIST in sequential	Offline/Online	128 Mhz + 16 Mhz	5000	135.05

1. It is the most recommended by designer

5 Summary

This document is an overview about how and which BIST are available in some devices of the 40 nm and 50 nm family to detect latent faults.

In the latest generations of microcontroller, SPC57xx and SPC58xx, many parameters are configurable. This flexibility permits to perform the self–test in different ways (parallel or sequential mode), at different frequencies and, overall, splitting the self–test performing at different temporal intervals and increasing the final performances.

6 Revision history

Table 19. Document revision history

Date	Revision	Changes
02-Aug-2016	1	Initial release.
13-Jan-2017	2	Added Note in cover page.