AN4999
Application note

STSPIN32F0 overcurrent protection

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Introduction

The STSPIN32F0 device is a system-in-package providing an integrated solution suitable for driving three-phase BLDC motors using different driving modes. One of the integrated features of this device is overcurrent protection, which protects the application against damaging when high currents are reached.

The protection is implemented using an integrated comparator with an adjustable threshold. The overcurrent event can be managed both by the gate driving logic and by the microcontroller, according to user selection.

This document gives an overview of the OC protection feature and explains how to connect the STSPIN32F0 pins in order to implement the desired current threshold.

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1 Overcurrent internal block diagram

An internal block diagram of overcurrent protection is depicted in *Figure 1*. The voltage on the OC_COMP pin is compared with a threshold, selectable by the MCU lines PF6 and PF7 (see *Table 1*). When the threshold is exceeded, the OC comparator forces the output and then the PB12 line of the MCU high. Depending on the status of the OC_SEL signal (see *Figure 1*), the comparator output propagates to the control logic of gate drivers triggering the embedded protection. The OC protection implemented in the gate driving logic turns off the external high side power switches until all the high side driving inputs are low (refer to the STSPIN32F0 device datasheet for more details).

Figure 1. Overcurrent protection block diagram

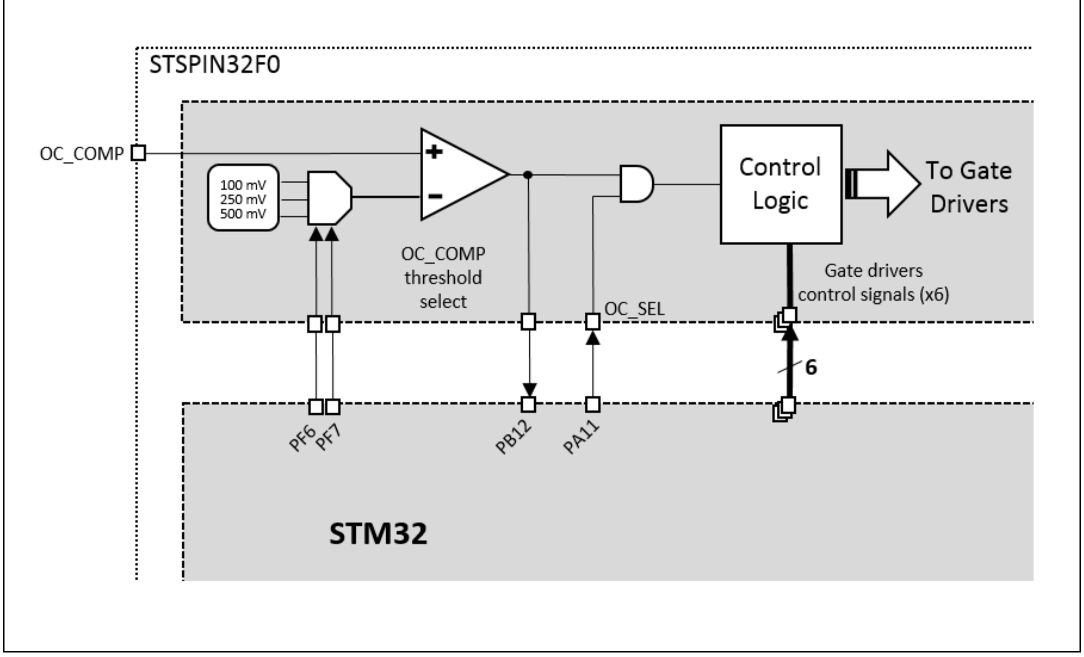


Table 1. OC threshold values

OC_TH_STBY2 (PF6)	OC_TH_STBY1 (PF7)	OC threshold [mV]	Note
0	0	N.A.	Standby mode
0	1	100	-
1	0	250	-
1	1	500	-

2 Overcurrent detection in a single shunt topology

The single shunt topology is shown in *Figure 2*. As a convention, the phases are indicated by letters U, V and W. Each phase of the motor is connected to its output OUTU, OUTV and OUTW driven by a half-bridge. The currents are noted as I_U, I_V, and I_W (positive values imply the current is flowing into the motor phase). The sum of the currents is always equal to zero:

Equation 1

$$I_U + I_V + I_W = 0$$

Currents are measured on a shunt resistor R_S, so the OC_COMP pin is connected directly to it. Therefore, the current flowing in a phase can be measured only when the respective low side MOSFET is turned on. The overall current measured is a combination of I_U, I_V, and I_W as listed in *Table 2*. The value of the current in a phase can be determined using the information coming from the other two phases according to *Equation 1*.

Figure 2. Power stage and OC protection schematic - single shunt

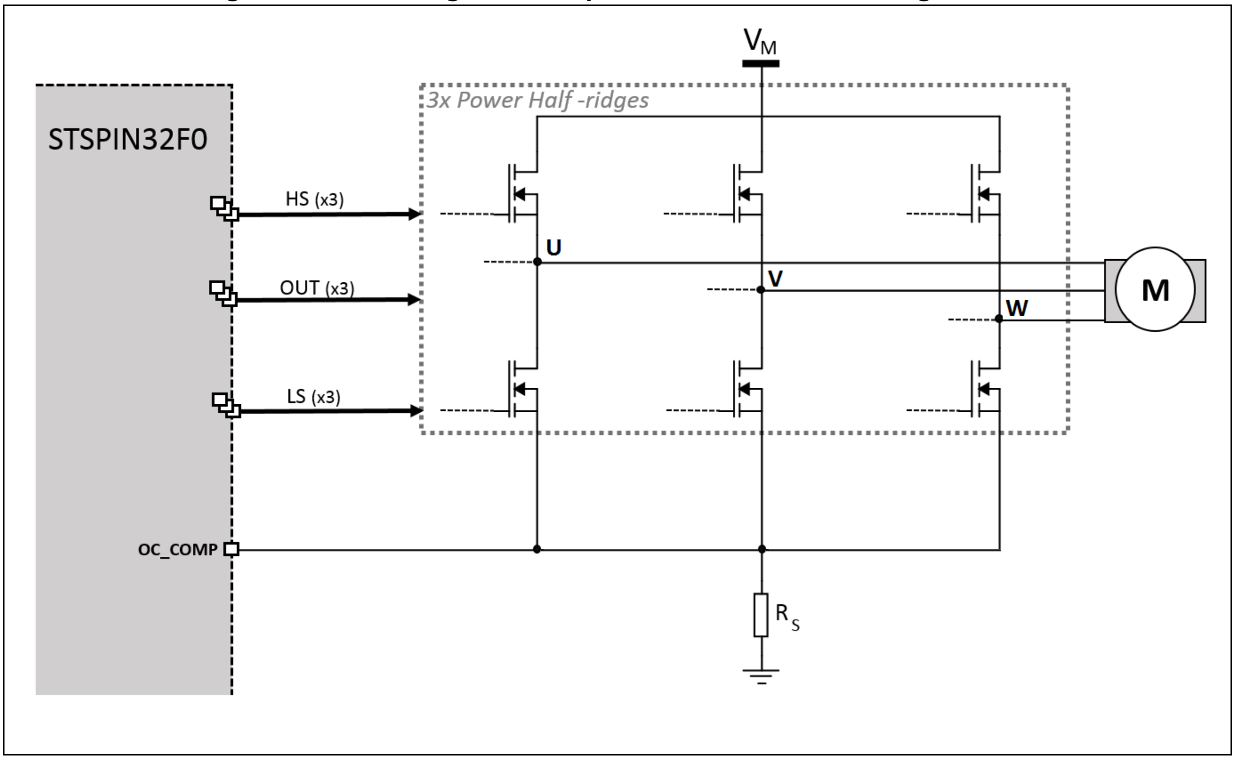


Table 2. Measured current according to power MOSFETs state - single shunt

Power MOSFET turned ON			Measured current on OC_COMP input
Phase U	Phase V	Phase W	
Low side	Low side	Low side	0
Low side	Low side	High side	$(I_U + I_V) \cdot Rs = - I_W \cdot R_S$
Low side	High side	Low side	$(I_U + I_W)\ Rs = -I_V \cdot R_S$
Low side	High side	High side	$I_U \cdot R_S$
High side	Low side	Low side	$(I_V + I_W) \cdot R_S = -I_U \cdot R_S$
High side	Low side	High side	$I_V \cdot R_S$
High side	High side	Low side	$I_W \cdot R_S$
High side	High side	High side	0

Considering the schematic shown in *Figure 2*, the threshold current I_{max} at which protection acts is:

Equation 2

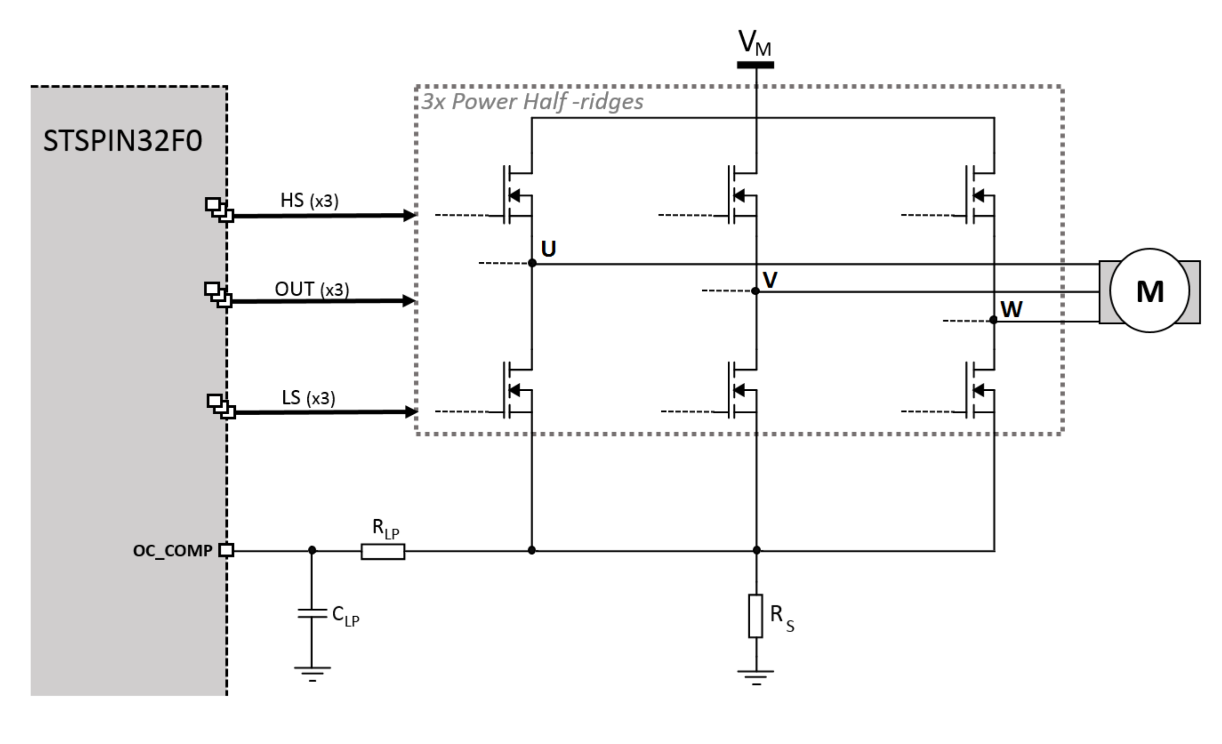
$$I_{max} = \frac{OC\_COMP_{th}}{R_S}$$

Where R_S is the value of the shunt resistor and OC_COMP_{th} is the internal reference chosen by the firmware according to *Table 1*. Should be noticed that power MOSFETs introduce noise when switching, hence a low pass filter can be added in order to reduce noise on the OC_COMP pin. Referring to *Figure 3*, a resistor R_{LP} >> R_S is used to decouple the capacitor C_{LP} and R_S. The cut-off frequency of the low pass filter is:

Equation 3

$$f_{LP} \cong \frac{1}{2\pi R_{LP} C_{LP}}$$

Figure 3. OC protection schematic - single shunt with low-pass filter



Bias resistor on OC_COMP pin (single shunt)

As *Equation 2* states, the current limit can be changed only changing the R_S or OC_COMP_{th}. However in many applications is not possible to change the R_S and only three values are available for the OC_COMP_{th} (see *Table 1*). To have a better resolution on the overcurrent threshold, it is possible to bias the OC_COMP pin with a pull-up resistor connected to V_{DD}, supplied by the STSPIN32F0. Consequently, the equivalent threshold will be decreased by the same amount of the bias voltage.

Referring to *Figure 4*, the OC_COMP pin will be biased at:

Equation 4

$$V_{bias,OC\_COMP} = V_{DD} \cdot \frac{R_{LP}}{R_B + R_{LP}}$$

Due to the R_B, the signal coming from the shunt resistor R_S will be partitioned too; considering a current I_x flowing through the R_S, the voltage contribution on the OC_COMP pin is:

Equation 5

$$V_{signal,OC\_COMP} = I_x R_S \cdot \frac{R_B}{R_B + R_{LP}}$$

Combining contributions described by *Equation 4* and *Equation 5* is possible to obtain the total voltage on the OC_COMP pin. The value of the current I_x, for which voltage on the OC_COMP becomes equal to the comparator internal reference OC_COMP_{th}, is the value of the maximum current allowed ($I_{max,b}$):

Equation 6

$$I_{max,b} \cdot R_S \cdot \frac{R_B}{R_B + R_{LP}} + V_{DD} \cdot \frac{R_{LP}}{R_B + R_{LP}} = OC\_COMP_{th}$$

In this way is possible to regulate the overcurrent threshold just changing the R_B resistor; its value can be found applying the following formula:

Equation 7

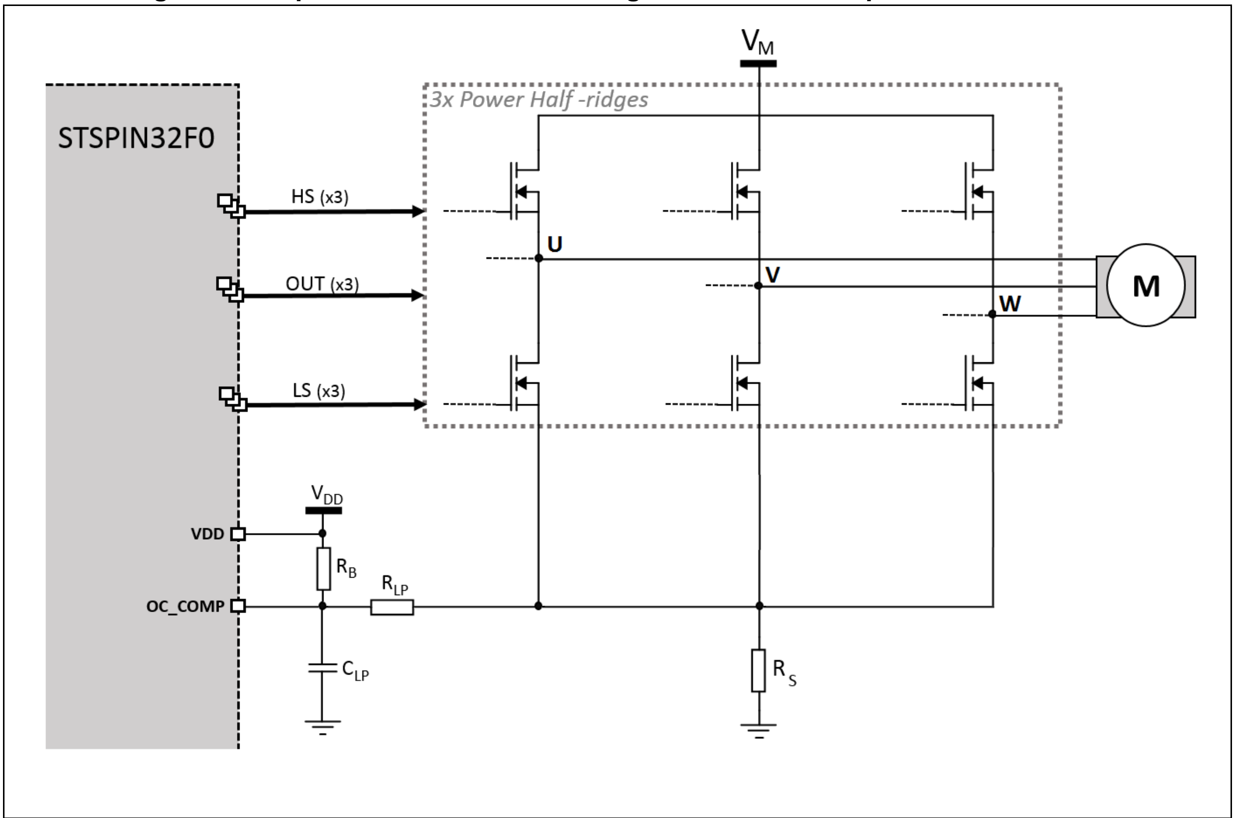
$$R_B \cong R_{LP} \cdot \left(\frac{V_{DD} - OC\_COMP_{th}}{OC\_COMP_{th} - I_{max,b} \cdot R_S}\right)$$

The presence of the R_B also modifies the low pass cut-off frequency stated in *Equation 3* as:

Equation 8

$$f_{LP} \cong \frac{1}{2\pi C_{LP} \dfrac{R_{LP} \cdot R_B}{R_{LP} + R_B}}$$

Figure 4. OC protection schematic - single shunt with low-pass filter and bias



3 Overcurrent detection in a dual shunt topology

In this topology only two phases have a shunt resistor; the third one is connected directly to GND. *Figure 5* gives an example of the dual shunt configuration where no shunt is connected to the W phase.

The current flowing in a phase is measured only when the respective low side MOSFET is turned on. Otherwise, the current does not flow into the related shunt resistor. Therefore, the overall current measured can be a combination of I_U, I_V, and I_W as listed in *Table 3*. According to *Equation 1* is possible to know the value of the current about a phase, using the value coming from the other two phases. This is the reason why the third shunt (e.g. on the phase W) is not connected.

However, potential issues can arise in overcurrent protection. Since the current on the phase W is not measured, high currents can flow in the phases but the signal coming from the other two shunt resistor is lower than expected. The worst case is when the U and V high side MOSFETs are on and the W low side MOSFET is on. In this situation, high currents can flow, but the voltage on the OC_COMP pin is always zero, hence overcurrent protection cannot be triggered.

For this reason, the dual shunt configuration for overcurrent protection can be used but is not recommended. Taking into account this notice, the overcurrent protection in dual shunt configuration can be analyzed as done in *Section 2* for single shunt configuration.

Figure 5. Power stage and OC protection schematic - dual shunt

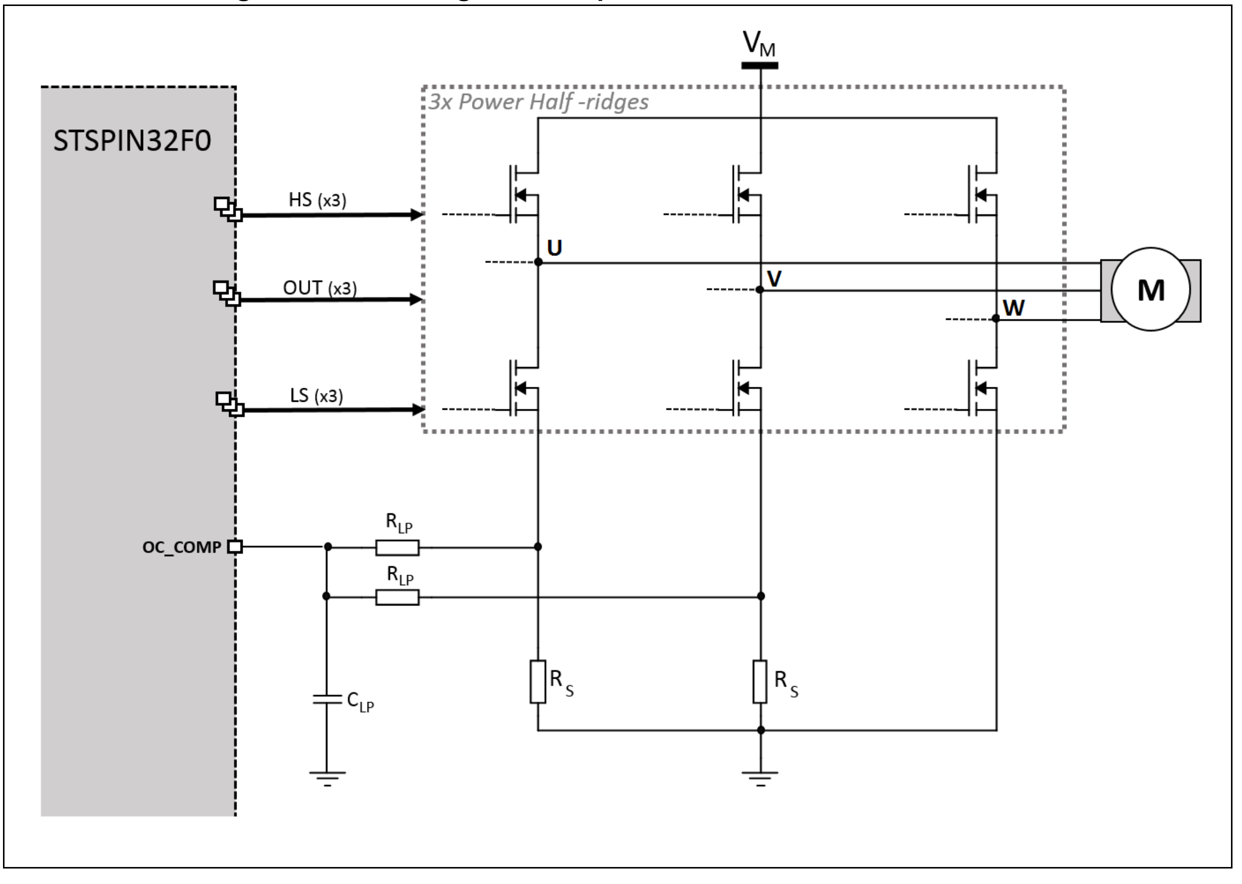


Table 3. Measured current according to power MOSFETs state - dual shunt

Power MOSFET turned ON			Measured current on OC_COMP input
Phase U	Phase V	Phase W	
Low side	Low side	Low side	$(I_U + I_V) \cdot R_S = -I_W R_S$
Low side	Low side	High side	$(I_U + I_V) \cdot R_S = -I_W R_S$
Low side	High side	Low side	$I_U \cdot R_S$ (1)
Low side	High side	High side	$I_U \cdot R_S$
High side	Low side	Low side	$I_V \cdot R_S$(1)
High side	Low side	High side	$I_V R_S$
High side	High side	Low side	0(1)
High side	High side	High side	0

1. Current is not measured on the phase W, potential issues can arise in overcurrent measurements.

According to the schematic shown in *Figure 5*, the threshold current I_{max} at which protection acts is:

Equation 9

$$I_{max} = \frac{2 \cdot OC\_COMP_{th}}{R_S}$$

Where OC_COMP_{th} is the comparator internal reference chosen by the firmware according to *Table 1 on page 3*.

The low pass filter introduced by the C_{LP} reduces noise on the OC_COMP pin. Referring to *Figure 5*, the cut-off frequency of the filter is:

Equation 10

$$f_{LP} \cong \frac{1}{\pi R_{LP} C_{LP}}$$

Bias resistor on OC_COMP pin (dual shunt)

As *Equation 9* states, the current limit can be changed only by changing the R_S or OC_COMP_{th}. However in many applications is not possible to change the R_S and only three values are available for OC_COMP_{th} (see *Table 1*). To have a better resolution on the overcurrent threshold is possible to bias the OC_COMP pin with a pull-up resistor connected to V_{DD}, supplied by the STSPIN32F0. Consequently, the equivalent threshold will be decreased by the same amount of the bias voltage.

Referring to *Figure 6*, the OC_COMP pin will be biased at:

Equation 11

$$V_{bias,OC\_COMP} = V_{DD} \cdot \frac{R_{LP}}{2R_B + R_{LP}}$$

Due to the R_B, the signal coming from the shunt resistors R_S will be partitioned too; considering the sum of the currents I_x flowing through the shunts R_S (in this specific case U and V), the voltage contribution on the OC_COMP pin is:

Equation 12

$$V_{signal,OC\_COMP} = \sum_{x=U,V} I_x R_S \cdot \frac{R_B}{2R_B + R_{LP}}$$

Combining contributions described by *Equation 11* and *Equation 12* is possible to obtain the total voltage on the OC_COMP. The total value of the current for which voltage on the OC_COMP becomes equal to the comparator internal reference OC_COMP_{th}, is the value of the maximum current allowed ($I_{max,b}$):

Equation 13

$$I_{max,b} \cdot R_S \cdot \frac{R_B}{2R_B + R_{LP}} + V_{DD} \cdot \frac{R_{LP}}{2R_B + R_{LP}} = OC\_COMP_{th}$$

In this way is possible to regulate the overcurrent threshold just changing the R_B resistor; its value can be found applying the following formula:

Equation 14

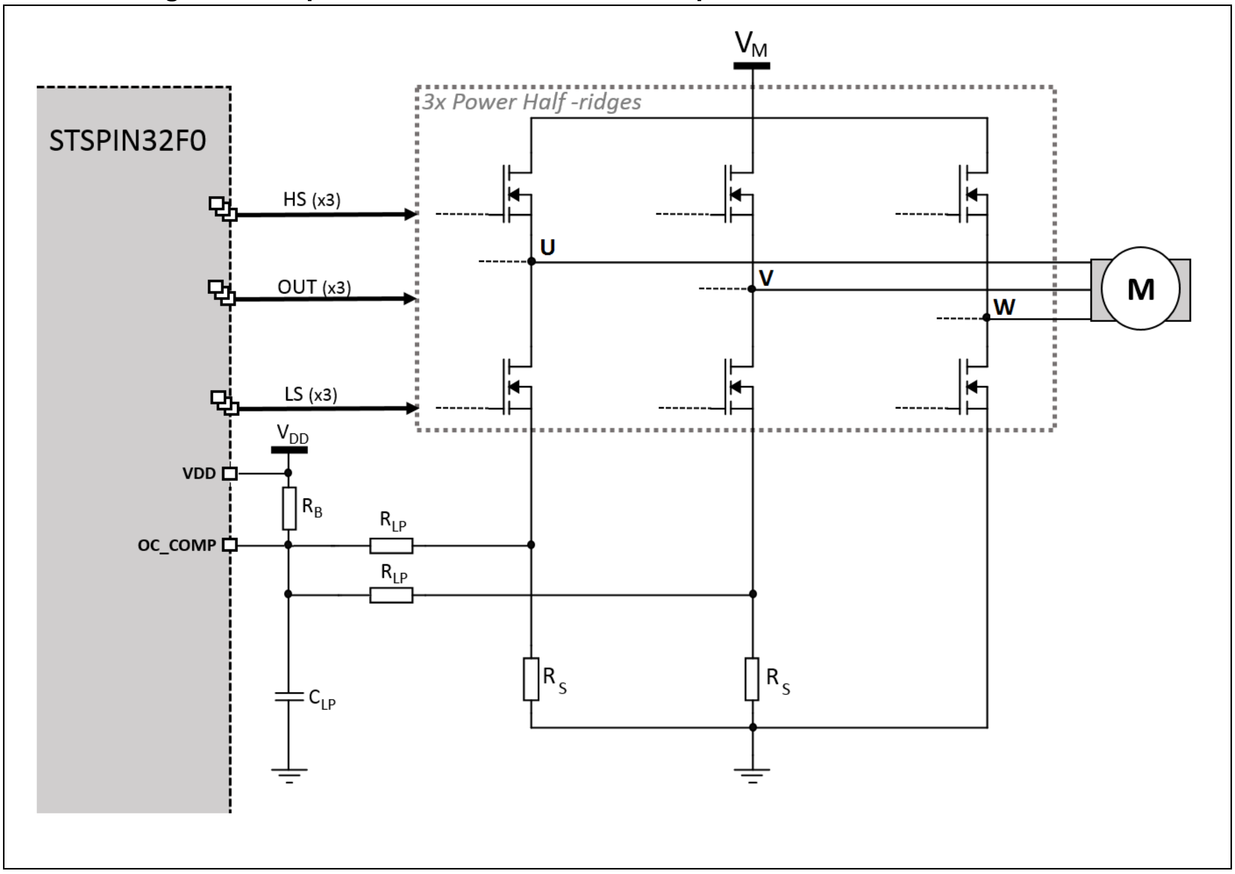
$$R_B \cong R_{LP} \cdot \left(\frac{V_{DD} - OC\_COMP_{th}}{2 \cdot OC\_COMP_{th} - I_{max,b} \cdot R_S} \right)$$

The presence of the R_B also modifies the low pass cut-off frequency stated in *Equation 10*.

Equation 15

$$f_{LP} \cong \frac{1}{2\pi C_{LP} \frac{R_{LP} \cdot R_B}{2R_B + R_{LP}}}$$

Figure 6. OC protection schematic with low-pass filter and bias - dual shunt



4 Overcurrent detection in a triple shunt topology

In this configuration the low side MOSFET of each half-bridge is connected to a shunt resistor used to measure the current in that phase. Referring to *Figure 7*, three resistors (R_{LP}) with the same value are used to sum the voltage of each shunt. Assume to choose $R_{LP} >> R_S$ so that all the current coming from a phase flows into the R_S. The voltage on the R_S is then reported on the OC_COMP pin through the partition given by the R_{LP} resistors. For a given phase X the voltage on the shunt resistor $V_{R,x}$ depends on the current flowing through the low side MOSFET on that phase:

Equation 16

$$V_{R,x} \cong I_X \cdot R_S$$

The voltage $V_{R,x}$ is then reported on the OC_COMP pin through the partition made by the resistors R_{LP}. The resulting voltage on the OC_COMP is:

Equation 17

$$V_{OC\_COMP,x} \cong V_{R,X} \cdot \frac{{}^{1}/_{2}\,(R_{LP} + R_S)}{R_{LP} + {}^{1}/_{2}\,(R_{LP} + R_S)}$$

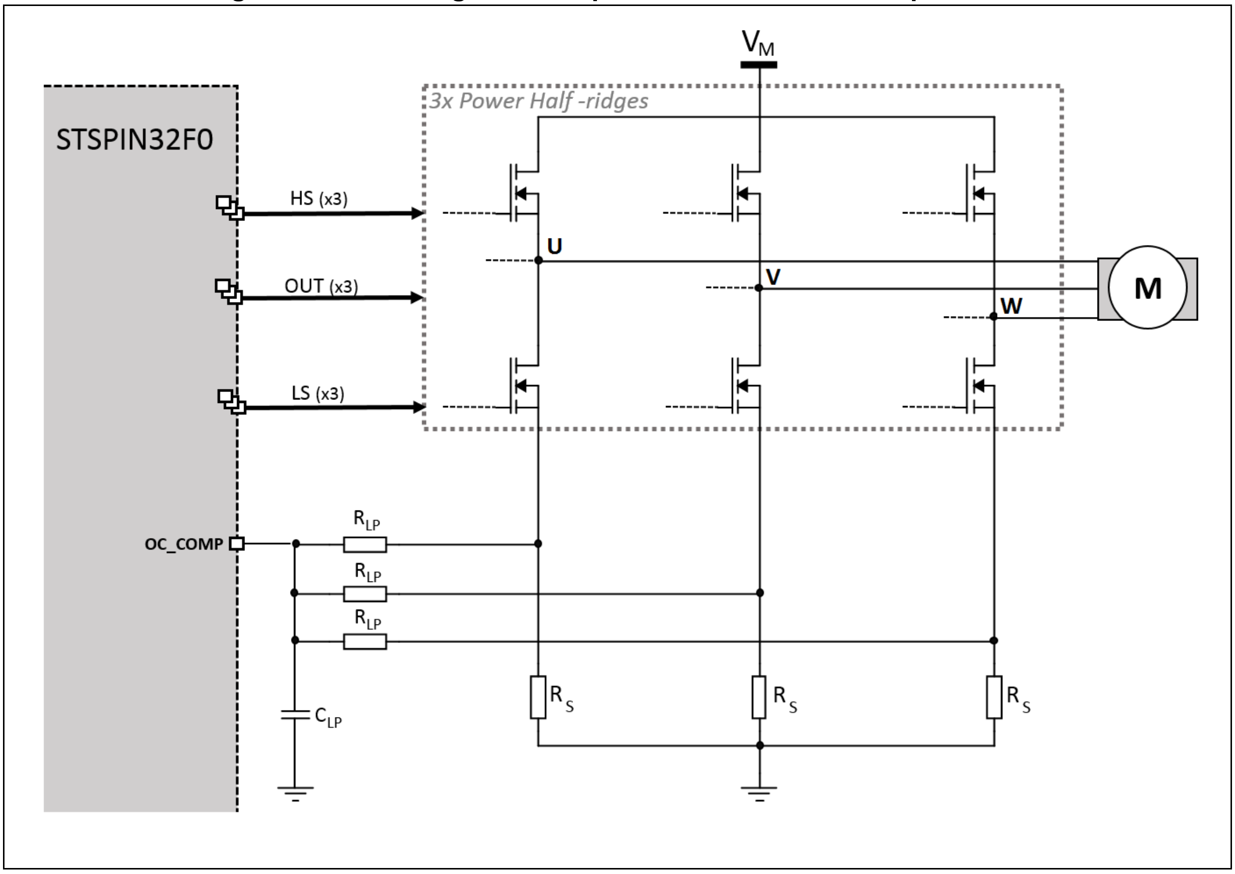
Using *Equation 16* and considering $R_{LP} >> R_S$, *Equation 17* becomes:

Equation 18

$$V_{OC\_COMP,x} \cong {}^{1}/_{3}\, I_X \cdot R_S$$

Each phase gives its contribution according to *Equation 18*, so that the overall signal on the OC_COMP pin is the sum of the voltage on each shunt resistor. As *Equation 18* shows, the main disadvantage of this circuitry is that the signal generated on the shunt resistor is attenuated by 1/3; however just three more resistors are needed.

Figure 7. Power stage and OC protection schematic - triple shunt



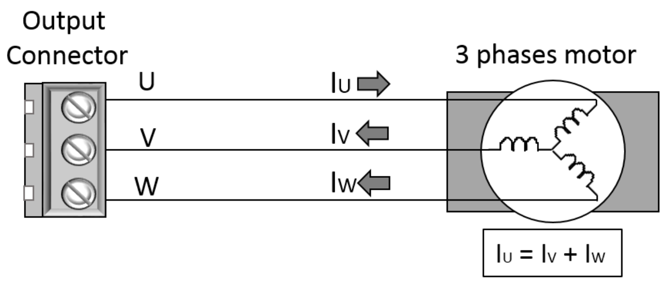
The current flowing in a phase is measured only when the respective low side MOSFET is turned on. Otherwise, the current does not flow into the related shunt resistor. Therefore, the overall current measured can be a combination of I_U, I_V, and I_W as listed in *Table 4*. The value of the current in a phase can be determined using the information coming from the other two phases according to *Equation 1 on page 4*.

Table 4. Measured current according to power MOSFETs state

Power MOSFET turned ON			Measured current on OC_COMP input
Phase U	Phase V	Phase W	
Low side	Low side	Low side	0
Low side	Low side	High side	$1/3 \cdot (I_U + I_V) \cdot R_S = -1/3 \cdot I_W \cdot R_S$
Low side	High side	Low side	$1/3 \cdot (I_U + I_W) \cdot R_S = -1/3 \cdot I_V \cdot R_S$
Low side	High side	High side	$1/3 \cdot I_U \cdot R_S$
High side	Low side	Low side	$1/3 \cdot (I_V + I_W) \cdot R_S = -1/3 \cdot I_U \cdot R_S$
High side	Low side	High side	$1/3 \cdot I_V \cdot R_S$
High side	High side	Low side	$1/3 \cdot I_W \cdot R_S$
High side	High side	High side	0

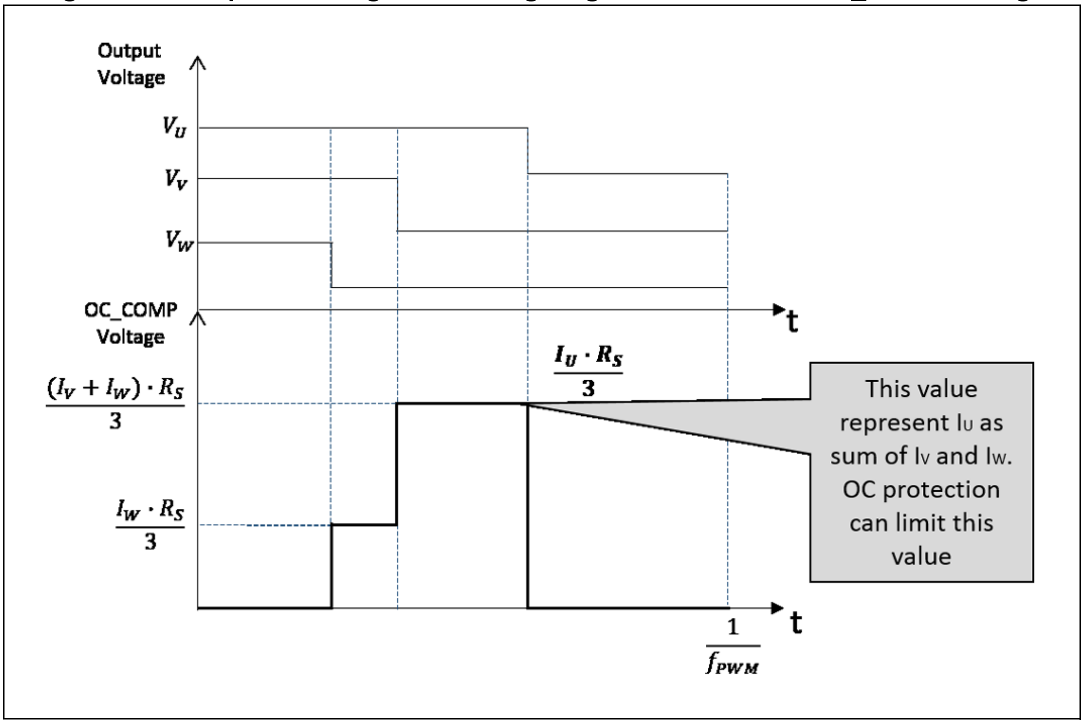
It should be noticed that phases are inductive loads and their current is controlled using the PWM method. This means that voltages and currents are not instantly correlated; e.g. on a given phase X, the high side MOSFET can be turned on but the current I_x flows into OUT_x. Conversely, the low side MOSFET can be on but the current flows out from OUT_x. This happens when the current in the inductive load is discharging. However, the current limiting based on overcurrent protection acts when the loads are charging. In this case, the maximum current flowing through one phase can be measured as the sum of the other two currents, as shown in *Table 4* and considering *Equation 1 on page 4*.

Figure 8. Example showing the output currents



As an example let's now consider the specific situation depicted in *Figure 8*, where the current is flowing into the phase U and comes back from the phase V and W. The PWM voltage signals are applied on the output nodes in order to control the currents (*Figure 9*). The higher current in this example is I_U: the maximum value that the OC_COMP pin will reach is 1/3 • I_U • R_S, just when the OUTU high side is on and the OUTV, W low sides are on. The amount of time for which OC_COMP voltage stays at this value depends on PWM frequency and duty cycles of the outputs. Should be noticed that the C_{LP} must be sized taking into account this timing, together with the response time of the overcurrent protection.

Figure 9. Example showing PWM voltage signals and related OC_COMP voltage



4.1 Sizing components values

Referring to the general schematic shown in *Figure 7*, some consideration (already done in *Section 2 on page 4* and *Section 3 on page 8*) can be done for components sizing. The R_{LP} resistors are chosen to be much greater than the R_S in order to decouple the current signals on each phase: the error due to coupling effects is:

Equation 19

$$\varepsilon = \frac{2R_S}{3(R_{LP} + R_S)} \cong \frac{2R_S}{3R_{LP}}$$

In the most of applications R_S <1 Ω and R_{LP} >1 kΩ, so coupling error is negligible.

The capacitor C_{LP} on the OC_COMP pin reduces noise and spikes generated by power MOSFET switching. The cut-off frequency of the low pass filter is:

Equation 20

$$f_{LP} \cong \frac{3}{2\pi R_{LP} C_{LP}}$$

The cut-off frequency can be chosen in order to have a response time of OC protection suitable for the application. A good trade-off between noise reduction and response time is to set the low pass frequency about 5 times the PWM frequency (f_{PWM}).

The threshold current I_{max} at which the overcurrent protection acts is:

Equation 21

$$I_{max} \cong \frac{3 \cdot OC\_COMP_{th}}{R_S}$$

Where OC_COMP_{th} is the comparator internal reference chosen by the firmware according to *Table 1 on page 3*.

Example 1

Assume PWM control with a f_{PWM} = 40 kHz that generates three sinusoidal currents in the motor phases. The nominal peak current is 1.5 A and the desired overcurrent threshold should be set at 3 A.

Using R_S = 0.1Ω, R_{LP} = 2.2 kΩ, C_{LP} = 1 nF and choosing the OC_COMP threshold at 100 mV is possible to disable the outputs when the current in one of the three phases reaches 3 A. The low pass filtering performed by the R_{LP} and C_{LP} has a frequency f_{LP} ~ 217 kHz, which is about 5 times the PWM frequency.

4.2 Bias resistor on OC_COMP pin (triple shunt)

As *Equation 21* states, the current limit can be changed only changing the R_S or OC_COMP_{th}. However in many applications is not possible to change R_S and only three values are available for OC_COMP_{th} (see *Table 1 on page 3*). To have a better resolution on the overcurrent threshold, is possible to bias the OC_COMP pin with a pull-up resistor connected to V_{DD}, supplied by the STSPIN32F0. Consequently, the equivalent threshold will be decreased by the same amount of the bias voltage.

Referring to *Figure 10*, the OC_COMP pin will be biased at:

Equation 22

$$V_{bias,OC\_COMP} \cong V_{DD} \cdot \frac{R_{LP}}{3R_B + R_{LP}}$$

Due to the R_B, the signal coming from the shunt resistors R_S will be partitioned too; considering the sum of the currents I_x flowing through the R_S for each phase, the voltage contribution on the OC_COMP pin is:

Equation 23

$$V_{signal,OC\_COMP} = \sum_{x=U,V,W} I_x R_S \cdot \frac{R_B}{3R_B + R_{LP}}$$

Combining contributions described by *Equation 22* and *Equation 23* is possible to obtain the total voltage on the OC_COMP. The total value of the current for which voltage on the OC_COMP becomes equal to the comparator internal reference OC_COMP_{th}, is the value of the maximum current allowed ($I_{max,b}$):

Equation 24

$$I_{max,b} \cdot R_S \cdot \frac{R_B}{3R_B + R_{LP}} + V_{DD} \cdot \frac{R_{LP}}{3R_B + R_{LP}} = OC\_COMP_{th}$$

In this way is possible to regulate the threshold just changing the R_B resistor; its value can be found applying the following formula:

Equation 25

$$R_B = R_{LP} \cdot \left(\frac{V_{DD} - OC\_COMP_{th}}{3 \cdot OC\_COMP_{th} - I_{max,b} \cdot R_S} \right)$$

The presence of the R_B also modifies the low pass cut-off frequency stated in *Equation 20*.

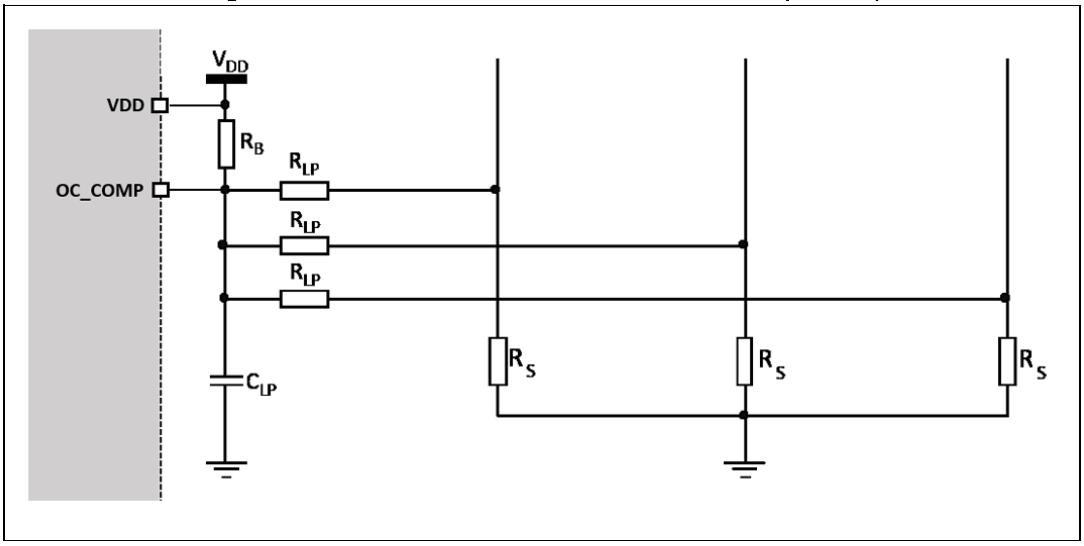
Equation 26

$$f_{LP} \cong \frac{1}{2\pi C_{LP} \dfrac{R_{LP} \cdot R_B}{3R_B + R_{LP}}}$$

Example 2

Referring to *Example 1*, consider to change the overcurrent threshold to 2 A using the same values of the OC_COMP_{th} and R_S. According to *Equation 25* using a $R_B \cong 70$ kΩ is possible to reduce the overcurrent threshold from 3 A to 2 A thus matching the new requirement on the overcurrent threshold. The filter frequency becomes slightly increased at 219 kHz, so no changes are needed on the C_{LP}.

Figure 10. OC COMP read-out with schematic (biased)



5 Conclusions

Despite of different shunt configurations described in *Section 2 on page 4*, *Section 3 on page 8*, and *Section 4 on page 12*, the results obtained are similar. Hereafter all the parameters used in the formulas are listed:

- $I_{max, th}$: current threshold at which the OC protection is triggered
- OC_COMP_{th}: internal reference for the comparator (can be 100, 250 or 500 mV - see *Table 1 on page 3*)
- R_S : shunt resistor(s)
- R_{LP}: resistor used to bring the signal from the shunt resistor(s) to the OC_COMP pin
- C_{LP}: filter capacitor on the OC_COMP pin
- R_B: optional resistor for the OC_COMP pin biasing
- V_{DD}: digital voltage supplied by the STSPIN32F0 (3.3 V typ.)
- F_{PWM}: frequency of the PWM driving signals

Moreover consider the parameter N_S, which represents the number of the shunt resistors used (e.g. for single shunt configuration N_S = 1). *Table 5* summarizes the formulas, with or without the OC_COMP biasing the resistor R_B.

Table 5. Formulas summary

Bias condition	Resistor to be chosen	Low pass cut off frequency
No bias on OC_COMP	$R_S = \left(\frac{N_S \cdot OC\_COMP_{th}}{I_{max,th}}\right)$	$f_{LP} = \frac{N_S}{2\pi R_{LP} C_{LP}}$
OC_COMP biased	$R_B = R_{LP} \cdot \left(\frac{V_{DD} - OC\_COMP_{th}}{N_S \cdot OC\_COMP_{th} - I_{max,th} \cdot R_S}\right)$	$f_{LP,b} = \frac{N_S R_B + R_{LP}}{2\pi R_{LP} C_{LP} R_B}$

Application example

This paragraph analyzes the setup described in *Example 1*, and shows how to act the OC protection feature. The power MOSFETs are connected to the STSPIN32F0 in a three shunt configuration and the OC_COMP pin is connected as shown in *Figure 7 on page 13*.

The firmware loaded into the internal MCU generates the 6 PWM signal resulting in 3 sinusoidal currents in the motor phases. Sinewaves are delayed of 120° each other, in order to implement open-loop voltage driving: PWM duty cycles are modulated in order to have a sinusoidal profile with specified amplitude.

As stated in *Example 1*, the following conditions are used:

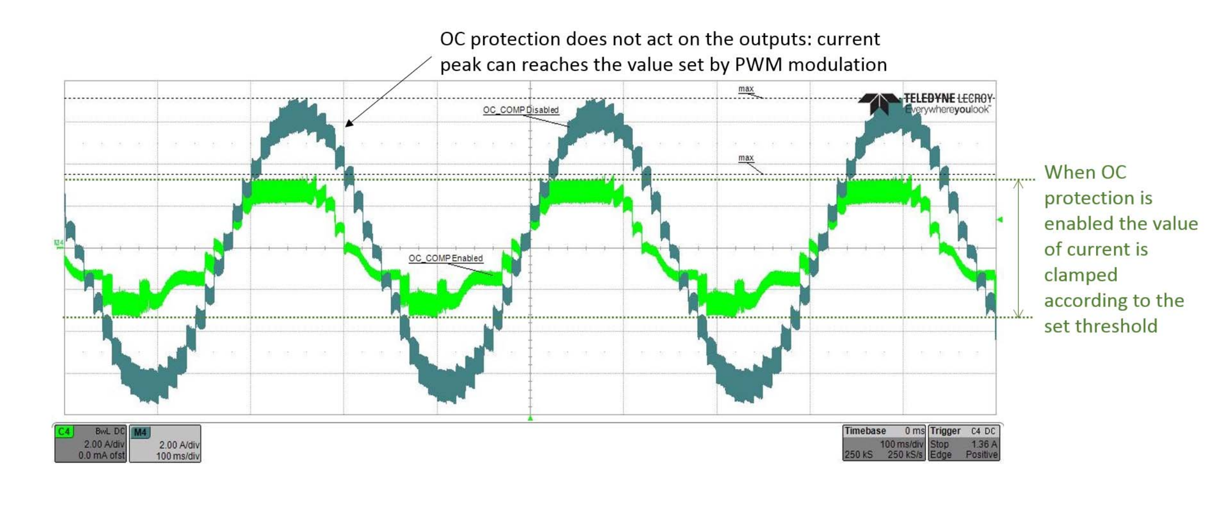
- f_{PWM} = 40 kHz
- R_S = 0.1 Ω
- R_{LP} = 2.2 kΩ
- C_{LP} = 1 nF
- OC_COMP_{th} = 100 mV

Since the triple shunt configuration is used, N_S = 3. The current threshold which triggers the OC protection is $I_{max,th}$ = 3 A - see *Equation 21 on page 16*. The analysis here described wants to highlight the effects of the OC protection: therefore, a peak current higher than the threshold is imposed. In this example, PWM duty cycles are chosen in order to have a current in each phase equal to the 7 A peak.

The resulting current acquisition for a single phase is reported in *Figure 11*. When the OC protection is disabled (OC_SEL = 0) the power MOSFETs work without limitations and the value of the peak current reaches the expected value of 7 A. Otherwise enabling the OC protection (OC_SEL = 1), the power MOSFETs are disabled whenever the current reaches the limit of 3 A, so the current is clamped and cannot reach the peak value of 7 A.

Although *Figure 11* shows just one phase, the clamping due to the OC protection is present in the same way on all the three phases.

Figure 11. OC protection effect on a phase current



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
31-Jan-2017	1	Initial release.