
ST8500 programmable power line communication modem
System on Chip design guide

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Introduction

The purpose of this application note is enabling any customer to design a full-performance ST8500 power line communication (PLC) node, based on the ST8500 evaluation kit (EVALKITST8500-1) design.

The ST8500 evaluation kit has been realized as a simple and flexible PLC node to ease the performance evaluation of the ST8500 device.

The kit is made of three boards: the ST8500 PLC module including the companion STLD1 line driver, the STM32 mother board and the power supply board based on the VIPER26H.

The PLC line coupling interface is designed to allow the ST8500 device to transmit and receive on the AC mains line using any narrow-band PLC modulation (single-carrier or OFDM) up to 500 kHz, for automatic meter reading (AMR) applications as well as any Smart Grid, Smart City, Smart Home or IoT applications.

Figure 1. ST8500 evaluation kit

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1 ST8500 programmable power line communication modem System on Chip description

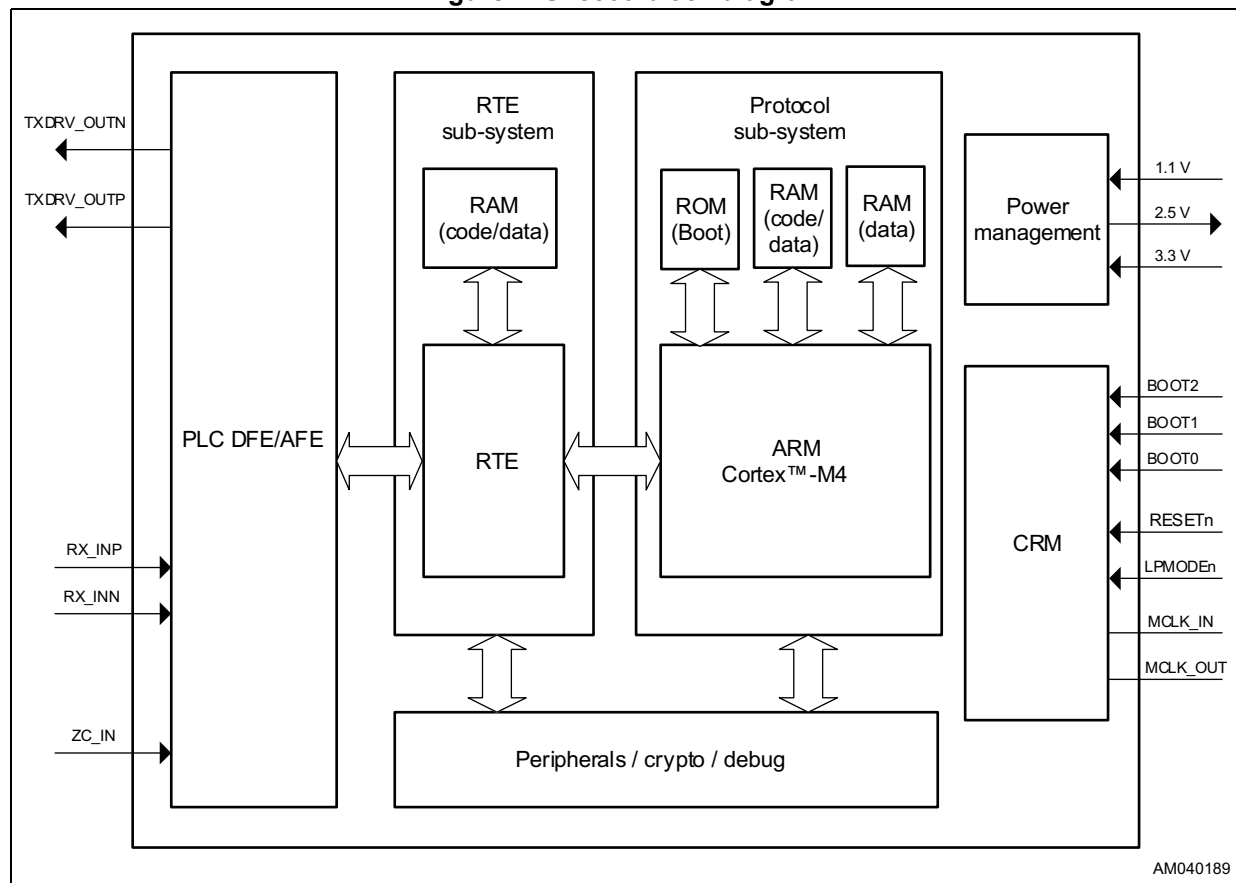
The ST8500 is a fully programmable power line communication (PLC) modem System on Chip (SoC), able to run any PLC protocol in the frequency band up to 500 kHz.

The device architecture has been designed to target the CENELEC EN50065, FCC and ARIB compliant applications supporting all major PLC protocol standards such as the ITU G.9904 (PRIME), ITU G.9903 (G3-PLC®) and many other possible PLC protocol specifications and evolutions.

The ST8500 basic block diagram is shown in [Figure 2](#).

For further details, see the ST8500 datasheet on st.com.

Figure 2. ST8500 block diagram



2 STLD1 power line communication dual line driver description

The STLD1 line driver is a low-distortion, high-current dual power amplifier specifically designed for power line communication applications, where the high output current is needed to drive the AC power line loads.

The operating on a single 8 - 18 V supply, the STLD1 is able to deliver the high output current up to 1.5 A rms and an output voltage swing up to the 18 V peak to peak single-ended / 36 V peak to peak differential.

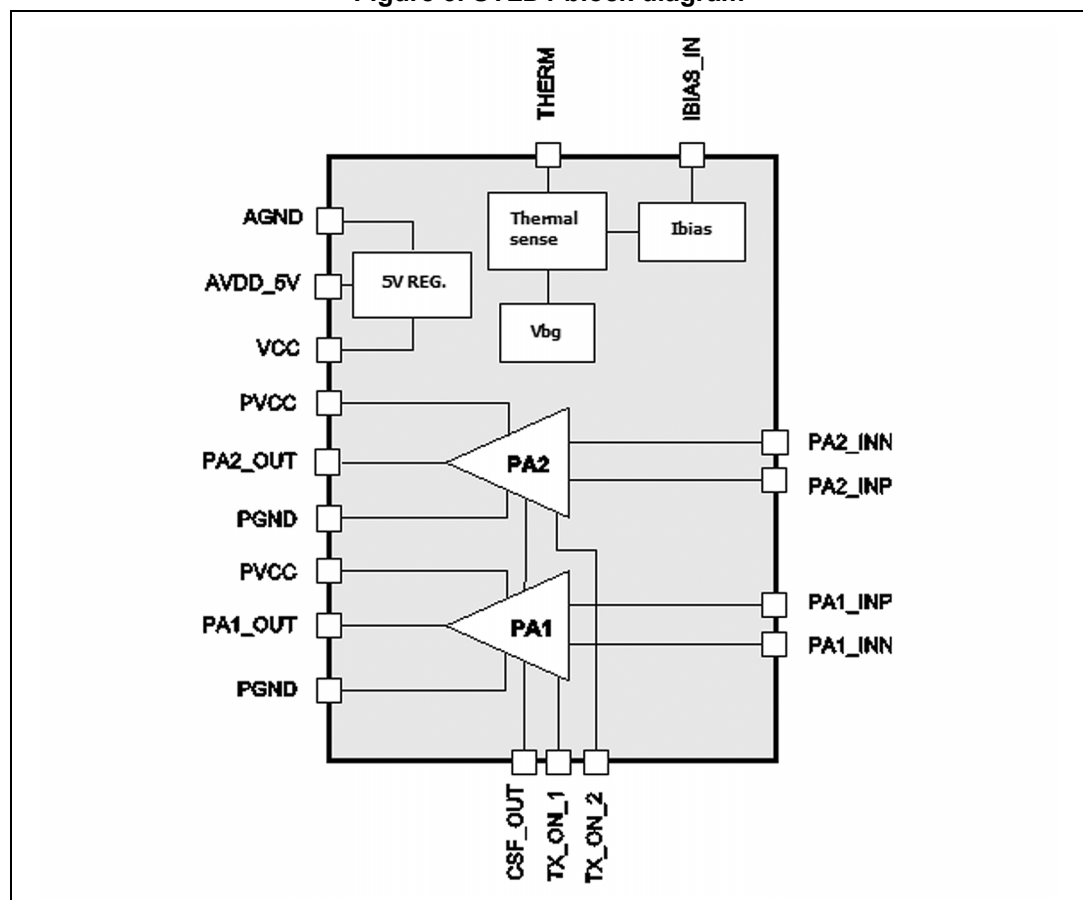
The STLD1 features a very low output impedance (down to $0.1\ \Omega$ in typical configuration) to ensure efficient transfer of power to very low impedance loads, typically between $0.5\ \Omega$ and $100\ \Omega$.

The device has the very low in-band and out-of-band two-tone inter-modulation distortion (IM3) as well as very high spurious-free dynamic range (SFDR) to guarantee an adequate margin to CENELEC, ARIB and FCC emission requirements.

It also features the thermal shutdown as well as current sense output.

The STLD1 block diagram is shown in [Figure 3](#).

Figure 3. STLD1 block diagram



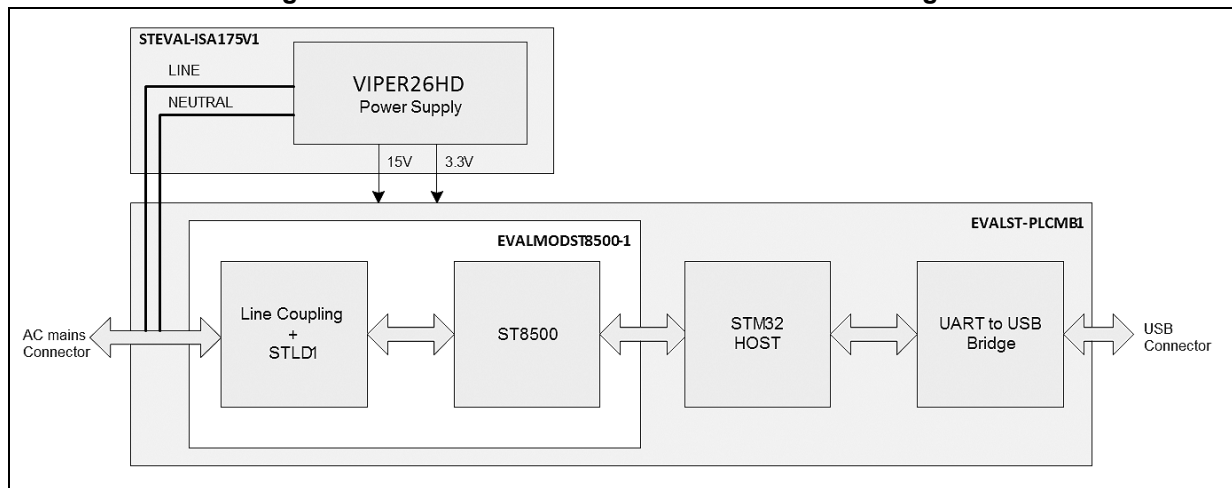
3 ST8500 evaluation kit description

The ST8500 evaluation kit is available as a board set comprising

- One ST8500 module, including the STLD1 line driver as a companion chip
- One STM32 mother board
- One power supply unit based on the VIPer26H

The functional block diagram is depicted in [Figure 4](#).

Figure 4. ST8500 evaluation kit - functional block diagram



4 ST8500 evaluation kit electrical characteristics

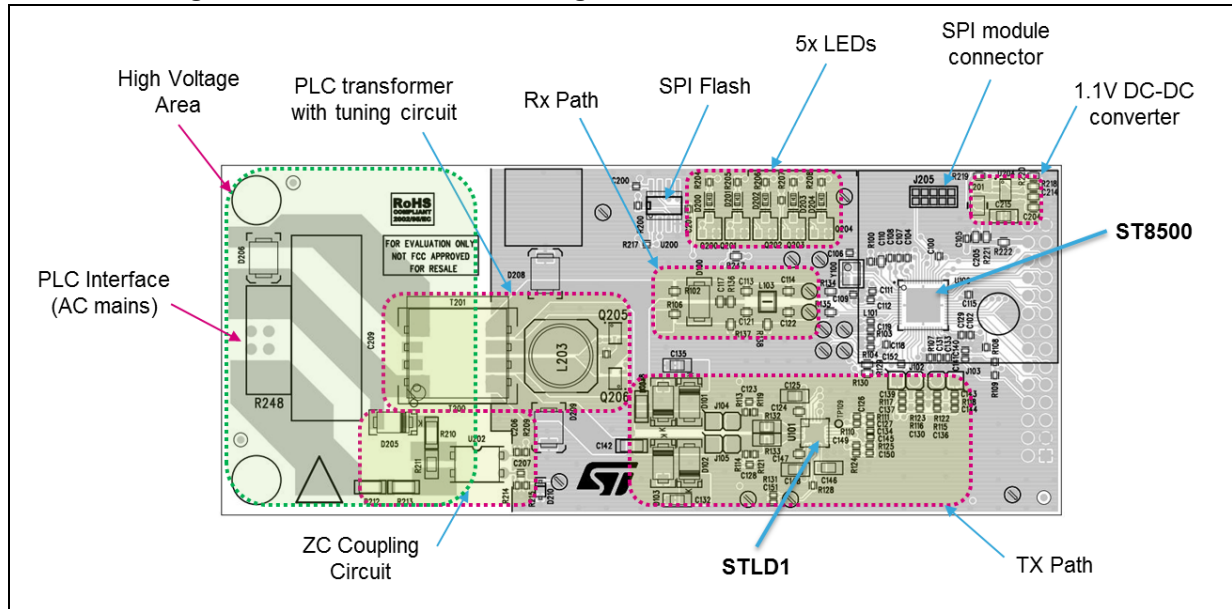
Table 1. Electrical characteristics

Parameter	Value				Notes
	Min.	Typ.	Max.	Unit	
AC mains input frequency	-	50/60	-	Hz	J107 connector
AC mains input voltage	90	230	440	V rms	
Single DC supply mode - DC source requirements					
DC input voltage	12	15	16	V	J101 connector
DC current capability	1	-	-	A	
VIPer26H power supply mode					
VCC DC voltage	14	15	16	V	J105 connector
VCC DC current capability	700	-	-	mA	
3.3 V DC voltage	3.1	3.3	3.5	V	
3.3 V DC current capability	200	-	-	mA	

5 ST8500 module description

The ST8500 module with its various sections is depicted in [Figure 5](#).

Figure 5. ST8500 module drawing with indication of the various sections



The main sections of the circuit will be described here after.

Note: *The passive and protection components included in the schematics are mostly for reference. Any BOM change due to the cost reduction or parts availability shall keep the main electrical characteristics of the components unchanged.*

5.1 ST8500 supply and digital connections

The ST8500 supply and digital circuit sections from module schematics are reported here below.

The device is supplied by 3V3 and 1V1 external supply rails, while the 2V5 AFE supply is internally generated from the 3V3 rail. Each supply pin has its own 100 nF bypass capacitor, plus bulk capacitors on specific pins.

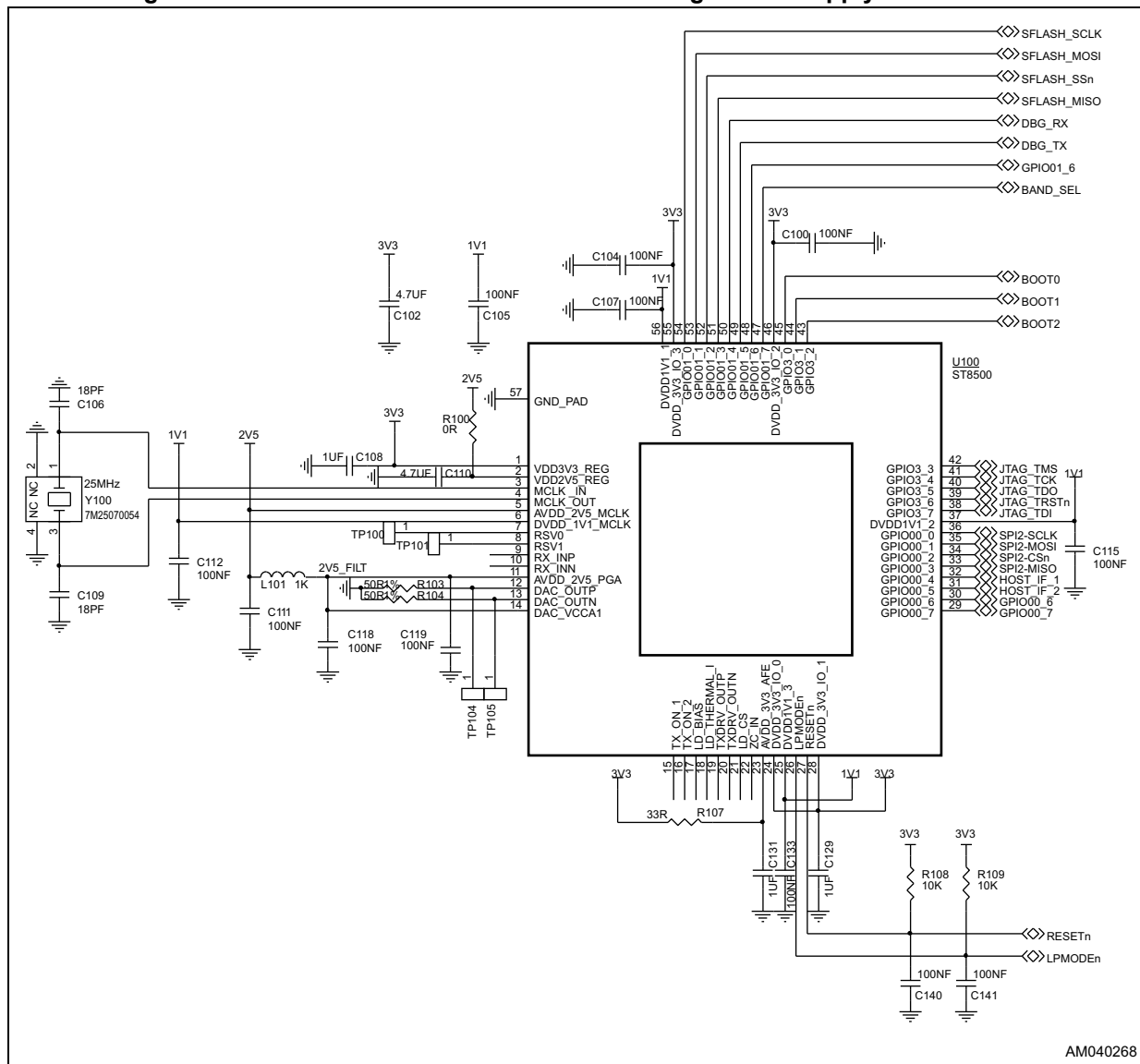
3V3 and 2V5 AFE supply pins have additional filtering to guarantee the PLC TX and RX performance.

The RESETn and LPMODEn pins have one 10 kΩ pull-up resistor and the 100 nF bypass capacitor each, for a clean boot and to achieve proper immunity to electromagnetic interference.

An optional SPI Flash memory is connected to the ST8500 SPI1 interface. Based on the boot configuration, it is possible to save the ST8500 FW on that SPI Flash for a standalone boot. Nevertheless, the default ST8500 boot mode requires the STM32 host controller to download the FW to the ST8500 internal RAM at boot time through the UART host interface.

To guarantee such default boot configuration, all BOOT pins (mapped on GPIO03_0, GPIO03_1 and GPIO03_2) have an internal pull-down.

Figure 6. ST8500 module schematics - ST8500 digital and supply connections



5.1.1 ST8500 digital IO mapping

See [Table 2](#) for the minimum set of signals to be included in the interface to the host controller, for proper application design.

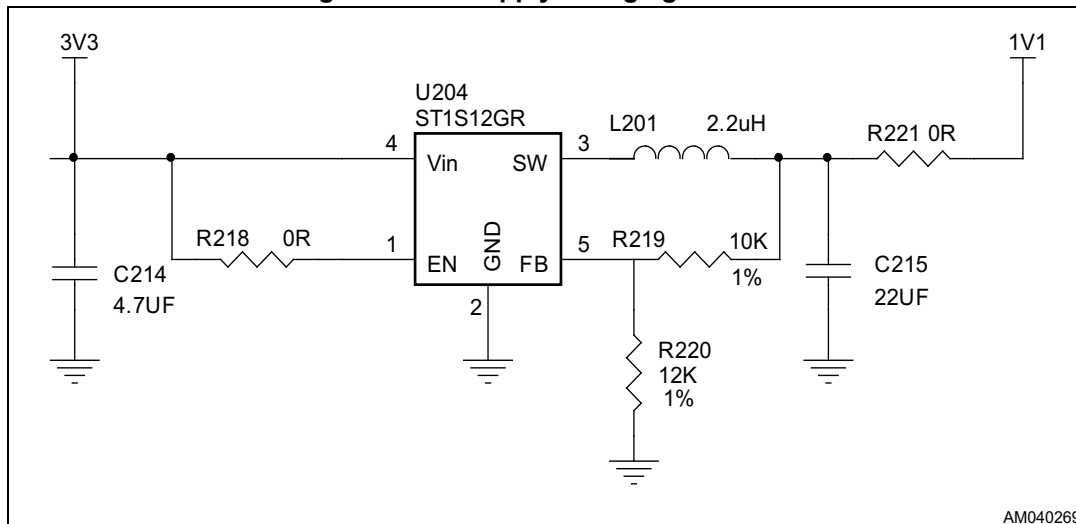
Table 2. Digital IO assignment table for the ST8500 evaluation kit

ST8500 pin	Selected function	Exported to	Remarks
RESETn	-	J200 (STM32 interface connector)	Included in the basic host interface
LPMODEn	-	J200 (STM32 interface connector)	-
GPIO00_0	SPI2-SCLK	J205 (SPI expansion connector)	-
GPIO00_1	SPI2-MOSI	J205 (SPI expansion connector)	-
GPIO00_2	SPI2-CSn	J205 (SPI expansion connector)	-
GPIO00_3	SPI2-MISO	J205 (SPI expansion connector)	-
GPIO00_4	USART0_RXD	J200 (STM32 interface connector)	Included in the basic host interface
GPIO00_5	USART0_TXD	J200 (STM32 interface connector)	Included in the basic host interface
GPIO00_6	GPIO00_6	J200 (STM32 interface connector)	-
GPIO00_7	GPIO00_7	J205 (SPI expansion connector)	LED on module
GPIO01_0	SFLASH_SCLK	U200 (optional SPI Flash)	-
GPIO01_1	SFLASH_MOSI	U200 (optional SPI Flash)	-
GPIO01_2	SFLASH_SS _n	U200 (optional SPI Flash)	-
GPIO01_3	SFLASH_MISO	U200 (optional SPI Flash)	-
GPIO01_4	DBG_RX	J200 (STM32 interface connector)	-
GPIO01_5	DBG_TX	J200 (STM32 interface connector)	USART2 TXD required for modem debug prints
GPIO01_6	GPIO01_6	J205 (SPI expansion connector)	-
GPIO01_7	BAND_SEL	Q205-Q206 (line coupling)	LED on module
GPIO03_0	BOOT0	J200 (STM32 interface connector)	LED on module
GPIO03_1	BOOT1	J200 (STM32 interface connector)	LED on module
GPIO03_2	BOOT2	J200 (STM32 interface connector)	LED on module
GPIO03_3	JTAG_TMS	J200 (STM32 interface connector)	ST8500 JTAG not accessible for customer development
GPIO03_4	JTAG_TCK	J200 (STM32 interface connector)	ST8500 JTAG not accessible for customer development
GPIO03_5	JTAG_TDO	J200 (STM32 interface connector)	ST8500 JTAG not accessible for customer development
GPIO03_6	JTAG_TRSTn	J200 (STM32 interface connector)	ST8500 JTAG not accessible for customer development
GPIO03_7	JTAG_TDI	J200 (STM32 interface connector)	ST8500 JTAG not accessible for customer development

5.1.2 1V1 supply voltage generation

The 1V1 supply rail is generated from the 3V3 supply using the ST1S12GR DC-DC switching converter for a low-cost and efficient solution.

Figure 7. 1V1 supply voltage generation



5.2 Power line interface section

The power line interface section is composed of four different sub-sections: the line driver, the line coupling, the reception filter, and the zero crossing (ZC) coupling. It is designed for isolation from the AC mains thanks to the PLC transformer and the ZC optocoupler.

Both transmission and reception paths are fully differential, allowing for the higher dynamic range and noise immunity.

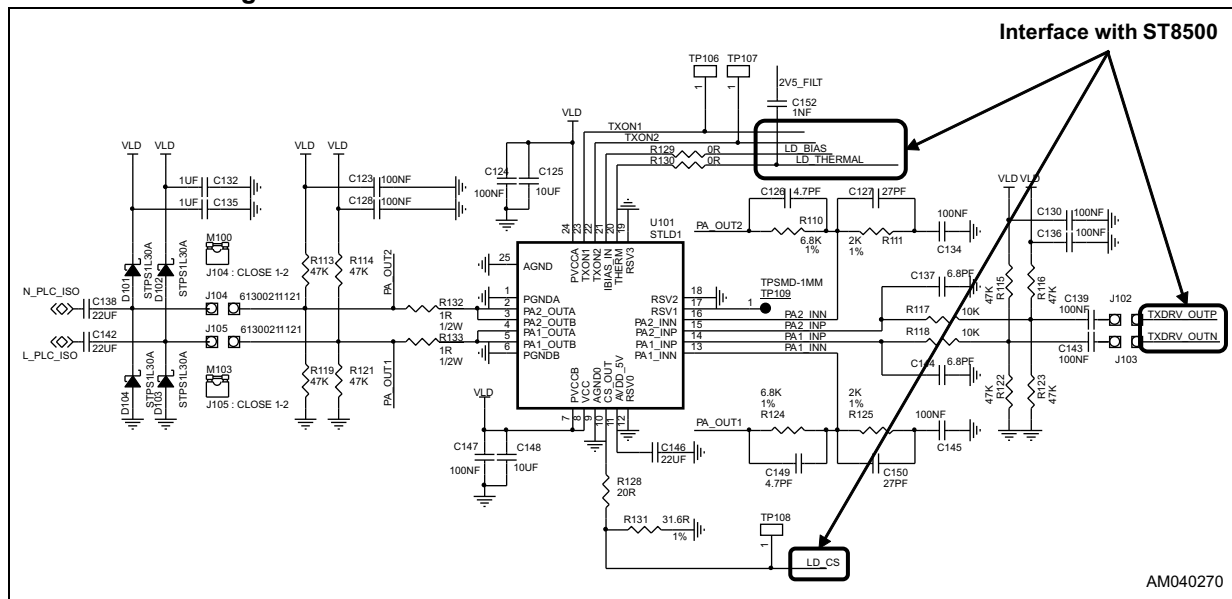
The frequency response of this section is usually sensitive to tolerance of component values. Actual components used in the power line interface section of the ST8500 evaluation kit have the following tolerances: $\pm 20\%$ for the X1 capacitor and the coils, $\pm 10\%$ for SMD ceramic X7R capacitors, $\pm 1\%$ for SMD resistors.

For the line driver, C0G/NPO type capacitors are required to guarantee linearity and stability against signal amplitude and frequency.

5.2.1 Line driver section

The line driver sub-section is based on the STLD1 dual line driver, whose input and output pins are externally available to allow configurability of the circuit. It is supplied by a single VCC power supply rail, with up to the 1 A supply current capability.

Figure 8. ST8500 module schematics - STLD1 line driver section



The STLD1 amplifies the differential transmitted signal generated by the ST8500 through the integrated current DAC and pre-driver, providing as well all the required current to drive the typically low impedance of the AC power line.

In the frequencies of interest, the in-band amplifier gain can be calculated as

Equation 1

$$|G_{TX}| = 1 + \frac{6K8}{2K} = 4.4 = 13 \text{ dB}$$

The C134 and C145 are used to set the DC gain of the filter to 0 dB (input bias and output bias voltages are both $V_{CC}/2$), while the C126 - C127 and C149 - C150 provide gain compensation by reducing the gain at high frequencies.

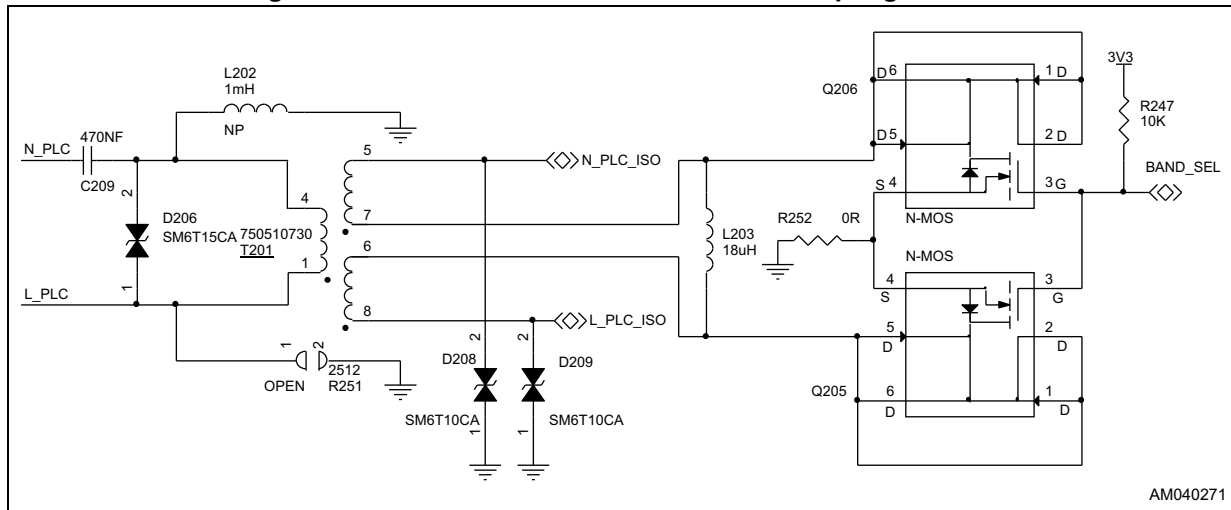
5.2.2 Line coupling section

The coupling to the power line requires a few passive components. Its basic components are the line transformer T201, the power inductor L203 and the X1 safety capacitor C209.

The L203 has been accurately chosen to have high saturation current ($> 2 \text{ A}$) and very low equivalent series resistance ($< 0.1 \Omega$), to limit distortion and insertion losses even with the heavy line load.

The line coupling also includes protection diodes against common-mode and differential disturbances coming from the power line, specifically D206, D208 and D209.

Figure 9. ST8500 module schematics - line coupling section



Center frequency for the coupling response can be calculated at first approximation as

Equation 2

$$f_c = \frac{1}{2\pi\sqrt{(L_{leak} + L203) \cdot C209}}$$

where L_{leak} is the leakage inductance of the coupling transformer T201, adding about 1 μH to the L203.

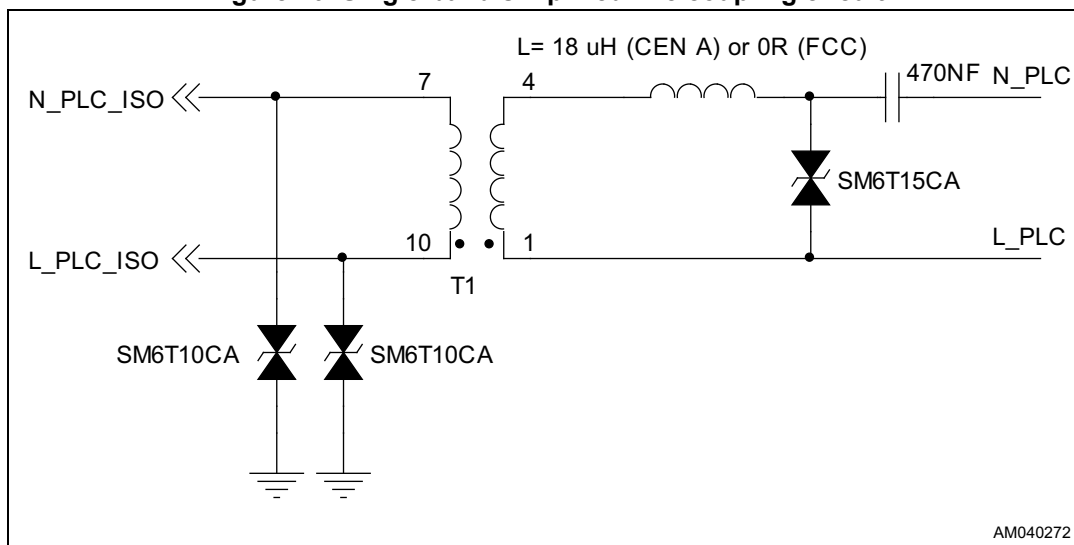
The Q factor of this coupling circuit is driven by the mains line impedance: the correct choice of the L203 and C209, anyway, allows limiting the loss to a few dBs even with a line impedance as low as 2 Ω .

The ST8500 evaluation kit line coupling circuit exploits an ST patented solution for automated frequency tuning: a ST8500 GPIO (BAND_SEL) controls a simple NMOS switch, to include the L203 (BAND_SEL=0) or bypass it (BAND_SEL=3V3) for the operation in CENELEC A or FCC band respectively.

Note: In case of tuning for the CENELEC B band, the L203 can be easily replaced by a 4.7 μH inductor with similar characteristics. The NMOS switch will be kept open in this case (BAND_SEL=0).

In case of the single-band PLC coupling, the circuit can be simplified as indicated in [Figure 10](#).

Figure 10. Single-band simplified line coupling circuit



Line transformer

Particular attention has been paid in choosing the line transformer characteristics. The required characteristics are listed in order to have a good signal transfer and minimize the insertion losses, it is recommended to choose a transformer with a primary (high-voltage side) inductance of 0.5 mH or greater, a leakage inductance around 1 μ H and total DC resistance lower than 0.5 Ω .

The reference part number included in the ST8500 evaluation kit is WE 750510730.

Table 3. Line coupling transformer specifications

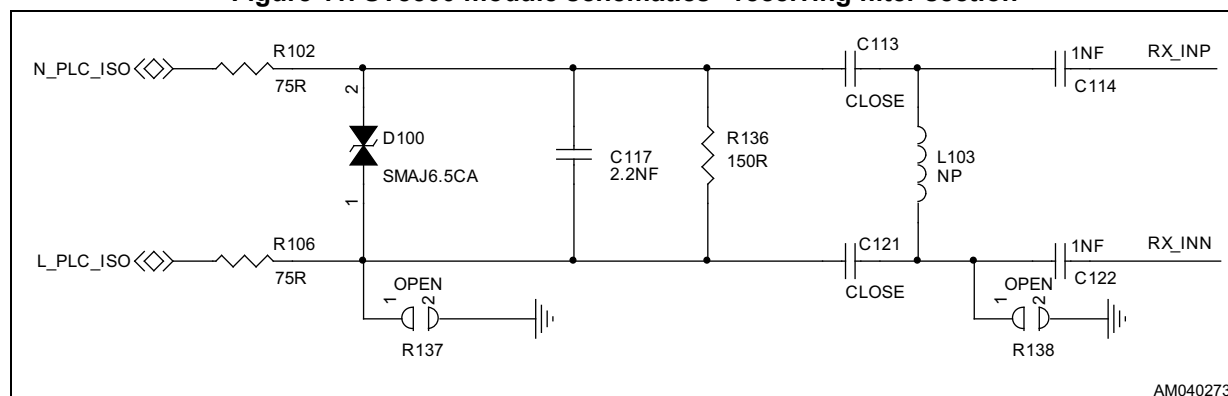
Parameter	Value
Turn ratio	1:1
Shunt inductance	≥ 0.5 mH
Leakage inductance	1 μ H (typ.)
DC total resistance	≤ 0.5 Ω
DC saturation current	≥ 15 mA
Inter-winding capacitance	< 30 pF
Withstanding voltage	≥ 4 kV for double insulation ≥ 1.5 kV for functional insulation

5.2.3 Reception filter

The reception filter in its default configuration is a simple band-pass filter covering both CENELEC and FCC bands.

Note that it has to divide by two the incoming signal amplitude, through a resistor divider, to adapt the line driver output range (up to 30 V peak to peak with $V_{CC} = 15$ V) to the ST8500 receiver input range (up to 15 V peak to peak).

Figure 11. ST8500 module schematics - receiving filter section

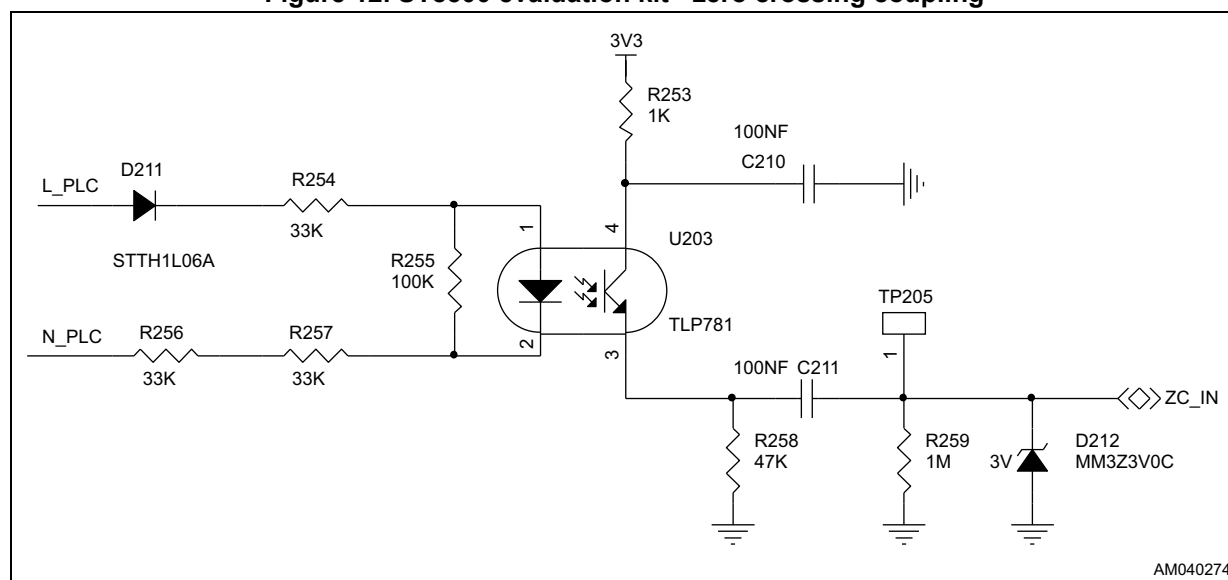


5.2.4 Zero crossing coupling

The zero crossing coupling circuit is aimed at providing a bipolar (AC) signal synchronous with the mains network voltage to the ZC_IN pin. This signal must be centered on AGND and limited to 10 V_{pp}.

The zero crossing coupling is optional, based on the specific PLC protocol and application layer requirements. In case the mains zero crossing is not required, the ZC_IN pin can be pulled up to 3V3.

Figure 12. ST8500 evaluation kit - zero crossing coupling



The isolated zero crossing circuit is realized through an optocoupler in non-inverting configuration. Neutral and phase lines are brought to the optocoupler through 3 x 33 k Ω resistors in series. The STTH1L06A diode blocks the negative half-wave, thus reducing the circuit power consumption by half. The 3 x 33 k Ω resistors limit the photodiode input current to nearly 2 mA rms at 230 V AC. Having several resistors in series helps preventing short-circuits in case of the resistor degradation.

The timing characteristics of this circuit are listed in [Table 4](#).

Table 4. Zero crossing isolated coupling - measured timing characteristics

Edge	ZC delay	ZC jitter
Positive	232 μ s	4 μ s
Negative	4.8 μ s	3 μ s

6 PCB design guidelines

6.1 Debug requirements for end applications

In order to speed up and simplify the bring-up, debug and validation of an end application based on the ST8500, it is recommended to export the following signals to a dedicated connector, or to easily accessible test points:

- USART0_RXD
- USART0_TXD
- DBG_TX
- RESETN
- BOOT1

Connecting the signals listed above to the STM32 mother board of the EVALKITST8500-1 could be very useful to test the communication performance of the ST8500 section of the end application, by enabling full low-level control of the ST8500 through the same SW tools used for the EVALKITST8500-1.

To control those signals by the STM32 of the EVALKITST8500-1, it should be possible to disconnect them from the host controller of the end application (e.g. by removing jumpers or 0 Ω resistors), or to set them in the high impedance state.

6.2 PCB design for STLD1 thermal performance

The ST8500 and STLD1 devices can operate within an ambient temperature range from -40 to +105 °C. Especially at high ambient temperature conditions, the effect of the power dissipation of the devices must be considered to keep the PLC node operating in safe conditions.

Almost all power dissipation care goes to the STLD1 line driver. Even if it features overtemperature protection, the role of the PCB design is the most important to ensure proper dissipation.

A QFN 4 x 4 package with the exposed pad (internally connected to AGND) has been chosen for the STLD1 device to have a very good thermal performance. To take the full advantage from this, the PCB must be designed to effectively conduct heat away from the package.

To get the low impedance thermal path from the STLD1 device to the PCB, a 2.7 x 2.7 mm thermal pad has been realized on the PCB top layer. In order to effectively remove the heat, the exposed pad must be soldered well to the PCB thermal pad.

For an effective heat transfer from the top layer of the PCB to the bottom layer, thermal vias need to be included within the thermal pad area. If properly designed, thermal vias are the most efficient paths for removing heat from the device.

The STLD1 on the ST8500 PCB module shows very good thermal resistance R_{th_ja} of 27 °C/W, allowing full-scale TX signal power even with a line impedance as low as 2 Ω .

The layout recommendations to achieve the best thermal performance are as follows

- For the TOP layer
 - The top layer function is to transmit heat from the package to the PCB border as well as to the bottom layer
 - An AGND copper area must be placed under the exposed pad, extending as much as possible around the device
 - An array of 3 x 3 thermal vias (top to bottom layer) at the 1.0 mm pitch, drill diameter 0.3 mm, shall connect the thermal pad to the bottom layer AGND plane and to the inner AGND planes
 - Any unused PCB area outside of the package footprint must be filled with copper tied to the dissipating AGND plane on the inner and bottom layer
- For the INNER layers
 - Fill with AGND the area below the STLD1 device
 - No tracks shall cut the AGND area below the device
- For the BOTTOM layer
 - The bottom layer acts as the real radiator
 - The solid AGND area of copper on this layer must be as large and continuous (not cut by tracks) as possible, to minimize the thermal impedance
 - To reduce the solder wicking effect due to open vias, possibly leading to poor soldering of the exposed pad, the “via encroaching” technique can be adopted. The bottom-side solder resist shall have small openings around the thermal vias (nearly 0.2 mm larger than the via drill diameter); the reduced area of exposed copper on the bottom limits the amount of the solder paste flowing down the vias
 - Traces on the bottom side must run as far as possible from the area corresponding to the heat column below the STLD1 device

Figure 13. STLD1 PCB dissipating area on the ST8500 module - top layer

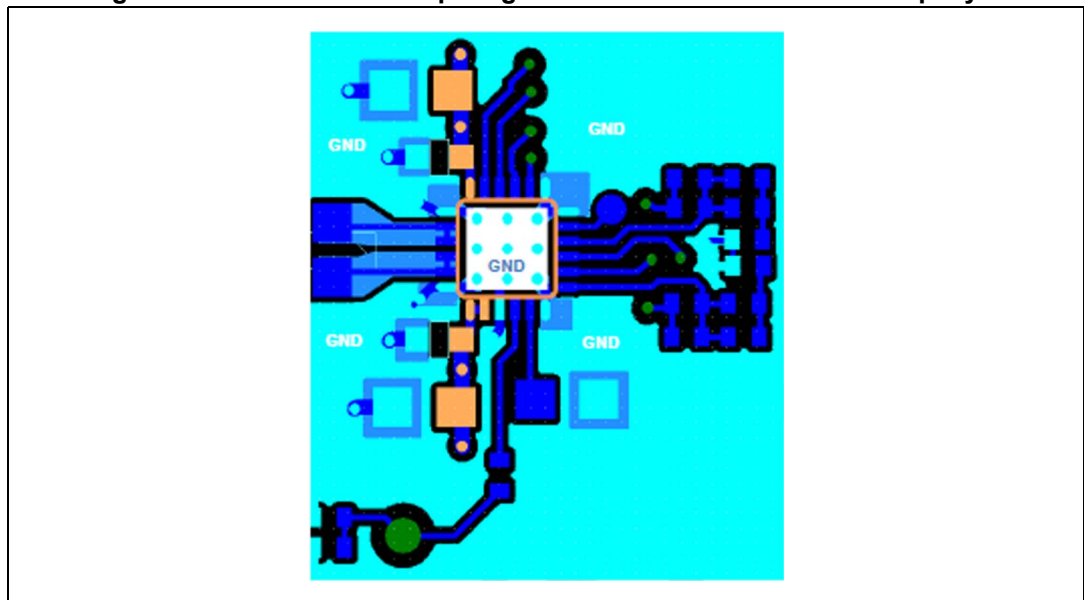


Figure 14. STLD1 PCB dissipating area on the ST8500 module - inner layer 2 (ground plane)

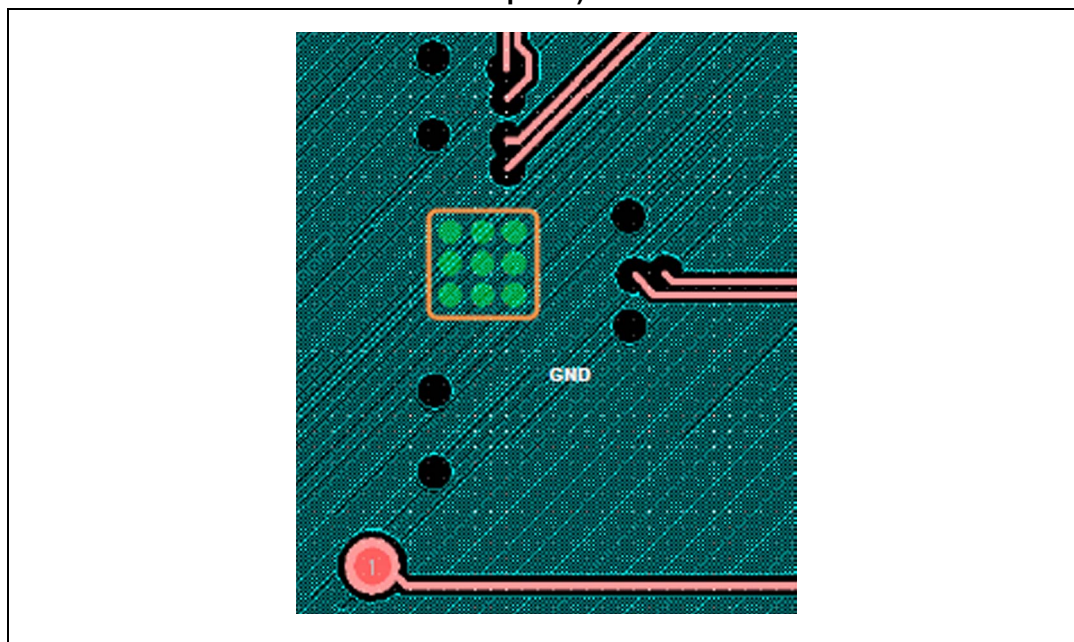


Figure 15. STLD1 PCB dissipating area on the ST8500 module - inner layer 3 (supply plane)

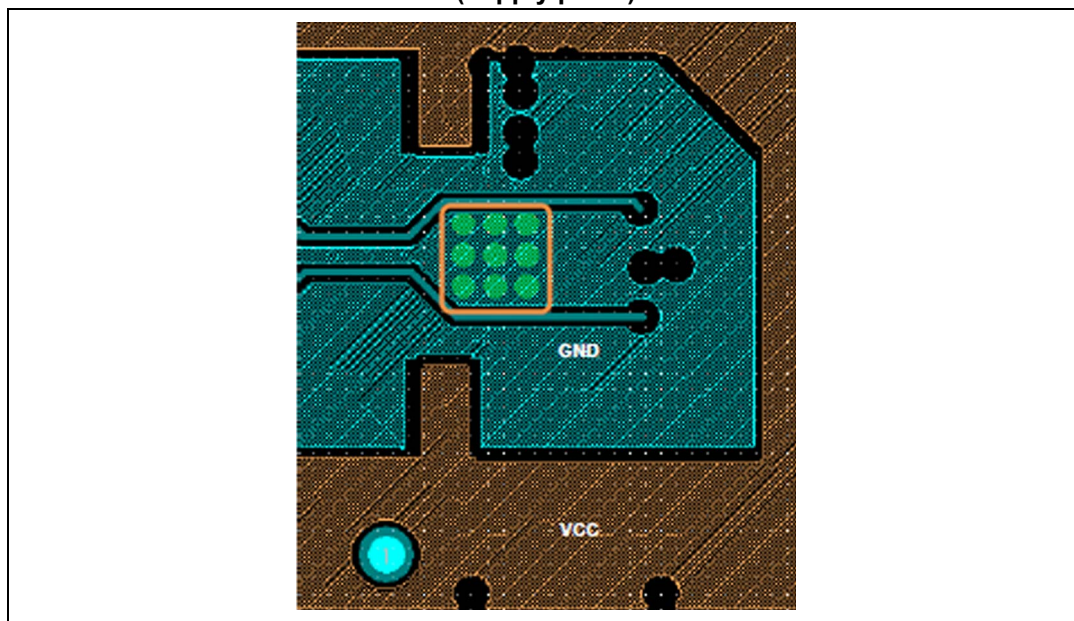
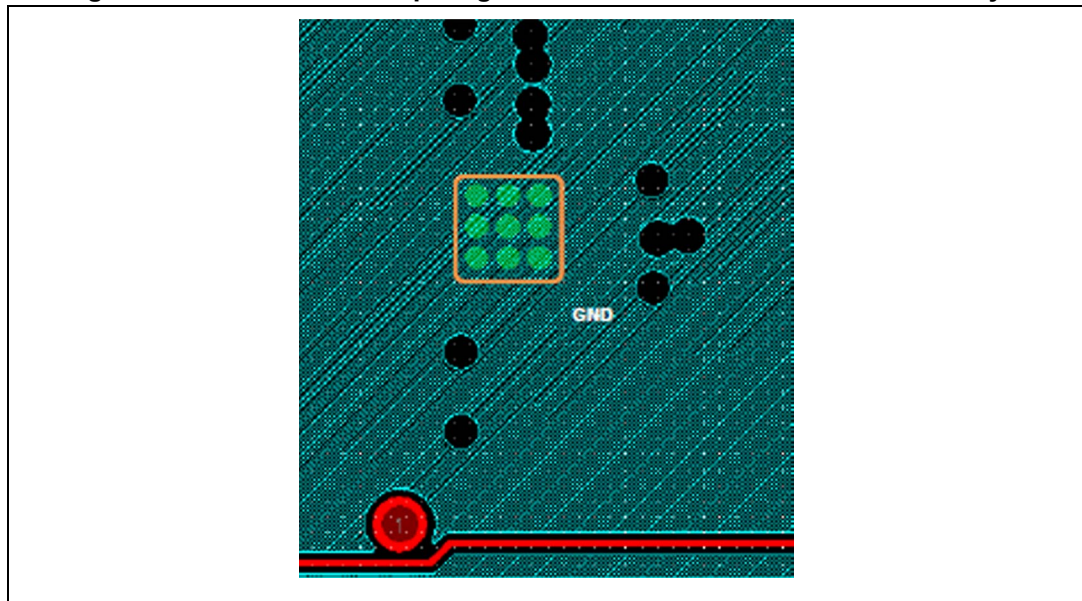


Figure 16. STLD1 PCB dissipating area on the ST8500 module - bottom layer



6.3 Power supply connections

Best practice rules must be applied to the connection of the ST8500 and STLD1 power supply rails: 3.3 V, 1V1 and VCC.

Decoupling capacitors must be placed as close as possible to their dedicated pins, the smallest capacitor value being placed first.

Wide tracks or planes must be used for power supplies wherever is possible.

6.4 Oscillator section

The ST8500 requires one 25 MHz quartz crystals connected to the internal oscillator. See the ST8500 datasheet for crystal characteristics. The frequency tolerance has to be chosen according to the specific PLC protocol requirements.

The reference part number, selected according to the most stringent requirements from the G3 specifications, is TXC 7M25070054 (± 10 ppm tolerance, ± 15 ppm stability).

It is very important to keep the crystal as close as possible to the ST8500 device. The oscillator circuit must be far away from noise sources such as

- Power supply switching circuitry
- Burst and surge protections
- Line coupling circuits
- Any PCB track or via carrying an RF switching signal

To properly shield and separate the oscillator section from the rest of the board, it is recommended to use a ground plane filling all the area around and below the crystal oscillator. No vias or tracks, except for the crystal connections, should cross the ground plane.

Connecting the case to ground could be a good practice to reduce the effect of radiated signals on the oscillator.

The load capacitors C106 and C109 have been selected in order to center the 25 MHz oscillator, taking into account the additional capacitive load by the ST8500 pins and PCB. Those values may have to be adjusted for any design using a different PCB layout and crystal.

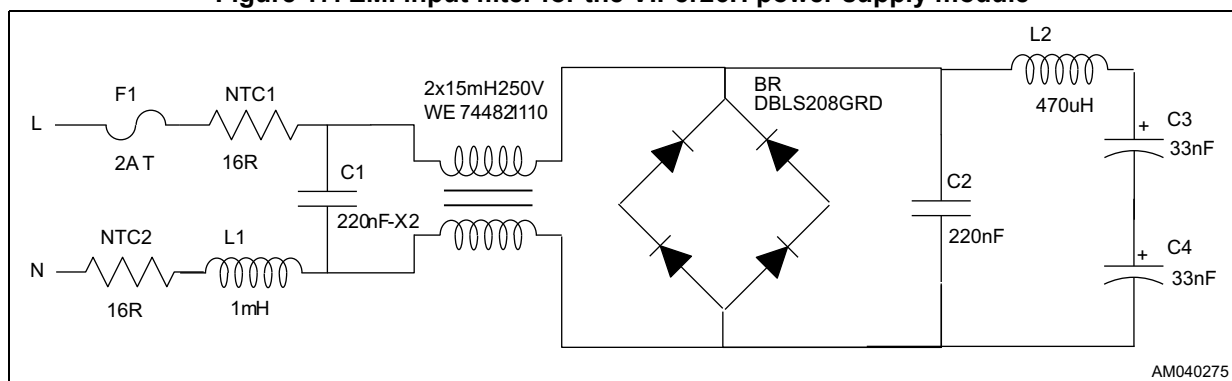
6.5 Power supply EMI filter

The power supply circuit design is not only relevant in terms of available power. Two points are particularly sensitive for a power line communication application

- The noise injected on the line
- The input impedance of the power supply unit

Both points involve the EMI input filter design. The circuit of [Figure 17](#) has been designed to have minimum influence on the ST8500 and STLD1 performance, in terms of load impedance and linearity, while guaranteeing very low conducted emissions.

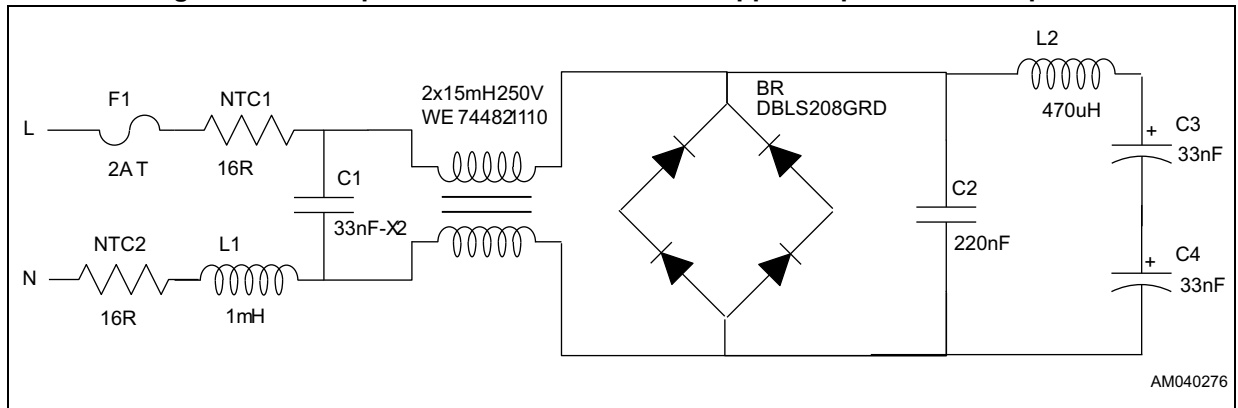
Figure 17. EMI input filter for the VIPer26H power supply module



Note: *In case of metering applications, an apparent power consumption limit of 10 VA exists, based on the IEC 62053-21 and 62053-22. This forces to reduce the value of the C1 in the EMI filter to 33 nF to be compliant, see [Figure 18](#).*

While not impacting the EMC performance and immunity, this modification may have a limited impact on PLC receiver sensitivity in very low-noise network conditions, even if this will become negligible in most real-field installations due to average mains noise much higher than the noise produced by the PSU.

Figure 18. EMI input filter modified to reduce apparent power consumption



7 EN50065 compliance tests

[Table 5](#) lists all the EMC/EMI compliance tests required by the European standard EN50065 for smart metering PLC applications on the low voltage distribution network (which have the highest EMC test levels among all low voltage appliances).

All applicable tests have been carried out on the ST8500 evaluation kit. Full EMC compliance to EN50065-1, EN50065-2-3 and EN50065-7 has been tested with the G3-PLC FW implementation.

All immunity tests require a communication link to be established between the equipment under test (EUT) and a stimulus device. During such tests, the presence of a live PLC communication is monitored to verify the acceptance criteria according to the specific test.

Table 5. List of standard tests required for EMC compliance to EN50065 - A-band PLC applications

Type	Basic standard	Test	Result
PLC transmission: conducted measurement	EN 50065-1	Bandwidth measurements	PASS ⁽¹⁾
	EN 50065-1	Maximum output levels	PASS ⁽¹⁾
Conducted disturbance measurements	EN 50065-1, EN 55022	Conducted emissions (9 kHz - 30 MHz)	PASS ^{(1), (2)}
Radiated disturbance measurements	EN 50065-1, EN 55022	Radiated emissions (30 MHz - 1 GHz)	PASS ⁽²⁾
Radiated immunity	EN 61000-4-3	RF radiated fields immunity test (80 - 1000 MHz, 10 V/m)	PASS
	EN 61000-4-8	Magnetic 50 Hz field immunity test (100 A/m, 300 A/m)	PASS
Contact/radiated immunity	EN 61000-4-2	Electro-static discharges immunity test (8 kV contact and air mode)	PASS ⁽³⁾
Conducted immunity	EN 61000-4-6	RF conducted signals immunity test (150 kHz - 80 MHz, 10 V rms)	PASS ⁽³⁾
	EN 50065-2-3	Narrow-band signals immunity test (95 kHz - 150 kHz; 150 kHz - 30 MHz)	PASS ⁽³⁾
	EN 61000-4-4	Fast transients immunity test (2 kV, 5 kHz)	PASS ⁽³⁾
	EN 61000-4-5	Surge immunity test (4 kV, common mode and differential mode)	PASS ⁽³⁾
	EN 61000-4-11	Power voltage dips and interruptions (30% - 10 ms; 60% - 100 ms; 100% - 5 s)	PASS ⁽³⁾
Input impedance measurement	EN50065-7	RX impedance	PASS ^{(1), (2)}
		TX impedance	PASS ⁽¹⁾

1. Related to the specific PLC protocol implementation.

2. Results impacted by the VIPer26H power supply module.

3. In case of non-metering applications, communicating outside the CENELEC A band, please refer to the immunity requirements listed in the EN50065-2-1 document, which may set lower limits for some tests.

8 Normative references

EN50065: signaling on low voltage electrical installations in the frequency range from 3 kHz to 148.5 kHz

- Part 1: general requirements, frequency bands and electromagnetic disturbances
- Part 2 - 3: immunity requirements
- Part 7: equipment impedance

IEC 62053: electricity metering equipment (a.c.) - particular requirements

- Part 21: static meters for active energy (classes 1 and 2)
- Part 22: static meters for active energy (classes 0,2 S and 0,5 S)

9 Document references

- ST8500 datasheet
- STLD1 datasheet
- EVALKITST8500-1 schematics
- EVALKITST8500-1 layout
- EVALKITST8500-1 BOM

10 Revision history

Table 6. Document revision history

Date	Revision	Changes
15-Dec-2017	1	Initial release.
25-Jun-2018	2	Updated Section 6 on page 18 (added Debug requirements for end applications).

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