AN4832
Application note

Migrating from STM32F303 line to STM32L4 Series and STM32L4+ Series microcontrollers

Introduction

For the designers of the STM32 microcontroller applications, being able to easily replace one microcontroller type by another in the same product family is an important asset. Migrating an application to a different microcontroller is often needed when the product requirements grow putting extra demands on the memory size or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and to shrink the PCB area.

This application note analyzes the steps required to migrate an existing design from STM32F303 line devices to STM32L4 Series / STM32L4+ Series microcontrollers. This document lists the full set of features available for STM32F303 line and the equivalent features on STM32L4 Series and STM32L4+ Series.

In order to migrate an application to STM32L4 Series / STM32L4+ Series, four aspects need to be considered: the hardware migration, the peripheral migration, the firmware migration and the software migration.

To fully benefit from this application note, the user must be familiar with the STM32 microcontrollers documentation available on *www.st.com*, with a particular focus on:

- The STM32F303 line reference manuals:
  - STM32F303xB/C/D/E, STM32F303x6/8, STM32F328x8, STM32F358xC, STM32F398xE advanced Arm®-based MCUs (RM0316)
- The STM32F303 line datasheets:
  - STM32F303xB STM32F303xC *Arm®-based Cortex®-M4 32b MCU+FPU, up to 256 Kbytes Flash+ 48 Kbytes SRAM, 4 ADCs, 2 DAC ch., 7 comp, 4 PGA, timers, 2.0-3.6 V* (DS9118)
  - STM32F303xD STM32F303xE *Arm® Cortex®-M4 32b MCU+FPU, up to 512 Kbytes Flash, 80 Kbytes SRAM, FSMC, 4 ADCs, 2 DAC ch., 7 comp, 4 Op-Amp, 2.0-3.6 V* (DS10362)
  - STM32F303x6/x8 *Arm® Cortex®-M4 32b MCU+FPU, up to 64 Kbytes Flash, 16 Kbytes SRAM 2 ADCs, 3 DACs, 3 comp., op-amp 2.0 - 3.6 V* (DS9866)
- The STM32L4 Series reference manuals:
  - RM0351 (STM32L4x6xx, STM32L4x5xx)
  - RM0394 (STM32L43xxx, STM32L44xxx, STM32L45xxx, STM32L46xxx)
  - RM0392 (STM32L471xx)
- The STM32L4 Series datasheets
- The STM32L4+ Series reference manual:
  - RM0432 (STM32L4Rxxx, STM32L4Sxxx)
- The STM32L4+ Series datasheets.

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1 STM32L4 Series and STM32L4+ Series overview

The STM32L4 Series and STM32L4+ Series devices provide a perfect fit in terms of ultra-low-power, performances, memory size and peripherals at a cost effective price.

In particular, the STM32L4 Series and STM32L4+ Series microcontrollers allow a high frequency/performance operation including the Arm®(a) Cortex®-M4 @ up to 120 MHz and an optimized Flash memory access through the adaptive real-time memory accelerator (ART Accelerator™).

The STM32L4 Series and STM32L4+ Series devices increase the low-power efficiency in dynamic mode (µA/MHz) and still reach a very low level of static power consumption on various available low-power modes.

The detailed list of available features and packages for each product is available in the respective datasheets.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 1 lists the memory availability for each product.

Table 1. STM32L4 Series and STM32L4+ Series memory availability

Part number	Flash size		Ram size		
	Size	Bank	SRAM1	SRAM2	SRAM3
STM32L4S9xx	2 Mbytes	Dual	192 Kbytes	64 Kbytes	384 Kbytes
STM32L4R9xx					
STM32L4S7xx					
STM32L4R7xx					
STM32L4S5xx					
STM32L4R5xx					
STM32L496xx	1 Mbyte	dual	256 Kbytes	64 Kbytes	-
STM32L4A6xx					
STM32L476xx	1 Mbyte	dual	96 Kbytes	32 Kbytes	-
STM32L486xx					
STM32L471xx					
STM32L475xx					
STM32L451xx	512 Kbytes	single	128 Kbytes	32 Kbytes	-
STM32L452xx					
STM32L462xx					
STM32L433xx	256 Kbytes	single	48 Kbytes	16 Kbytes	-
STM32L443xx					
STM32L432xx					
STM32L442xx					
STM32L431xx					

The STM32L4 Series and STM32L4+ Series devices include a larger set of peripherals with advanced features compared to the STM32F303 line ones, such as:

- Advanced encryption hardware accelerator (AES)
- Single wire protocol interface (SWPMI) (not available on STM32L4+ Series)
- Serial audio interface (SAI)
- Low-power UART (LPUART)
- Low-power timer (LPTIM)
- Liquid crystal display controller (LCD) (not available on STM32L4+ Series)
- Digital filter for sigma delta modulators (DFSDM) (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L47xxx/48xxx and STM32L45xxx/46xxx)
- Voltage reference buffer (VREFBUF)
- Digital to analog converter with low power Sample and Hold feature (DAC)
- Quad-SPI interface (QUADSPI) (not available on STM32L4+ Series)
- Firewall (FW)
- Clock recovery system (CRS) for USB (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx)
- SRAM1 size is different on the various STM32L4 Series / STM32L4+ Series devices:
  - 192 Kbytes for STM32L4+ Series
  - 256 Kbytes for STM32L49xxx/4Axxx
  - 96 Kbytes for STM32L47xxx/48xxx
  - 128 Kbytes for STM32L45xxx/46xxx
  - 48 Kbytes for STM32L43xxx/44xxx
- Additional SRAM2 with data preservation in Standby mode:
  - 64 Kbytes for STM32L4+ Series and STM32L49xxx/4Axxx
  - 32 Kbytes for STM32L47xxx/48xxx and STM32L45xxx/46xxx
  - 16 Kbytes for STM32L43xxx/44xxx
- Additional SRAM3 for STM32L4+ Series:
  - 384 Kbytes
- Dual bank boot and 8-bit ECC on Flash memory (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
- Optimized power consumption and enriched set of low-power mode

The STM32L45xxx/46xxx and STM32L43xxx/44xxx devices implement an USB FS device only instead of an USB OTG FS. They also implement reduced Flash memory size (512 Kbytes for STM32L45xxx/46xxx and 256 Kbytes for STM32L43xxx/44xxx).

This migration guide is only covering the migration from STM32F303 line to STM32L4 Series / STM32L4+ Series. As a consequence the new features present on STM32L4 Series and STM32L4+ Series but not already present on STM32F303 line are not covered (refer to the STM32L4 Series and STM32L4+ Series reference manuals and datasheets for an exhaustive overview).

2 Hardware migration

2.1 Package availability

The STM32F303 line and the STM32L4 Series / STM32L4+ Series devices have a wide selection of packages. STM32F303 line offers spreads from 32 to 144 pins packages and STM32L4 Series / STM32L4+ Series offer spreads from 32 to 169 pin packages.

The available packages in the STM32L4 Series and STM32L4+ Series are listed in *Table 2*.

Table 2. Packages available on STM32L4 Series and STM32L4+ Series

Package[1]	STM32L4+ Series	STM32L4 Series				Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx		
UFQFPN32	-	-	-	-	X	(5 x 5)	STM32L432xx, STM32L442xx, STM32L431xx
LQFP48	-	-	-	-	X	(7 x 7)	STM32L433xx, STM32L443xx, STM32L431xx
UFQFPN48	-	-	-	X	X	(7 x 7)	STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L431xx
WLCSP49	-	-	-	-	X	(3.141 x 3.127)	STM32L433xx, STM32L443xx, STM32L431xx
WLCSP64	-	-	-	-	X	(3.141 x 3.127)	STM32L433xx, STM32L443xx, STM32L431xx
LQFP64	-	X	X	X	X	(10 x 10)	STM32L433xx, STM32L443xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L431xx, STM32L471xx, STM32L475xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series				Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx		
UFBGA64	-	-	-	X	X	(5 x 5)	STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L431xx
WLCSP64	-	-	-	X	-	(3.357 x 3.657)	STM32L451xx, STM32L452xx, STM32L462xx
WLCSP72	-	-	X	-	-	(4.4084 x 3.7594)	STM32L476xx, STM32L486xx, STM32L471xx, STM32L475xx
WLCSP81	-	-	X	-	-	(4.4084 x 3.7594)	STM32L476xx
WLCSP100	-	X	-	-	-	(4.618 x 4.142)	STM32L496xx, STM32L4A6xx
LQFP100	X	X	X	X	X	(14 x 14)	STM32L433xx, STM32L443xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L431xx, STM32L471xx, STM32L475xx, STM32L4R5xx, STM32L4S5xx, STM32L4R9xx, STM32L4S9xx
UFBGA100	-	-	X	X	X	(7 x 7)	STM32L433xx, STM32L443xx, STM32L431xx
UFBGA132	X	X	X	-	-	(7 x 7)	STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L471xx, STM32L475xx, STM32L4R5xx, STM32L4S5xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series				Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx		
UFBGA144	X	-	-	-	-	(10 x 10)	STM32L4R9xx, STM32L4S9xx
LQFP144	X	X	X	-	-	(20 x 20)	STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L471xx, STM32L475xx, STM32L4R5xx, STM32L4S5xx, STM32L4R9xx, STM32L4S9xx
WLCSP144	X	-	-	-	-	(5.24 x 5. 24)	STM32L4R5xx, STM32L4S5xx, STM32L4R7xx, STM32L4S7xx, STM32L4R9xx, STM32L4S9xx
UFBGA169	X	X	-	-	-	(7 x 7)	STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4S5xx, STM32L4R9xx, STM32L4S9xx

1. X = supported.

The available packages in the STM32F303 line are listed in *Table 3*.

Table 3. Package availability on STM32F303 line

Package[1]	STM32F303 line		
	STM32F303xB/C	STM32F303xD/E	STM32F303x6/8
UFQFPN32	-	-	-
UFQFPN48	-	-	-
WLCSP49	-	-	-
WLCSP64	-	-	-
WLCSP72	-	-	-
WLCSP81	-	-	-
WLCSP100	X	X	-
LQFP32	-	-	X
LQFP48	X	-	X

Table 3. Package availability on STM32F303 line (continued)

Package[1]	STM32F303 line		
	STM32F303xB/C	STM32F303xD/E	STM32F303x6/8
LQFP64	X	X	X
LQFP100	X	X	-
LQFP144	-	X	-
UFBGA64	-	-	-
UFBGA100	-	X	-
UFBGA132	-	-	-

1. X = supported.

For a detailed package availability and package selection, refer to the STM32F303 line and to the STM32L4 Series and STM32L4+ Series microcontrollers documentation available on *www.st.com.*

Both families share a high level of pin compatibility. Most of the peripherals share the same pins. The transition between the two families is easy since only a few pins are impacted.

Table 4 and *Table 5* compare the pinout between STM32F303 line and STM32L4 Series / STM32L4+ Series for the 48, 64, 100 and 144 pin packages.

Table 4. STM32F303 line and STM32L4 Series and STM32L4+ Series pinout differences (QFP)

STM32F303 line					STM32L4 Series STM32L4+ Series				
QFP 48	QFP 64	QFP 100	QFP 144	Pinout	QFP 48	QFP 64	QFP 100	QFP 144	Pinout
-	-	-	10	**PH0**	-	-	-	10	**PF0** (1)(2)
-	-	-	11	**PH1**	-	-	-	11	**PF1** (1)(2)
-	-	10	-	**PF9**	-	-	10	-	**VSS** (1)(3)(4)
-	-	11	-	**PF10**	-	-	11	-	**VDD** (1)(3)(4)
5	5	12	23	**PF0-OSC_IN**	5	5	12	23	**PH0-OSC_IN** (1)(2)(3)(4)
6	6	13	24	**PF1-OSC_OUT**	6	6	13	24	**PH1-OSC_OUT** (1)(2)(3)(4)
-	-	19	-	**PF2**	-	-	19	-	**VSSA** (1)(2)(3)(4)
-	-	20	-	**VSSA/VREF-**	-	-	20	-	**VREF-** (1)(2)(3)(4)
-	-	27(5)	-	**PF4**	-	-	27	-	**VSS** (1)(2)(3)(4)
-	-	73	-	**PF6**	-	-	73	-	**VDDUSB** (1)(2)(3)(4)(6)
36	48	-	-	**VDD**	36	48	-	-	**VDDUSB** (1)(2)(3)(4)(6)
-	-	-	95	**VDD**	-	-	-	95	**VDDIO2** (1)(2)(6)
-	-	-	106	**PH2**	-	-	-	106	**VDDUSB** (1)(2)(6)
-	-	-	131	**VDD**	-	-	-	131	**VDDIO2** (1)(2)(6)
44	60	94	138	**BOOT0**	44	60	94	138	**PH3/BOOT0** (1)(3)(4)

1. For STM32L4R5xx/4S5xx/4R7xx/4S7xx and STM32L49xxx/4Axxx.
2. For STM32L47xxx/48xxx.
3. For STM32L45xxx/46xxx.
4. For STM32L43xxx/44xxx.
5. For STM32F303xB/C.
6. VDDUSB and VDDIO2 pins can be connected externally to VDD.

Note: STM32L4R9xx/4S9xx are not compatible with STM32L4 Series, for more details, refer to application note Migration between STM32L476xx/486xx and STM32L4+ Series microcontrollers (AN5017).

Table 5. STM32F303 line and STM32L4 Series / STM32L4+ Series pinout differences (BGA)

STM32F303 line		STM32L4 Series STM32L4+ Series	
UFBGA100	**Pinout**	**UFBGA100**	**Pinout**
D1	**PC14**	D1	**PC14-OSC32_IN**(1)(2)
E1	**PC15**	E1	**PC14_OSC_OUT**(1)(2)
F1	**PF0-OSC_IN**	F1	**PH0-OSC_IN**(1)(2)
G1	**PF1-OSC_OUT**	G1	**PH1-OSC_OUT**(1)(2)
J1	**PF2**	J1	**VSSA**(1)(2)
K1	**VSSA/VREF-**	K1	**VREF-**(1)(2)
L1	**VDDA**	L1	**VREF+**(1)(2)
M1	**VREF+**	M1	**VDDA**(1)(2)
F2	**PF9**	F2	**VSS**(1)(2)
G2	**PF10**	G2	**VDD**(1)(2)
A4	**BOOT0**	A4	**PH3/BOOT0**(1)(2)
C11	**PF6**	C11	**VDDUSB**(1)(2)(3)

1. For STM32L45xxx/46xxx devices.
2. For STM32L43xxx/44xxx devices.
3. VDDUSB and VDDIO2 pins can be connected externally to VDD.

Recommendations to migrate board from STM32F303 line to STM32L4 Series / STM32L4+ Series

A dedicated V_{DDUSB} supply is used in STM32L4 Series / STM32L4+ Series. It must be connected to the VDDUSB pin (pin 48 on QFP64, pin 73 on QFP100, pin 36 on QFPN48 and pin C11 on BGA100).

Find below in *Figure 1* the STM32L47xxx/48xxx tips for LQFP64 and FQFP100 packages.

Figure 1. Compatible board design: LQFP64

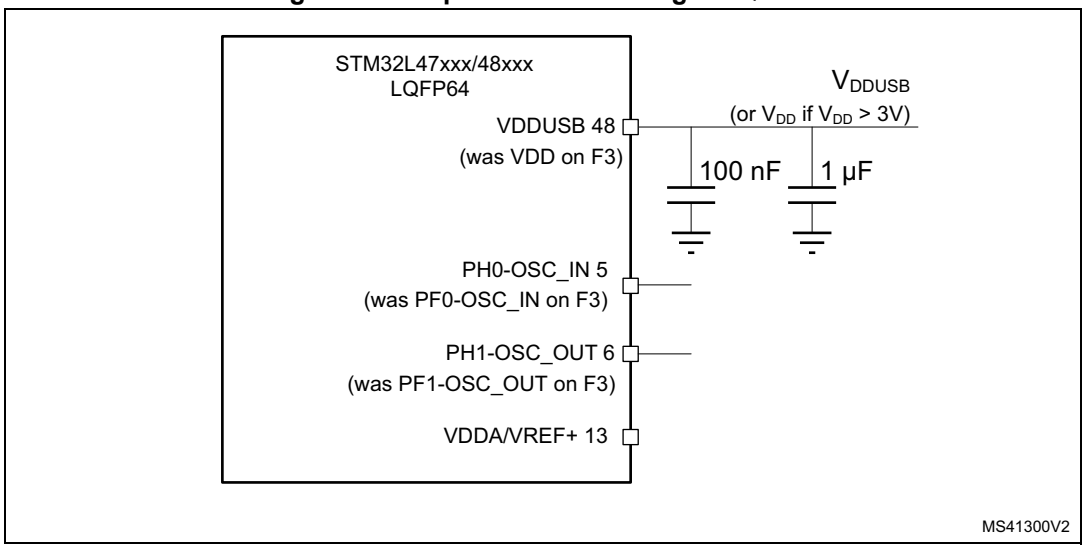
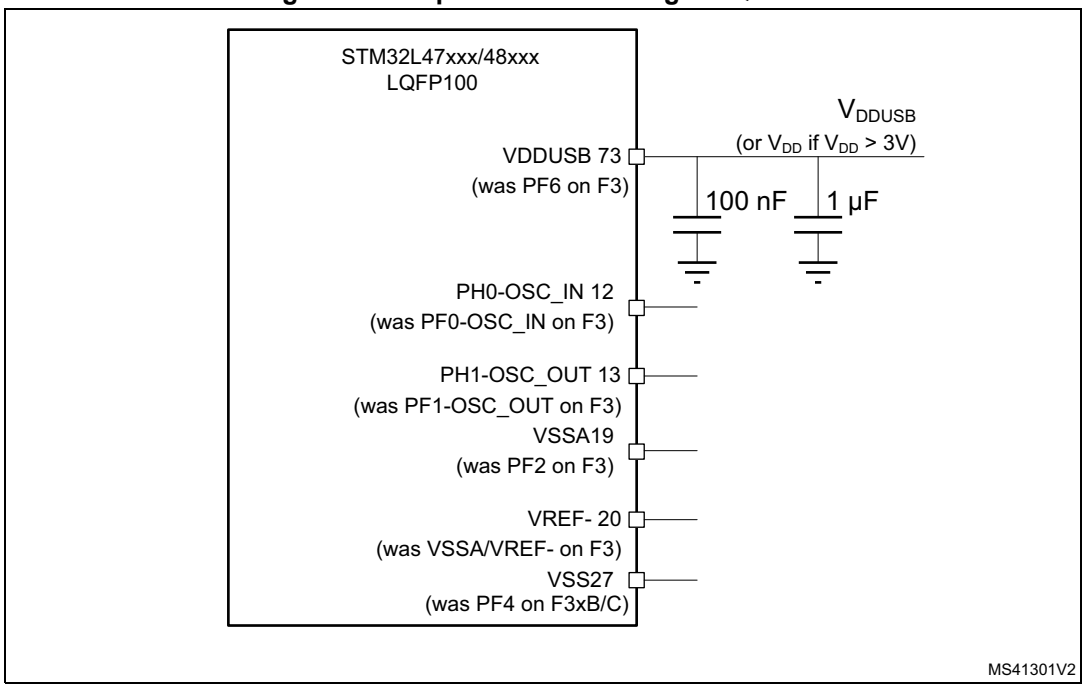


Figure 2. Compatible board design: LQFP100



See also *Getting started with STM32L4 Series and STM32L4+ Series hardware development* application note (AN4555).

SMPS packages

Some STM32L4 Series and STM32L4+ Series devices offer a package option allowing the connection of an external SMPS. This is done through two VDD12 pins that are replacing two existing pins in the package baseline.

The compatibility is kept between the STM32L4 derivatives regarding those two pins (the pins replaced are different across the package types but are the same for all the derivatives on similar packages). Refer to the product datasheet for details.

3 Boot mode selection

The STM32F303 line and the STM32L4 Series / STM32L4+ Series devices can select the boot modes between three options: boot from main Flash memory, boot from SRAM or boot from system memory. However, the way to select the boot mode differs between the products.

In STM32F303 line, the boot mode is selected with the pin BOOT0 and the option bit nBOOT1 located in the user option bytes at the memory address 0x1FFF 7800.

In STM32L47xxx/48xxx, the boot mode is selected with 1 pin BOOT0 and the nBOOT1 option bit located in the user option bytes at memory address 0x1FFF 7800.

In STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx, the boot mode is selected with nBOOT1 option bit and pin BOOT0 or nBOOT0 option bit depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register as shown in *Table 6*.

Table 6 and *Table 7* summarize the different configurations available for selecting the boot mode.

Table 6. Boot modes for STM32L47xxx/48xxx devices and STM32F303 line

Boot mode selection(1)		Boot mode	Aliasing
BOOT1(2)	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM1 (SRAM for STM32F303 line)	Embedded SRAM1 is selected as boot space (SRAM for STM32F303 line)

1. X= equivalent to 0 or 1.
2. The BOOT1 value is the opposite of the nBOOT1 option bit.

Table 7. Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx devices

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOO0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main flash empty(1)	Boot memory space alias
X	X	0	1	0	Flash memory selected as boot area
X	X	0	1	1	System memory selected as boot area
X	1	X	0	X	Flash memory selected as boot area
0	X	1	1	X	Embedded SRAM1 selected as boot area

Table 7. Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx devices (continued)

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOO0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main flash empty(1)	Boot memory space alias
0	0	X	0	X	Embedded SRAM1 selected as boot area
1	X	1	1	X	System memory is selected as boot area
1	0	X	0	X	System memory is selected as boot area

1. Only for the STM32L45xxx/46xxx and STM32L43xxx/44xxx devices: a Flash empty check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed (0xFFFF FFFF) and if the boot selection is configured to boot from the main Flash memory.

Embedded boot loader

The embedded boot loader is located in the system memory and programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 8. Bootloader interfaces

Peripheral	Pin	STM32F303 line			STM32L4 Series / STM32L4+ Series
		C/B	D/E	6/8	-
DFU	USB_DM (PA11) USB_DP (PA12)	X	X	-	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	X	-	-	-
	USART2_TX (PA2) USART2_RX (PA3)	-	X	X	X
USART3	USART3_TX (PC10) USART3_RX (PC11)	-	-	-	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	-	X	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	-	-	X
I2C3	I2C3_SCL (PC0) I2C3_SDA (PC1)	-	-	-	X
I2C4	I2C4_SCL (PD12)	-	-	-	X
	I2C4_SDA (PD13)	-	-	-	X(1)

Table 8. Bootloader interfaces (continued)

Peripheral	Pin	STM32F303 line			STM32L4 Series / STM32L4+ Series
		C/B	D/E	6/8	-
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	-	-	-	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	-	-	X
CAN1	CAN1_RX (PB8) CAN1_TX (PB9)	-	-	-	X
CAN2	CAN2_RX (PB5) CAN2_TX (PB6)	-	-	-	X(2)

1. Only for STM32L49xxx/4Axxx and STM32L45xxx/46xxx devices.
2. Only for STM32L49xxx/4Axxx devices.

For more details on the bootloader, refer to *STM32 microcontroller system memory boot mode* application note (AN2606).

For smaller packages, it is important to check the pin and peripheral availability.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals that can be classified in three groups:

- The first group is for the peripherals that are common to all products. Those peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second group is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third group is for peripherals which have been considerably modified from one product to another (new architecture, new features...). For this last group of peripherals, the migration will require new developments at application level.

Table 9 gives a general overview of this classification. The “software compatibility” mentioned in *Table 9* refers to the register description for “low level” drivers.

The STMCube™ hardware abstraction layer (HAL) between STM32F303 line and STM32L4 Series / STM32L4+ Series is compatible.

Table 9. STM32 peripheral compatibility analysis
STM32F303 line compared to STM32L4 Series / STM32L4+ Series

<table>
<tr><th rowspan="2">Peripheral</th><th colspan="6">Nb inst. in STM32</th><th colspan="3">Compatibility with STM32L4 Series / STM32L4+ Series</th></tr>
<tr><th>STM32F303 line</th><th>L4Rxxx/ 4Sxxx</th><th>L49xxx /4Axxx</th><th>L47xxx /48xxx</th><th>L45xxx /46xxx</th><th>L43xxx /44xxx</th><th>Software</th><th>Pinout</th><th>Comments</th></tr>
<tr><td>SPI</td><td>4</td><td colspan="5">3</td><td rowspan="2">Partial</td><td rowspan="2">Partial</td><td rowspan="2">– I2S is no longer supported by SPI and it is replaced by a dedicated serial audio interface (SAI) on STM32L4 Series and STM32L4+ Series
– Some alternate functions are not mapped on the same GPIO for SPI2/SPI3</td></tr>
<tr><td>I2S (full duplex)</td><td>0</td><td colspan="5">0</td></tr>
<tr><td>WWDG</td><td>1</td><td colspan="5">1</td><td rowspan="4">Full</td><td rowspan="4">NA</td><td>-</td></tr>
<tr><td>IWDG</td><td>1</td><td colspan="5">1</td><td>-</td></tr>
<tr><td>DBGMCU</td><td>1</td><td colspan="5">1</td><td>-</td></tr>
<tr><td>CRC</td><td>1</td><td colspan="5">1</td><td>-</td></tr>
</table>

Table 9. STM32 peripheral compatibility analysis
STM32F303 line compared to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	Nb inst. in STM32						Compatibility with STM32L4 Series / STM32L4+ Series		
	STM32F303 line	L4Rxxx/ 4Sxxx	L49xxx /4Axxx	L47xxx /48xxx	L45xxx /46xxx	L43xxx /44xxx	Software	Pinout	Comments
EXTI	1	1					Partial	Full	Only PH2 GPIO not available as EXTI input on STM32L4 Series / STM32L4+ Series
USB OTG FS	0	1			0		NA	NA	-
USB FS	1	0			1		Partial	Partial	Additional features on STM32L4 Series and STM32L4+ Series
DMA	2	2					Partial	NA	Different features and DMA mapping requests differ (see *Section 4.3: Direct memory access controller (DMA)*)
TIM Basic General P. Advanced Low-power IRTIM	 2 6 3 0 1	 2 7 2 2 1			 2 4 1 2 1	 2 3 1 2 1	Full	Partial	– Some pins are not mapped on the same GPIO – Timer instance names may differ – Internal connections may differ
SDIO/ SDMMC	0	1					NA	NA	-
PWR	1	1					Partial	NA	-
RCC	1	1					Partial	NA	-
USART **UART** **LPUART**	3 2 0	3 2 1			3 1 1	3 0 1	Full (NA for LPUART)	Full (NA for LPUART)	-
I2C	3	4		3	4	3	Full	Partial	– Fully compatible pinout for I2C1/2 – I2C3 mapped on different GPIOs – Additional features
ADC	4	1	3		1		Partial	Partial	– Additional features – Some ADC channels mapped on different GPIOs

Table 9. STM32 peripheral compatibility analysis
STM32F303 line compared to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	Nb inst. in STM32						Compatibility with STM32L4 Series / STM32L4+ Series		
	STM32F 303 line	L4Rxxx/ 4Sxxx	L49xxx /4Axxx	L47xxx /48xxx	L45xxx /46xxx	L43xxx /44xxx	Software	Pinout	Comments
RTC	1	1					Partial	Full	Additional features
FLASH	1	1					None	NA	New peripheral
GPIO	Up to 115 IOs	Up to 140 IOs	Up to 136 IOs	Up to 114 IOs	Up to 83 IOs	Up to 83 IOs	Full	Full	Reset configuration: – STM32F303 line: input floating mode – STM32L4 Series / STM32L4+ Series: analog mode
SYSCFG	1	1					Partial	NA	-
CAN	1	1	2	1			Partial	Full	CAN2 is only available on STM32L49xxx/4Axxx
DAC channels	3	2			1		Partial	Partial	Additional feature
FMC	1	1			0		Full	Full	– PC card interface not supported on STM32L4 Series / STM32L4+ Series – NAND supported on STM32L4 Series / STM32L4+ Series
COMP	7 (B/C/D/E) 3 (6/8)	2					None	Partial	Some pins mapped on different GPIO
OPAMP	4 (B/C/D/E) 1 (6/8)	2			1		None	Partial	– Some pins mapped on different GPIOs – One less OPAMP on STM32L4 Series / STM32L4+ Series

Color key:

= No compatibility (new feature or new architecture)

= Partial compatibility (minor changes)

= Not applicable

4.2 Memory mapping

The peripheral address mapping has been changed in STM32L4 Series / STM32L4+ Series compared to STM32F303 line.

Table 10 provides the peripheral address mapping correspondence between STM32F303 line and STM32L4 Series / STM32L4+ Series.

Table 10. Peripheral address mapping differences

Peripheral	STM32F303xB/C/D/E/6/8 lines		STM32L4 Series STM32L4+ Series	
	Bus	Base Address	Bus	Base Address
FSMC control register	-	-	AHB3	0xA000 0000(2)
FMC control registers	AHB4	0xA000 0400	-	-
FMC banks 3 and 4		0x8000 0400	-	-
FMC banks 1 and 2		0x6000 0000	-	-
RNG	-	-	AHB2	0x5006 0800
AES	-	-		0x5006 0000
ADC	-	-		0x5004 0000
USB OTG FS	-	-		0x5000 0000(2)
ADC3 - ADC4	AHB3	0x5000 0400	-	-
ADC1 - ADC2		0x5000 0000	-	-
GPIOI	-	-	AHB2	0x4800 2000(1)
GPIOH	AHB2	0x4800 1C00		0x4800 1C00
GPIOG		0x4800 1800		0x4800 1800(2)
GPIOF		0x4800 1400		0x4800 1400(2)
GPIOE		0x4800 1000		0x4800 1000
GPIOD		0x4800 0C00		0x4800 0C00
GPIOC		0x4800 0800		0x4800 0800
GPIOB		0x4800 0400		0x4800 0400
GPIOA		0x4800 0000		0x4800 0000
TSC	AHB1	0x4002 4000		0x4002 4000
CRC		0x4002 3000	AHB1	0x4002 3000
Flash interface		0x4002 2000		0x4002 2000
RCC		0x4002 1000		0x4002 1000
DMA2		0x4002 0400		0x4002 0400
DMA1		0x4002 0000		0x4002 0000
DFSDM	-	-	APB2	0x4001 6000(2)
SAI2	-	-		0x4001 5800(2)
SAI1	-	-		0x4001 5400

Table 10. Peripheral address mapping differences (continued)

Peripheral	STM32F303xB/C/D/E/6/8 lines		STM32L4 Series STM32L4+ Series	
	Bus	Base Address	Bus	Base Address
TIM20	APB2	0x4001 5000	-	-
TIM17		0x4001 4800	APB2	0x4001 4800(2)
TIM16		0x4001 4400		0x4001 4400
TIM15		0x4001 4000		0x4001 4000
SPI4		0x4001 3C00	-	-
USART1		0x4001 3800	APB2	0x4001 3800
TIM8		0x4001 3400		0x4001 3400(2)
SPI1		0x4001 3000		0x4001 3000
TIM1		0x4001 2C00		0x4001 2C00
SDMMC1	-	-		– 0x40012800 – 0x50062400 (AHB2) on STM32L4+ Series
FIREWALL	-	-		0x4001 1C00
EXTI	APB2	0x4001 0400		0x4001 0400
SYSCFG + COMP + OPAMP		0x4001 0000	-	-
COMP	-	-	APB2	0x4001 0200
VREFBUF	-	-		0x4001 0030
SYSCGF	-	-		0x4001 0000
DAC1_CH2	APB1	0x4000 9800	-	-
LPTIM1	-	-	APB1	0x4000 9400
SWPMI1	-	-		0x4000 8800
LPUART1	-	-		0x4000 8000
LPTIM1	-	-		0x4000 7C00
I2C4	-	-		0x4000 8400
I2C3	APB1	0x4000 7800	-	-
OPAMP	-	-	APB1	0x4000 7800
DAC1_CH1	APB1	0x4000 7400		0x4000 7400
PWR		0x4000 7000		0x4000 7000
bxCAN		0x4000 6400	-	-
CAN1	-	-	APB1	0x4000 6400
CAN2	-	-		0x4000 6800

Table 10. Peripheral address mapping differences (continued)

Peripheral	STM32F303xB/C/D/E/6/8 lines		STM32L4 Series STM32L4+ Series	
	Bus	Base Address	Bus	Base Address
USB/CAN SRAM	APB1	0x4000 6000	-	-
USB device FS		0x4000 5C00	-	-
I2C3	-	-	APB1	0x4000 5C00
I2C2	APB1	0x4000 5800		0x4000 5800
I2C1		0x4000 5400		0x4000 5400
UART5		0x4000 5000		0x4000 5000(2)
UART4		0x4000 4C00		0x4000 4C00(2)
USART3		0x4000 4800		0x4000 4800
USART2		0x4000 4400		0x4000 4400
I2S3ext		0x4000 4000	-	-
SPI3/I2S3		0x4000 3C00	APB1	0x4000 3C00
SPI2/I2S2		0x4000 3800		0x4000 3800
I2S2ext		0x4000 3400	-	-
IWDG		0x4000 3000	APB1	0x4000 3000
WWDG		0x4000 2C00		0x4000 2C00
RTC		0x4000 2800		0x4000 2800
LCD	-	-		0x4000 2400
TIM7	APB1	0x4000 1400		0x4000 1400
TIM6		0x4000 1000		0x4000 1000
TIM5	-	-		0x4000 0C00(2)
TIM4	APB1	0x4000 0800		0x4000 0800(2)
TIM3		0x4000 0400		0x4000 0400(2)
TIM2		0x4000 0000		0x4000 0000
USB SRAM	-	-		0x4000 6C00(3)
USB FS	-	-		0x4000 6800(3)
CRS	-	-		0x4000 6000(3)
OCTOSPI2	-	-	AHB3	0xA000 1400
OCTOSPI	-	-		0xA000 1000
OCTOSPIM	-	-	AHB2	0x5006 1C00
GFXMMU	-	-	AHB1	0x4002 C000
DMAMUX1	-	-		0x4002 0800

Table 10. Peripheral address mapping differences (continued)

Peripheral	STM32F303xB/C/D/E/6/8 lines		STM32L4 Series STM32L4+ Series	
	Bus	Base Address	Bus	Base Address
DSIHOST	-	-	APB2	0x4001 6C00
LCD-TFT	-	-		0x4001 6800
Color key: = new peripheral				

1. Only for STM32L496xx/4A6xx.
2. Not Applicable for STM32L43xxx/44xxx.
3. Only for STM32L43xxx/44xxx.

Regarding the SRAM

The STM32F303xB/C devices feature up to 48 Kbytes of embedded SRAM with the hardware parity check.

- 8 Kbytes of CCM (core coupled memory) RAM mapped on both instruction and data bus, used to execute critical routines or to access data (parity check on all of CCM RAM).
- 40 Kbytes of SRAM mapped on the data bus (parity check on first 16 Kbytes of SRAM).

The STM32F303xD/E devices feature 80 Kbytes of embedded SRAM with the hardware parity check.

- 16 Kbytes of CCM SRAM mapped on both instruction and data bus, used to execute critical routines or to access data (parity check on all of CCM SRAM).
- 64 Kbytes of SRAM mapped on the data bus (parity check on first 32 Kbytes of SRAM).

The STM32F303x6/8 devices feature 16 Kbytes of embedded SRAM with the hardware parity check on the whole SRAM.

- 4 Kbytes of SRAM on instruction and data bus (core coupled memory or CCM) and used to execute critical routines or to access data.
- 12 Kbytes of SRAM mapped on the data bus.

The STM32L4 Series and STM32L4+ Series devices feature an additional SRAM (SRAM2) of 64 Kbytes on STM32L4+ Series and STM32L49xxx/4Axxx, 32 Kbytes on STM32L47xxx/48xxx and STM32L45xxx/46xxx and 16 Kbytes on STM32L43xxx/44xxx and an additional SRAM (SRAM3) of 384 Kbytes available only in STM32L4+ Series.

The SRAM2 includes below additional features:

- Read protection (RDP)
- Erase by system reset (option byte) or by software
- Content is preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, Stop 2 mode
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

Bit-banding on Cortex-M4

STM32F303 line and STM32L4 Series / STM32L4+ Series support bit-banding on the lowest 1 Mbyte of SRAM and on the peripheral memory region.

However the peripherals mapped in this bit-banding region are not the same on each series of products.

The peripherals accessible with bit-banding are:

- For STM32F303 line: all the peripherals except FMC, ADC, GPIOx registers.
- For STM32L4 Series and STM32L4+ Series: all the peripherals except FSMC, RNG, AES, USB OTG FS, GPIOx, ADC registers.

4.3 Direct memory access controller (DMA)

The STM32F303 line devices implement a “general purpose” DMA similar to the STM32L4 Series and STM32L4+ Series devices. *Table 11* shows the main differences.

For STM32L4+ Series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer. In the rest of STM32L4 Series and STM32L4+ Series devices, the DMA request line is connected directly to the peripherals.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routine function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

Table 11. DMA differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

DMA	STM32F303 line	STM32L4 Series STM32L4+ Series
Architecture	– 2 DMA controllers can access memory and peripherals (F3xB/C/D/E) – 1 DMA controller can access memory and peripherals (F3x6/8)	– 2 DMA controllers can access memory and peripherals
Channels	– 12 channels (F3xB/C/D/E) – 7 channels (F3x6/8) – 8 requests per channel	– 7 channels – 8 requests per channel

Table 12 presents the correspondence between the DMA requests in STM32F303 line and in STM32L4 Series / STM32L4+ Series.

Table 12. DMA request differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

Peripheral	DMA request	STM32F303xB/C/D/E	STM32F303x6/8	STM32L4 Series STM32L4+ Series
ADC	ADC1	DMA1_Channel1	DMA1_Channel1	DMA1_Channel1 DMA2_Channel3
	ADC2	DMA2_Channel1 DMA2_Channel3	DMA1_Channel2 DMA1_Channel4	DMA1_Channel2(1) DMA2_Channel4(1)
	ADC3	DMA2_Channel5	NA	DMA1_Channel3(1) DMA2_Channel5(1)
	ADC4	DMA2_Channel2 DMA2_Channel4		NA
DAC	DAC1_CH1	DMA1_Channel3 DMA2_Channel3	DMA1_Channel3 DMA1_Channel5	DMA1_Channel3 DMA2_Channel4
	DAC1_CH2	DMA1_Channel4 DMA2_Channel4	DMA1_Channel4	DMA1_Channel4 DMA2_Channel5
DFSDM	DFSDM0	NA		DMA1_Channel4(1)
	DFSDM1			DMA1_Channel5(1)
	DFSDM2			DMA1_Channel6(1)
	DFSDM3			DMA1_Channel7(1)
DCMI	DCMI			DMA2_Channel7(2) DMA2_Channel5(2)
CRYPT	CRYPT_OUT			NA
	CRYPT_IN			
HASH	HASH_IN			DMA2_Channel7(3)
AES	AES_IN			DMA2_Channel1 DMA2_Channel5
	AES_OUT			DMA2_Channel2 DMA2_Channel3
SDIO	SDIO			NA
SDMMC	SDMMC1			DMA2_Channel4 DMA2_Channel5
LPUART	LPUART_RX			DMA2_Channel7
	LPUART_TX			DMA2_Channel6
UART	UART4_RX	DMA2_Channel3	NA	DMA2_Channel5(1)
	UART4_TX	DMA2_Channel5		DMA2_Channel3(1)
	UART5_RX	NA		DMA2_Channel2(1)
	UART5_TX			DMA2_Channel1(1)

Table 12. DMA request differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F303xB/C/D/E	STM32F303x6/8	STM32L4 Series STM32L4+ Series
USART	USART1_RX	DMA1_Channel5	DMA1_Channel5	DMA1_Channel5 DMA2_Channel7
	USART1_TX	DMA1_Channel4	DMA1_Channel4	DMA1_Channel4 DMA2_Channel6
	USART2_RX	DMA1_Channel6	DMA1_Channel6	DMA1_Channel6
	USART2_TX	DMA1_Channel7	DMA1_Channel7	DMA1_Channel7
	USART3_RX	DMA1_Channel3	DMA1_Channel3	DMA1_Channel3
	USART3_TX	DMA1_Channel2	DMA1_Channel2	DMA1_Channel2
	USART6_RX	NA		
	USART6_TX			
SPI	SPI1_RX	DMA1_Channel2	DMA1_Channel2 DMA1_Channel4 DMA1_Channel6	DMA1_Channel2 DMA2_Channel3
	SPI1_TX	DMA1_Channel3	DMA1_Channel3 DMA1_Channel5 DMA1_Channel7	DMA1_Channel3 DMA2_Channel4
	SPI2_RX	DMA1_Channel4	NA	DMA1_Channel4
	SPI2_TX	DMA1_Channel5		DMA1_Channel5
	SPI3_RX	DMA2_Channel1		DMA2_Channel1
	SPI3_TX	DMA2_Channel2		DMA2_Channel2
	SPI4_RX	DMA2_Channel4(3)		NA
	SPI4_TX	DMA2_Channel5(3)		
	QUADSPI	NA		DMA1_Channel5 DMA2_Channel7
I2C	I2C1_RX	DMA1_Channel7	DMA1_Channel3 DMA1_Channel5 DMA1_Channel7	DMA1_Channel7 DMA2_Channel6
	I2C1_TX	DMA1_Channel6	DMA1_Channel2 DMA1_Channel4 DMA1_Channel6	DMA1_Channel6 DMA2_Channel7
	I2C2_RX	DMA1_Channel5	NA	DMA1_Channel5
	I2C2_TX	DMA1_Channel4		DMA1_Channel4
	I2C3_RX	DMA1_Channel2(3)		DMA1_Channel3
	I2C3_TX	DMA1_Channel1(3)		DMA1_Channel2
	I2C4_RX	NA		DMA2_Channel1
	I2C4_TX			DMA2_Channel2

Table 12. DMA request differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F303xB/C/D/E	STM32F303x6/8	STM32L4 Series STM32L4+ Series
I2S	I2S2_ext_RX	NA		
	I2S2_ext_TX			
	I2S3_ext_RX			
	I2S3_ext_TX			
TIM1	TIM1_CH1	DMA1_Channel2	DMA1_Channel2	DMA1_Channel2
	TIM1_CH2	DMA1_Channel3	DMA1_Channel3	DMA1_Channel3
	TIM1_CH4	DMA1_Channel4	DMA1_Channel4	DMA1_Channel4
	TIM1_TRIG	DMA1_Channel4	DMA1_Channel4	DMA1_Channel4
	TIM1_COM	DMA1_Channel4	DMA1_Channel4	DMA1_Channel4
	TIM1_UP	DMA1_Channel5	DMA1_Channel5	DMA1_Channel6
	TIM1_CH3	DMA1_Channel6	DMA1_Channel6	DMA1_Channel7
TIM2	TIM2_UP	DMA1_Channel2	DMA1_Channel2	DMA1_Channel2
	TIM2_CH3	DMA1_Channel1	DMA1_Channel1	DMA1_Channel1
	TIM2_CH1	DMA1_Channel5	DMA1_Channel5	DMA1_Channel5
	TIM2_CH2	DMA1_Channel7	DMA1_Channel7	DMA1_Channel7
	TIM2_CH4	DMA1_Channel7	DMA1_Channel7	DMA1_Channel7
TIM3	TIM3_CH4	DMA1_Channel3	DMA1_Channel3	DMA1_Channel3(1)
	TIM3_UP	DMA1_Channel3	DMA1_Channel3	DMA1_Channel3(1)
	TIM3_CH1	DMA1_Channel6	DMA1_Channel6	DMA1_Channel6
	TIM3_TRIG	DMA1_Channel6	DMA1_Channel6	DMA1_Channel6
	TIM3_CH3	DMA1_Channel2	DMA1_Channel2	DMA1_Channel2
TIM4	TIM4_CH1	DMA1_Channel1	NA	DMA1_Channel1(1)
	TIM4_CH2	DMA1_Channel4		DMA1_Channel4(2)
	TIM4_UP	DMA1_Channel7		DMA1_Channel7
	TIM4_CH3	DMA1_Channel5		DMA1_Channel5
TIM5	TIM5_CH3	NA		DMA2_Channel2
	TIM5_UP			DMA2_Channel2
	TIM5_CH4			DMA2_Channel1
	TIM5_TRIG			DMA2_Channel1
	TIM5_CH1			DMA2_Channel5
	TIM5_CH2			DMA2_Channel4
	TIM5_COM			DMA2_Channel1
TIM6	TIM6_UP	DMA1_Channel3 DMA2_Channel3	DMA1_Channel3	DMA1_Channel3 DMA2_Channel4
TIM7	TIM7_UP	DMA1_Channel4 DMA2_Channel4	DMA1_Channel4	DMA1_Channel4 DMA2_Channel5

Table 12. DMA request differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F303xB/C/D/E	STM32F303x6/8	STM32L4 Series STM32L4+ Series
TIM8	TIM8_CH1 TIM8_CH2 TIM8_CH3 TIM8_UP TIM8_CH4 TIM8_TRIG TIM8_COM	DMA2_Channel3 DMA2_Channel5 DMA2_Channel1 DMA2_Channel1 DMA2_Channel2 DMA2_Channel2 DMA2_Channel2	NA	DMA2_Channel6 DMA2_Channel7 DMA2_Channel1 DMA2_Channel1 DMA2_Channel2 DMA2_Channel2 DMA2_Channel2
TIM15	TIM15_CH1 TIM15_UP TIM15_TRIG TIM15_COM	DMA1_Channel5 DMA1_Channel5 DMA1_Channel5 DMA1_Channel5	DMA1_Channel5 DMA1_Channel5 DMA1_Channel5 DMA1_Channel5	DMA1_Channel5 DMA1_Channel5 DMA1_Channel5 DMA1_Channel5
TIM16	TIM16_CH1 TIM16_UP TIM16_CH1 TIM16_UP	DMA1_Channel3 DMA1_Channel3 DMA1_Channel6 DMA1_Channel6	DMA1_Channel3 DMA1_Channel3 DMA1_Channel6 DMA1_Channel6	DMA1_Channel3 DMA1_Channel3 DMA1_Channel6 DMA1_Channel6
TIM17	TIM17_CH1 TIM17_UP TIM17_CH1 TIM17_UP	DMA1_Channel1 DMA1_Channel1 DMA1_Channel7 DMA1_Channel7	DMA1_Channel1 DMA1_Channel1 DMA1_Channel7 DMA1_Channel7	DMA1_Channel1(1) DMA1_Channel1(1) DMA1_Channel7 DMA1_Channel7
TIM20	TIM20_CH1 TIM20_CH2 TIM20_CH3 TIM20_UP TIM20_CH4 TIM20_TRIG TIM20_COM	DMA2_Channel1(3) DMA2_Channel2(3) DMA2_Channel3(3) DMA2_Channel3(3) DMA2_Channel4(3) DMA2_Channel4(3) DMA2_Channel4(3)	NA	
SAI	SAI1_A	NA		DMA2_Channel1 DMA2_Channel6
	SAI1_B			DMA2_Channel2 DMA2_Channel7
	SAI2_A			DMA1_Channel6(1) DMA2_Channel3(1)
	SAI2_B			DMA1_Channel7(1) DMA2_Channel4(1)
SWPMI	SWPMI_RX			DMA2_Channel1
	SWPMI_TX			DMA2_Channel2

Color key:
= Feature not available (NA)
= Differences

1. Not applicable for STM32L43xxx/44xxx.
2. Only for STM32L4A6xx/4A6xx.
3. Only for STM32L4A6xx.

4.4 Interrupts

Table 13 presents the interrupt vectors in STM32F303 line compared to STM32L4 Series and STM32L4+ Series.

Table 13. Interrupt vector differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

Position	STM32F303 line	STM32L4 Series STM32L4+ Series
0	WWDG	WWDG
1	PVD	PVD / PVM
2	TAMP_ STAMP	TAMPER / CSS
3	RTC_WKUP	RTC_WKUP
4	FLASH	FLASH
5	RCC	RCC
6	EXTI0	EXTI0
7	EXTI1	EXTI1
8	EXTI2_TS	EXTI2
9	EXTI3	EXTI3
10	EXTI4	EXTI4
11	DMA1_Channel1	DMA1_Channel1
12	DMA1_Channel2	DMA1_Channel2
13	DMA1_Channel3	DMA1_Channel3
14	DMA1_Channel4	DMA1_Channel4
15	DMA1_Channel5	DMA1_Channel5
16	DMA1_Channel6	DMA1_Channel6
17	DMA1_Channel7	DMA1_Channel7
18	ADC1_2	ADC1_2
19	CAN1_TX	CAN1_TX
20	CAN1_RX0	CAN1_RX0
21	CAN1_RX1	CAN1_RX1
22	CAN1_SCE	CAN1_SCE
23	EXTI9_5	EXTI9_5
24	TIM1_BRK / TIM15	TIM1_BRK / TIM15
25	TIM1_UP / TIM16	TIM1_UP / TIM16
26	TIM1_TRG_COM / TIM17	TIM1_TRG_COM / TIM17
27	TIM1_CC	TIM1_CC
28	TIM2	TIM2

Table 13. Interrupt vector differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

Position	STM32F303 line	STM32L4 Series STM32L4+ Series
29	TIM3	TIM3(1)
30	TIM4	TIM4(1)
31	I2C1_EV	I2C1_EV
32	I2C1_ER	I2C1_ER
33	I2C2_EV	I2C2_EV
34	I2C2_ER	I2C2_ER
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	USART3	USART3
40	EXTI15_10	EXTI15_10
41	RTC_Alarm	RTC_Alarm
42	USBWakeUp	DFSDM3(1)
43	TIM8_BRK	TIM8_BRK(1)
44	TIM8_UP	TIM8_UP(1)
45	TIM8_TRG_COM	TIM8_TRG_COM(1)
46	TIM8_CC	TIM8_CC(1)
47	ADC3	ADC3(1)
48	FMC	FMC(1)
49	NA	SDMMC
50		TIM5(1)
51	SPI3	SPI3
52	UART4	UART4(1)
53	UART5	UART5(1)
54	TIM6_DACUNDER	TIM6_DACUNDER
55	TIM7	TIM7
56	DMA2_Channel1	DMA2_Channel1
57	DMA2_Channel2	DMA2_Channel2
58	DMA2_Channel3	DMA2_Channel3
59	DMA2_Channel4	DMA2_Channel4
60	DMA2_Channel5	DMA2_Channel5
61	ADC4	DFSDM0(2)

Table 13. Interrupt vector differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

Position	STM32F303 line	STM32L4 Series STM32L4+ Series
62	NA	DFSDM1(2)
63		DFSDM2(1)
64	COMP1_2_3	COMP
65	COMP4_5_6	LPTIM1
66	COMP7	LPTIM2
67	NA	– OTG_FS (STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – USB_FS (STM32L45xxx/46xxx and STM32L43xxx/44xxx)
68		DMA2_CH6
69		DMA2_CH7
70		LPUART1
71		– QUADSPI – OCTOSPI1 (STM32L4+ Series)
72	I2C3_EV (only on D/E)	I2C3_EV
73	I2C3_ER (only on D/E)	I2C3_ER
74	USB_HP	SAI1
75	USB_LP	SAI2(1)
76	USB_WakeUp_RMP	– SWPMI1 – OCTOSPI2 (STM32L4+ Series)
77	TIM20_BRK (only on D/E)	TSC
78	TIM20_UP (only on D/E)	– LCD – DSIHOST (STM32L4R9xx/4S9xx)
79	TIM20_TRG_COM (only on D/E)	AES
80	TIM20_CC (only on D/E)	RNG
81	FPU	FPU
82	NA	HASH and CRS
83		I2C4_EV
84	SPI4 (only on D/E)	I2C4_ER

Table 13. Interrupt vector differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

Position	STM32F303 line	STM32L4 Series STM32L4+ Series
85	NA	DCMI
86		CAN2_TX
87		CAN2_RX0
88		CAN2_RX1
89		CAN2_SCE
90		DMA2D
91		LCD-TFT
92		LCD-TFT_ER
93		GFXMMU
94		DMAMUX1_OVR

Color key:

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

1. Reserved for STM32L45xxx/46xxx and STM32L43xxx/44xxx devices.
2. Reserved for STM32L43xxx/44xxx devices.

4.5 Reset and clock control (RCC)

The main differences related to the RCC between STM32L4 Series / STM32L4+ Series and STM32F303 line are presented in *Table 14*.

Table 14. RCC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

RCC	STM32F303 line	STM32L4 Series STM32L4+ Series
MSI	NA	– MSI is a low power oscillator with programmable frequency up to 48 MHz – It can replace PPLs as system clock (faster wakeup, lower consumption) – It can be used as USB device clock (no need for external high speed crystal oscillator) – Multi Speed RC factory and user trimmed 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz – Auto calibration from LSE
HSI16	8 MHz RC factory and user trimmed	16 MHz RC factory and user trimmed
LSI	Around 40 kHz (between 30 kHz and 50 kHz)	– 32 kHz RC – Lower consumption, higher accuracy (refer to product datasheet)
HSE	4 to 32 MHz	4 to 48 MHz
LSE	– 32.768 kHz – Configurable drive/consumption – Available in backup domain (VBAT)	
HSI48	NA	– 48 MHz RC (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx) – Can drive USB Full Speed, SDMMC and RNG

Table 14. RCC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

RCC	STM32F303 line	STM32L4 Series STM32L4+ Series
PLL	– Internal PLL can be used to multiply HSI or HSE output clock frequency – The PLL sources are HSI, HSE	– Main PLL for system – 2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – 1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L45xxx/46xxx and STM32L43xxx/44xxx) – Each PLL can provide up to 3 independent outputs – The PLL multiplication/division factors are different from STM32F303 line – PLL clock sources: MSI, HSI16, HSE
System clock source	HSI, HSE or PLL	MSI, HSI16, HSE or PLL
System clock frequency	– Up to 72 MHz – 8 MHz after reset using HSI	– Up to 80 MHz (or 120 for STM32L4+ Series) – 4 MHz after reset using MSI
AHB frequency	Up to 72 MHz	Up to 80 MHz (or 120 for STM32L4+ Series)
APB1 frequency	Up to 36 MHz	Up to 80 MHz (or 120 for STM32L4+ Series)
APB2 frequency	Up to 72 MHz	Up to 80 MHz (or 120 for STM32L4+ Series)
RTC clock source	LSI, LSE or HSE/32	LSI, LSE or HSE/32
MCO clock source	– MCO pin (PA8): LSI, LSE, SYSCLK, HSI, HSE, PLLCLK/2 – With configurable prescaler 1, 2, 3, 4, 8, 16, 32, 64, 128	– MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI or HSI48 (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx) – With configurable prescaler 1, 2, 4, 8 or 16 for each output
CSS	– CSS (clock security system) – CSS on HSE	– CSS on HSE (clock security system) – CSS on LSE

Table 14. RCC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

RCC	STM32F303 line	STM32L4 Series STM32L4+ Series
Internal oscillator measurement / calibration	– LSE connected to TIM16 CH1 IC: can measure HSI with respect to LSE clock high precision – HSE/32 connected to TIM16 CH1 IC: can measure HSE with respect to LSE/HSI clock	– LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision – LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision – HSE/32 connected to TIM17 CH1 IC: can measure HSE with respect to LSE/HSI16 clock – MSI connected to TIM17 CH1 IC: can measure MSI with respect to HSI16/HSE clock – On STM32L45xxx/46xxx and STM32L43xxx/44xxx HSE/32 and MSI connect to TIM16 CH1 IC
Interrupt	– CSS (linked to NMI IRQ) – PLLRDY, HSERDY, HSIRDY, LSERDY, LSIRDY (linked to RCC global IRQ)	– CSS (linked to NMI IRQ) – LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY (only on STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) (linked to RCC global IRQ)
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Feature not available (NA) = Differences.		

In addition to the differences described in *Table 14*, the additional adaptation steps described in sections *4.5.1*, *4.5.2* and *4.5.3* may be needed for the migration

4.5.1 Performance versus V_{CORE} ranges

In STM32L4 Series and STM32L4+ Series, the maximum CPU clock frequency and the number of Flash memory wait states depend on the selected voltage range V_{CORE}.

Table 15. STM32L4 Series and STM32L4+ Seriesperformance versus V_{CORE} ranges(1)

CPU performance	Power performance	V_{CORE} Range	Typical Value (V)	Max frequency (MHz)					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
STM32L4 Series									
High	Medium	1	1.2	-	80	64	48	32	16
Medium	High	2	1.0	-	26	26	18	12	6
STM32L4+ Series									
High	Medium	1 boost mode	1.28	120	100	80	60	40	20
		1 normal mode	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8

1. WS = wait state.

On STM32F303 line, the maximum CPU clock frequency and the number of Flash memory wait states are linked by the below conditions:

- Zero wait state, if 0 < HCLK ≤ 24 MHz
- One wait state, if 24 MHz < HCLK ≤ 48 MHz
- Two wait states, if 48 MHz < HCLK ≤ 72 MHz.

4.5.2 Peripheral access configuration

*S*ince the address mapping of some peripherals has been changed in STM32L4 Series and STM32L4+ Series compared to STM32F303 line, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from reset mode] (see *Table 16*).

Table 16. RCC registers used for peripheral access configuration

Bus	Register STM32F303 line	Register STM32L4 Series STM32L4+ Series	Comments
AHB	RCC_AHBRSTR	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHBENR	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2)	Used to [enable/disable] the AHB peripheral clock
	NA	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)	Used to [enable/disable] the AHB peripheral clock in Sleep mode

Table 16. RCC registers used for peripheral access configuration (continued)

Bus	Register STM32F303 line	Register STM32L4 Series STM32L4+ Series	Comments
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2	Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2	Used to [enable/disable] the APB1 peripheral clock
	NA	RCC_APB1SMENR1 RCC_APB1SMENR2	Used to [enable/disable] the APB1 peripheral clock in Sleep mode
APB2	RCC_APB2RSTR		Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	NA	RCC_APB2SMENR	Used to [enable/disable] the APB2 peripheral clock in Sleep mode
Color key: = Feature not available (NA)			

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source independent from the system clock that is used to generate the clock required for their operation.

- **USB:**
  - In STM32F303 line: the USB 48 MHz clock is derived from the PLL VCO (STM32F303xB/C/D/E devices).
  - In STM32L4 Series and STM32L4+ Series: the USB 48 MHz clock is derived from one of the following sources:
    Main PLL VCO (PLLUSB1CLK)
    PLLSAI1 VCO (PLLUSB2CLK)
    MSI clock (when the MSI clock is auto-trimmed with the LSE, it can be used by the USB OTG FS device)
    HSI48 internal oscillator (only on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx).
- **SDIO/SDMMC:**

  In STM32L4 Series and STM32L4+ Series the SDMMC clock is derived from one of the following sources:
  Main PLL VCO (PLLUSB1CLK)
  PLLSAI1 VCO (PLLUSB2CLK) MSI clock
  HSI48 internal oscillator (only on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx).

- **RTC:**
  - In STM32F303 line: the RTC clock which is derived from LSE, LSI or from HSE clock divided by 32.
  - In STM32L4 Series and STM32L4+ Series: the RTC (and LCD Glass clock) is derived from one of the three following sources:
    LSE clock
    LSI clock
    HSE clock divided by 32 (PCLK frequency must always be greater than or equal to RTC clock frequency).
- **ADC:**
  - In STM32F303 line: the ADCs asynchronous clock is derived from the PLL output. It can reach 72 MHz and can then be divided by 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128 or 256.
  - In STM32L4 Series and STM32L4+ Series: the asynchronous ADCs clock can be derived from one of the three following sources:
    System clock (SYSCLK)
    PLLSAI1 VCO (PLLADC1CLK)
    PLLSAI2 VCO (PLLADC2CLK)[(a)]. In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).
- **DAC:**
  In STM32L4 Series and STM32L4+ Series: in addition to the PCLK1 clock, LSI clock is used for the sampling and hold operation.
- **I2Cs:**
  - In STM32F303 line: the I2C1/2 (I2C1/2/3 in STM32F303xD/E) clock which is derived (selected by software) from one of the two following sources: system clock or HSI clock.
  - In STM32L4 Series and STM32L4+ Series: the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16 or APB1 (PCLK1).
- **I2S:**
  I2S external clock is available on STM32F303 line and not available in STM32L4 Series nor STM32L4+ Series.

a. PLLSAI2VCO (PLLADC2CLK) is a clock source only on STM32L49xxx/4Axxx and STM32L47xxx/48xxx.

4.6 Power control (PWR)

In STM32L4 Series and STM32L4+ Series, the PWR controller presents some differences when compared to STM32F303 line. These differences are summarized in *Table 17*.

Table 17. PWR differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

PWR	STM32F303 line	STM32L4 Series STM32L4+ Series
Power supplies	– V_{DD} = 2.0 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator – It is provided externally through VDD pins	– V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator – It is provided externally through VDD pins
	– V_{DD18} = 1.65 to 1.95 V – V_{DD18} is the power supply for digital core, SRAM and Flash memory – V_{DD18} is internally generated through an internal voltage regulator	– V_{CORE} = 1.0 to 1.28 V – V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory – It is generated by an internal voltage regulator – Two V_{CORE} ranges can be selected by software depending on target frequency
	V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when VDD is not present	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present
	V_{DD} must always be kept lower than or equal to V_{DDA}	Independent power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}) allow to improve power consumption by running MCU at lower supply voltage than analog and USB
	– V_{SSA}, V_{DDA} STM32F303x6/8/B/C/D/E = 2.0 to 3.6 V – External power supply for ADC, DAC, comparators, operational amplifiers, temperature sensor, PLL, HSI 8 MHz oscillator, LSI 40 kHz oscillator, and reset block – V_{DDA} must be in the 2.4 to 3.6 V range when the OPAMP and DAC are used. – It is forbidden to have $V_{DDA} < V_{DD}$ - 0.4 V – An external Schottky diode must be placed between VDD and VDDA to guarantee that this condition is met	– V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DAC/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V. – V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators – The V_{DDA} voltage level is independent from the V_{DD} voltage
	NA	– V_{LCD} = 2.5 to 3.6 V – The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter

Table 17. PWR differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F303 line	STM32L4 Series STM32L4+ Series
Power supplies (continuation)	– NA – USB FS powered by V_{DD} – V_{DD} must be > 3.0 V (or degraded electrical characteristic between 2.7 V to 3 V)	– V_{DDUSB} = 3.0 to 3.6 V – V_{DDUSB} is the external independent power supply for USB transceivers – The V_{DDUSB} voltage level is independent from the V_{DD} voltage
	NA	– V_{DDIO2} = 1.08 V to 3.6 V – V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]) – The V_{DDIO2} voltage level is independent from the V_{DD} voltage (not applicable for STM32L45xxx/46xxx and STM32L43xxx/44xxx)
		– Available only on SM32L4R9xx/4S9xx – VDDDSI is independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY – This supply must be connected to the global VDD
		– Available only on SM32L4R9xx/4S9xx – VCAPDSI is the output of the DSI regulator (1.2 V) which must be connected externally to VDD12DSI
		– Available only on SM32L4R9xx/4S9xx – VDD12DSI is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins – An external capacitor of 2.2µF must be connected on the VDD12DSI pin
Battery backup domain	– RTC with backup registers (64 bytes on B/C, 20 bytes on 6/8) – LSE – PC13 to PC15 I/Os	– RTC with backup registers (128 bytes) – LSE – PC13 to PC15 I/Os
Power supply supervisor	– Integrated POR / PDR circuitry – Programmable voltage detector (PVD)	– Integrated POR / PDR circuitry – Programmable voltage detector (PVD)
	NA	– Brownout reset (BOR) – BOR is always enabled, except in Shutdown mode
		4 peripheral voltage monitoring (PVM) – PVM1 for V_{DDUSB} – PVM2 for V_{DDIO2} – PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V)

Table 17. PWR differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F303 line	STM32L4 Series STM32L4+ Series
Low-power modes	Sleep mode	Sleep mode
	NA	Low Power Run mode – System clock is limited to 2 MHz – I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz – Consumption is reduced at lower frequency thanks to LP regulator usage
		Low power Sleep mode – System clock is limited to 2 MHz – I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz – Consumption is reduced at lower frequency thanks to LP regulator usage
	Stop mode (all clocks are stopped)	Stop 0, Stop1 and Stop2 mode Some additional functional peripherals (see wakeup source)
	Standby mode (V_{DD18} domain powered off)	Standby mode (V_{CORE} domain powered off) – Optional SRAM2 retention – Optional I/O pull-up or pull-down configuration
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off)
Wake-up sources	Sleep mode Any peripheral interrupt/wakeup event	Sleep mode Any peripheral interrupt/wakeup event
	Stop mode – Any EXTI line event/interrupt – PVD, USB wakeup, RTC, COMPx, I2Cx, U(S)ARTx	Stop 0, Stop 1 and Stop 2 mode – Any EXTI line event/interrupt – BOR, PVD, PVM, COMP, RTC, USB, IWDG, – U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
	Standby mode – NRST external reset – IWDG reset – 3 WKUP pins – RTC event	Standby mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin – IWDG reset
	NA	Shutdown mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin

Table 17. PWR differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F303 line	STM32L4 Series STM32L4+ Series
Wake-up clocks	Wake-up from Stop HSI RC clock	Wake-up from Stop HSI16 16 MHz or MSI (all ranges up to 48 MHz) allowing 5 µs wakeup at high speed without waiting for PLL startup time
	Wake-up from Standby HSI RC clock	Wake-up from Standby MSI (ranges from 1 to 8 MHz)
	NA	Wake-up from Shutdown MSI 4 MHz
Configuration	Two registers in STM32F303 line	– In STM32L4 Series / STM32L4+ Series the registers are different – 23 registers in STM32L4 Series / STM32L4+ Series 4 control registers 2 status registers 1 status clear register 2 registers per GPIO port (A,B,..H) for controlling pull-up and pull-down (16 registers) – Most configuration bits from STM32F303 line can be found in STM32L4 Series / STM32L4+ Series (but sometime may have different programming mode)

Color key:

= New feature or new architecture

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

4.7 Real-time clock (RTC)

STM32L4 Series / STM32L4+ Series and STM32F303 line implement almost the same features on the RTC. *Table 18* shows the differences.

Table 18. RTC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

RTC	STM32F303 line	STM32L4 Series STM32L4+ Series
Features	Smooth calibration available	Smooth calibration available
	3 tamper pin (available in VBAT)	3 tamper pin (available in VBAT)
	– On STM32F303xB/C/D/E: 64 bytes backup registers – On STM32F303x6/8: 20 bytes backup registers	128 bytes backup registers
Color key: = Same feature, but specification change or enhancement		

For more information, refer to the RTC section of STM32L4 Series and STM32L4+ Series reference manuals.

4.8 System configuration controller (SYSCFG)

The STM32L4 Series and STM32L4+ Series SYSCFG implements additional features compared to the STM32F303 line one. *Table 19* shows the differences.

Table 19. SYSCFG differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

SYSCFG	STM32F303 line	STM32L4 Series STM32L4+ Series
Features	– Remapping memory areas – Managing the external interrupt line connection to the GPIOs – Setting SRAM write protection and software erase – Enabling /disabling I2C Fast-mode Plus driving capability on some I/Os – ADC triggers remapping – DAC triggers remapping – See details in RM0316	– Remapping memory areas – Managing the external interrupt line connection to the GPIOs – Managing robustness feature – Setting SRAM2 write protection and software erase – Configuring FPU interrupts – Enabling the firewall – Enabling /disabling I2C Fast-mode Plus driving capability on some I/Os and voltage booster for I/Os analog switches

Table 19. SYSCFG differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

SYSCFG	STM32F303 line	STM32L4 Series STM32L4+ Series
Configuration	-	– Most registers from STM32F303 line are identical in STM32L4 Series – A few bits are different and EXTI configuration may differ (number of GPIO is different depending on product)
Color key: = Same feature, but specification change or enhancement		

4.9 General-purpose I/O interface (GPIO)

The STM32L4 Series GPIO peripheral embeds some identical features compared to the STM32F303 line.

The GPIO code written for the STM32F303 line devices may require minor adaptations for STM32L4 Series devices. This is due to the mapping of particular functions on different GPIOs (refer to *Section 2* for pinout differences, and to product datasheet for the detailed alternate function mapping differences).

Below are the main GPIO features:

- GPIO mapped on AHB bus for better performance.
- I/O pin multiplexer and mapping: the pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, there cannot be any conflict between the peripherals sharing the same I/O pin.

At reset, the STM32F303 line GPIOs are configured in input floating mode while the STM32L4 Series GPIOs are configured in analog mode (to avoid consumption through the IO Schmitt trigger).

For more information about the STM32L4 Series GPIO programming and usage, refer to the “I/O pin multiplexer and mapping” section in the GPIO section of the STM32L4 Series reference manuals and to the product datasheet for detailed description of the pinout and alternate function mapping.

4.10 Extended interrupts and events controller (EXTI) source selection

The external interrupt/event controller (EXTI) is very similar on STM32F303 line and STM32L4 Series / STM32L4+ Series. *Table 20* shows the main differences.

Table 20. EXTI differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

EXTI	STM32F303 line	STM32L4 Series STM32L4+ Series
Number of event/interrupt lines	Up to 36 lines: – 8 direct, 28 configurable	Up to 41 lines – 12 direct, 26 configurable on STM32L4+ Series – 15 direct, 26 configurable on STM32L49xxx/4Axxx – 14 direct, 26 configurable on STM32L47xxx/48xxx – 12 direct, 25 configurable on STM32L45xxx/46xxx and STM32L43xxx/44xxx
Configuration	-	Registers are slightly different to cope with different number of interrupts
Color key: = Same feature, but specification change or enhancement		

4.11 Flash memory

Table 21 presents the differences between the Flash memory interface of STM32F303 line compared to STM32L4 Series / STM32L4+ Series.

The STM32L4 Series and STM32L4+ Series devices instantiate a different Flash module. Consequently the STM32L4 Series and STM32L4+ Series Flash programming procedures and registers are different from the ones of STM32F303 line. Any code written for the Flash interface in STM32F303 line needs to be rewritten to run in STM32L4 Series and STM32L4+ Series.

All the STM32F303xB/C devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

All the STM32F303xD/E devices feature 384/512 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

All the STM32F303x6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

For more information on programming, erasing and protection of the STM32L4 Series and STM32L4+ Series Flash memory, refer to the STM32L4 Series and STM32L4+ Series reference manuals.

Table 21. FLASH differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

FLASH	STM32F303 line	STM32L4 Series STM32L4+ Series
Main/ Program memory	0x0800 0000 to (up to) 0x0807 FFFF	– 0x0800 0000 to up to 0x080F FFFF – 0x0800 0000 to up to 0x081F FFFF (only for STM32L4+ Series)
	– Up to 512 Kbytes – 1 bank – Up to 256 pages of 2 Kbytes – Programming granularity: 64-bit – Read granularity: 128-bit	– For STM32L4+ Series devices: Up to 2 Mbytes Split in 2 banks When dual bank is enabled each bank: 256 pages of 4 Kbytes and each page: 8 rows of 512 bytes When dual bank is disabled: memory block contains 256 pages of 8 Kbytes and each page: 8 rows of 1024 bytes – For STM32L49xxx/4Axxx and STM32L47xxx/48xxx: Up to 1 Mbyte Split in 2 banks where each bank: 256 pages of 2 Kbytes and each page: 8 rows of 256 bytes – For STM32L45xxx/46xxx: 512 Kbytes 1 bank where 256 pages of 2 Kbytes and each page: 8 rows of 256 bytes – For STM32L43xxx/44xxx: Up to 256 Kbytes 1 bank 128 pages of 2 Kbytes Each page: 8 rows of 256 bytes – Programming and read granularity: 72 bits (including 8 ECC bits)
Features	NA	– Read while write (RWW) – Dual bank boot (only for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
		Flash Empty check (for STM32L45xxx/46xxx and STM32L43xxx/44xxx)
Wait state	Up to 2 (depending on the frequency)	Up to 5 (depending on the core voltage and frequency)

Table 21. FLASH differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

FLASH	STM32F303 line	STM32L4 Series STM32L4+ Series
ART Accelerator™	NA	Allowing 0 wait state when executing from the cache
One time programmable (OTP)		1 Kbyte OTP bytes (bank1)
Erase granularity	Page erase and mass erase	Page erase (2 Kbytes), bank erase and mass erase (both banks)
Read protection (RDP)	– Level 0 no protection – RDP = 0xAA	– Level 0 no protection – RDP = 0xAA
	– Level 1 memory protection – RDP ≠ {0xAA, 0xCC}	– Level 1 memory protection – RDP ≠ {0xAA, 0xCC}
	Level 2 RDP = 0xCC(1)	Level 2 RDP = 0xCC(1)
Proprietary code readout Protection (PCROP)	NA	– 1 PCROP area per bank – Granularity: 64-bit – PCROP_RDP option: PCROP area preserved when RDP level decreased – For STM32L4+ Series: Dual bank: 1 PCROP area per bank Single bank: 2 PCROP areas
Write protection (WRP)	Granularity: 2 pages	– 2 write protection area per bank – Granularity: 2 Kbytes – For STM32L4+ Series: Dual bank: 2 areas per bank Single bank: 4 areas

Table 21. FLASH differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

FLASH	STM32F303 line	STM32L4 Series STM32L4+ Series
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	SRAM_PE	NA
	VDDA_MONITOR	
	RDP	
	USER	
	NA	nRST_SHDW
	WDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
		BOR_LEV[2:0]
		BFB2 (except for STM32L45xxx/46xxx and STM32L43xxx/44xxx)
	nBOOT1	nBOOT1
User option bytes	NA	SRAM2_RST, SRAM2_PE
		DUAL BANK (except for STM32L4+ Series, STM32L45xxx/46xxx and STM32L43xxx/44xxx)
		nBOOT0 (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx)
		nSWBOOT0 (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx)
		DBANK (for STM32L4+ Series)
		DB1M (for STM32L4+ Series)

Color key:

= New feature or new architecture

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

1. Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1.

4.12 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32L4 Series and STM32L4+ Series devices implement several new features on the U(S)ART when compared to STM32F303 line devices. *Table 22*, *Table 23* and *Table 24* show the differences.

Table 22. U(S)ART differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

U(S)ART	STM32F303 line	STM32L4 Series STM32L4+ Series
Instances	– 3 x USART – 2 x UART	– 3 x USART – 2 x UART (STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – 1 x UART (For STM32L45xxx/46xxx) – 1 x LPUART
Baud rate	Up to 9 Mbit/s	Up to 10 Mbit/s (when the clock frequency is 80 MHz and oversampling is by 8)
Color key: = Differences		

Table 23. STM32F303 USART features

USART modes/features (1)	STM32F303xB/C			STM32F303xD/E			STM32F303x6/8	
	USART1/ USART2/ USART3	UART4	UART5	USART1/ USART2/ USART3	UART4	UART5	USART1	USART2/ USART3
Hardware flow control for modem	X	-	-	X	-	-	X	X
Continuous communication using DMA	X	X	-	X	X	-	X	X
Multiprocessor communication	X	X	X	X	X	X	X	X
Synchronous mode	X	-	-	X	-	-	X	X
Smartcard mode	X(2)(3)	-	-	X(4)	-	-	X(4)	-
Single-wire half-duplex communication	X	X	X	X	X	X	X	X
irDA SIR ENDEC block	X	X	X	X	X	X	X	-
LIN mode	X	X	X	X	X	X	X	-
Dual clock domain and wakeup from Stop mode	X	X	X	X	X	X	X	-
Receiver timeout interrupt	X	X	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	X	X	-
Auto baud rate detection	X(5)	-	-	X(5)	-	-	X(5)	-
Driver Enable	X	-	-	X	-	-	X	X
USART data length	8 and 9 bits			7, 8 and 9 bits			7, 8 and 9 bits	

1. X= supported.
2. SCLK output is disabled when UE bit = 0.
3. With the following limitation for STM32F303xB/C: if the USART is used in smartcard mode and the card cannot use the default communication parameters after Answar To Reset and does not support clock stop, it is not possible to use SCLK to clock the card. This is due to the fact that the USART and its clock output must be disabled while reprogramming some of the parameters.
4. SCLK is always available when CLKEN=1, regardless of the UE bit value.
5. Four modes.

Table 24. STM32L4x6 USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	USART4	USART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
irDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain and wakeup from Stop mode	X	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection(2)	X	X	X	X	X	-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.
2. 4 modes.

For STM32L4+ Series, the USART peripheral has two new features:

- Two internal FIFOs for transmit and receive data.
- SPI slave transmission underrun error flag.

4.13 Serial peripheral interface (SPI) / IC to IC sound (I2S) /serial audio interface (SAI)

STM32L4 Series / STM32L4+ Series and STM32F303 line contain the same SPI devices features except for I2S and SAI. *Table 25* shows the differences.

Table 25. SPI differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

SPI	STM32F303 line	STM32L4 Series STM32L4+ Series
Instances	– x3 (STM32F303xB/C) – x4 (STM32F303xD/E) – x1 (STM32F303x6/8)	x3
Features	– STM32F303xB/C = 3 x SPI + 2 x I2S – STM32F303xD/E = 4 x SPI + 2 x I2S – STM32F303x6/8 = 1 x SPI + 0 x I2S	– I2S feature is not supported by SPI in STM32L4 Series / STM32L4+ Series – SAI interfaces are available instead 2 for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx 1 for STM32L45xxx/46xxx and STM32L43xxx/44xxx
Data size	Programmable from 4 to 16-bit	Programmable from 4 to 16-bit
Data buffer	32-bit Tx & Rx FIFOs (up to 4 data frames)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds)	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds)
Mode	– SPI TI mode – SPI Motorola mode – NSSP mode	– SPI TI – SPI Motorola mode – NSSP mode
Speed	Up to 18 Mbit/s	Up to 40 Mbits/s (APB at 80 Hz)
Configuration	-	Refer to STM32L4 Series and STM32L4+ Series reference manuals for details
Color key: = Differences		

Migrating from I2S to SAI:

The STM32L4 Series and STM32L4+ Series does not include the I2S interface part of the SPI peripheral. Instead, it includes serial audio interfaces.

Table 26 shows the main differences between I2S and SAI. Only the full duplex I2S instances are considered.

Table 26. Migrating from I2S to SAI

I2S/SAI	STM32F303 line (I2S)	STM32L4 Series STM32L4+ Series (SAI)
Instances Full duplex I2S	x 2/0	– x2 (SAI1, SAI2) for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx – x1 (SAI1) for STM32L45xxx/46xxx and STM32L43xxx/44xxx
Features	Full-duplex communication	Two independent audio sub-blocks (per SAI) which can be transmitters or receivers with their respective FIFO
	Master or slave operations	– Synchronous or asynchronous mode between the audio sub-blocks – Possible synchronization between multiple SAIs – Master or slave configuration independent for both audio sub-blocks
	8-bit programmable linear prescaler to reach accurate audio sample frequencies (from8 kHz to 192 kHz)	Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode
	– Data format may be 16-bit, 24-bit or 32-bit – Data direction is always MSB first	– Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit. – First active bit position in the slot is configurable – LSB first or MSB first for data transfer
	Channel length is fixed to 16-bit (16-bit data size) or 32-bit (16-bit, 24-bit, 32-bit data size) by audio channel	– Up to 16 slots available with configurable size – Number of bits by frame can be configurable – Frame synchronization active level configurable (offset, bit length, level) – Stereo/Mono audio frame capability
	Programmable clock polarity (steady state).	Communication clock strobing edge configurable (SCK)
	16-bit register for transmission and reception with one data register for both channel sides	8-word integrated FIFOs for each audio sub-block (facilitating interrupt mode)

Table 26. Migrating from I2S to SAI (continued)

I2S/SAI	STM32F303 line (I2S)	STM32L4 Series STM32L4+ Series (SAI)
Features (continued)	Supported I2S protocols: – I2S Philips standard – MSB-justified standard (left-justified) – LSB-justified standard (right-justified) – PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)	Audio protocols: – I2S, LSB or MSB-justified, PCM/DSP, TDM (up to 16 channels), AC'97 – SPDIF output
	DMA capability for transmission and reception (16-bit wide)	2-channel DMA per SAI
	Master clock may be output to drive an external audio component. Ratio is fixed at 256 × F_S (where F_S is the audio sampling frequency)	
	Interruption sources when enabled: – Errors – Tx Buffer Empty, Rx Buffer not Empty	Interruption sources when enabled: – Errors – FIFO requests
	Error flags with associated interrupts if enabled respectively: – Overrun and underrun detection – Anticipated frame synchronization signal detection in slave mode – Late frame synchronization signal detection in slave mode	Same features than STM32F303 line + protection against misalignment in case of underrun and overrun
Configuration	-	– There is no compatibility between STM32F303 line I2S and STM32L4 Series / STM32L4+ Series SAI – User must configure the SAI interface for the target protocol – Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Differences		

The SAI peripheral improves the robustness of the communication in Slave mode compared to the I2S peripheral (in case of data clock glitch for example).

In master mode, while migrating an application from STM32F303 line to STM32L4 Series and STM32L4+ Series, the user must review the possible master clock (MCLK), data bit clock (SCK) and frame synchronization (FS) frequency. Indeed, the STM32L4 Series and STM32L4+ Series PLL multiplication factors and the SAI internal clock divider can be different from the STM32F303 line I2S depending on the external oscillator.

In STM32L4 Series and STM32L4+ Series, SAI1 and SAI2 input clocks are derived (selected by software) from one of the following sources:

- For STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices:
  - An external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2.
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - PLLSAI2 (P) divider output (PLLSAI2CLK)
  - Main PLL (P) divider output (PLLSAI3CLK)
  - HSI (for STM32L4+ Series only)
- For STM32L45xxx/46xxx and STM32L43xxx/44xxx devices:
  - An external clock mapped on SAI1_EXTCLK for SAI1
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - Main PLL (P) divider output (PLLSAI2CLK)
  - HSI16 clock

When the clock is derived from one of the internal PLLs, the three PLL inputs are either HSI16, HSE or MSI (between 4 and 48 MHz) divided by a programmable factor PLLM (from 1 to 8 (or from1 to 16 for STM32L4+ Series)).

This input is then multiplied by PLLN (from 8 to 86 (or from 8 to 127 for STM32L4+ Series)) to reach PLL VCO frequency (which must be between 64 and 344 MHz).

The input is finally divided by PLLP (7 or 17 on STM32L47xxx/48xxx, [2...31] on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx) to provide the input clock of the SAI (max 80 MHz (or 120 MHz for STM32L4+ Series)).

For STM32L4+ Series, when the clock is derived from one of the internal PLLs, the three PLL inputs are either HSI16, HSE or MSI divided by its own programmable factor (PLLM, PLLSAI1M and PLLSAI2M) (from 1 to 16).

When the master clock MCLK is used by the external slave audio peripheral, the PLL output is divided by the SAI internal master clock divider factor (1, 2, 4, 6, 8, ..., 30) to provide the master clock (MCLK). The data bit clock is then derived from MCLK with the following formula:

$$SCK = MCLK \times (FRL + 1) / 256 = (MCLK) / (256 / (FRL + 1))$$

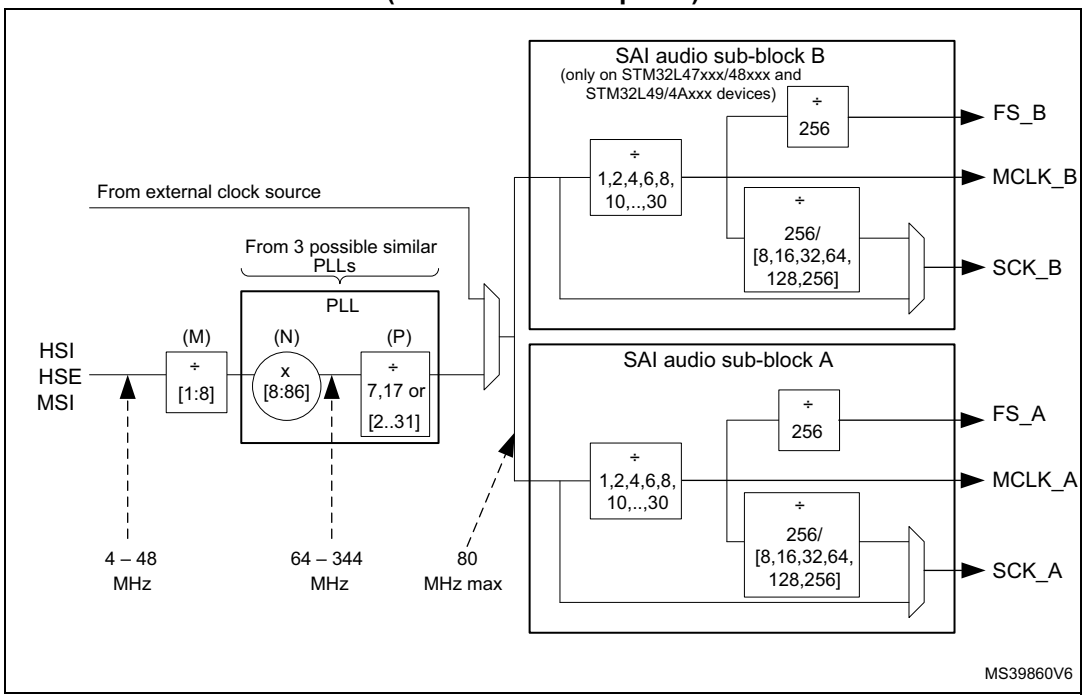
With:

- FRL is the number of bit clock cycles - 1 in the audio frame (0 to 255)
- (FRL + 1) must be a power of 2 higher or equal to 8
- (FRL + 1) = 8, 16, 32, 64, 128, 256

SCK can also be directly connected to the input clock of the SAI when the MCLK output is not needed. The frame synchronization (FS) frequency is always MCLK/256.

Figure 3 shows the clock generation scheme in STM32L4 Series / STM32L4+ Series. Refer to the STM32L4 Series and STM32L4+ Series reference manuals for more details.

Figure 3. STM32L4 Series / STM32L4+ Series generation of clock for SAI master mode (when MCLK is required)



4.14 USB full speed (USB FS)

The STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices implement a USB OTG FS peripheral.The STM32L45xxx/46xxx and STM32L43xxx/44xxx devices implement a USB FS peripheral.

The STM32F303 line devices implement a USB FS peripheral.

Most features supported by STM32F303 line are also supported by STM32L4 Series and STM32L4+ Series. The main differences are listed in *Table 27*.

Table 27. USB differences between STM32F303 line and STM32L4 Series

USB FS	STM32F303 line	STM32L4 Series (STM32L45xxx/46xxx and STM32L43xxx/44xxx)
Features	– Universal serial bus revision 2.0 – STM32F303xD/E embed the USB with LPM support	Universal serial bus revision 2.0 including link power management (LPM) support
	– Configurable number of endpoints from 1 to 8 – Cyclic redundancy check (CRC) generation/checking, Non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing – Isochronous transfers support – Double-buffered bulk/isochronous endpoint support – USB Suspend/Resume operations – Frame locked clock pulse generation	
	NA	– Attach detection protocol (ADP) – Battery charging detection (BCD) – USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)
		Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB.
Mapping	APB1	
Buffer memory	– STM32F303xB/C: 512 bytes of dedicated packet buffer memory SRAM – STM32F303xD/E: 1024 bytes of dedicated packet buffer memory SRAM. When the CAN peripheral clock is enabled in the RCC_APB1ENR register, only the first 768 Bytes are available to USB while the last 256 bytes are used by CAN	1024 bytes of dedicated packet buffer memory SRAM
Low-power modes	– USB suspend and resume – STM32F303xD/E: Link power management (LPM) support	– USB suspend and resume – Link power management (LPM) support
Configuration	-	– In STM32L4 the registers are different – Refer to the STM32L4 reference manuals for details

Color key:

= New feature or new architecture

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

4.15 Analog-to-digital converters (ADC)

Table 28 presents the differences between the STM32F303 line and the STM32L4 Series / STM32L4+ Series ADC peripherals.

New features available: FIFO, oversampling and more dual modes.

Table 28. ADC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

ADC	STM32F303 line	STM32L4 Series STM32L4+ Series
ADC Type	SAR structure	SAR structure
Instances	– 4 instances (B/C/D/E) – 2 instances (6/8)	– 3 instances (STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – 1 instance (STM32L4+ Series, STM32L45xxx/46xxx and STM32L43xxx/44xxx)
Maximum sampling frequency	– 5.1 Msps (Fast channels) – 4.8 Msps (Slow channels	– 5.1 Msps (Fast channels) – 4.8 Msps (Slow channels)
Number of channels	Up to 19 channels per ADC	Up to 19 channels per ADC
Resolution	12-bit	12-bit + digital oversampling up to 16-bit
Conversion modes	– Single / continuous / scan / discontinuous – Dual Mode	– Single / continuous / scan / discontinuous – Dual Mode
DMA	Yes	Yes

Table 28. ADC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

ADC	STM32F303 line		STM32L4 Series STM32L4+ Series	
External trigger	Yes		Yes	
	External event for regular group **STM32F303 ADC1/2** TIM1_CC1 TIM1_CC2 TIM1_CC3 TIM2_CC2 TIM3_TRGO TIM4_CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4 **STM32F303 ADC3/4** TIM3_CC1 TIM2_CC3 TIM1_CC3 TIM8_CC1 TIM8_TRGO EXTI line 2 TIM4_CC1 TIM2_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM3_TRGO TIM4_TRGO TIM7_TRGO TIM15_TRGO TIM2_CC1	External event for injected group **STM32F303 ADC1/2** TIM1_TRGO TIM1_CC4 TIM2_TRGO TIM2_CC1 TIM3_CC4 TIM4_TRGO EXTI line 15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO **STM32F303 ADC3/4** TIM1_TRGO TIM1_CC4 TIM4_CC3 TIM8_CC2 TIM8_CC4 TIM4_CC3 TIM4_CC4 TIM4_TRGO TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM1_CC3 TIM3_TRGO TIM2_TRGO TIM7_TRGO TIM15_TRGO	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM3 TRGO TIM4 CC4(1) EXTI line 11 TIM8_TRGO(1) TIM8_TRGO2(1) TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO(1) TIM6_TRGO TIM15_TRGO TIM3_CC4(1)	External event for injected group: TIM1 TRGO TIM1 CC4 TIM2 TRGO TIM2 CC1 TIM3 CC4(1) TIM4 TRGO(1) EXTI line15 TIM8_CC4(1) TIM1_TRGO2 TIM8_TRGO(1) TIM8_TRGO2(1) TIM3_CC3(1) TIM3_TRGO(1) TIM3_CC1(1) TIM6_TRGO TIM15_TRGO
Supply requirement	2.0 V to 3.6 V		– 1.62 V to 3.6 V – Independent power supply (V_{DDA})	
Reference voltage	– External – The higher/positive reference voltage for the ADC: 2.0 V ≤ VREF+ ≤ VDDA		Reference voltage for STM32L4 Series / STM32L4+ Series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)	

Table 28. ADC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

ADC	STM32F303 line	STM32L4 Series STM32L4+ Series
Electrical parameters	– For STM32F303xB/C/D/E: Consumption linked to conversion mode 194 µA for Single-ended mode at 1 MSPS 212 µA for Differential mode at 1 MSPS – For STM32F303x6/8: Consumption linked to conversion mode 214 µA for Single-ended mode at 1 MSPS 246 µA for Differential mode at 1 MSPS	Consumption proportional to conversion speed: 200 µA/Msps
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	$V_{REF-} \leq V_{IN} \leq V_{REF+}$
Color key: = New feature or new architecture = Same feature, but specification change or enhancement		

1. Except for STM32L43xxx/44xxx devices.

4.16 Digital-to-analog converter (DAC)

The STM32L4 Series and STM32L4+ Series implement an enhanced DAC compared to the one present in the STM32F303 line. *Table 29* shows the differences.

Table 29. DAC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

DAC	STM32F303 line	STM32L4 Series STM32L4+ Series
Number of channels	– For STM32F303xB/C/D/E: 2 x 12-bit DAC channels with output buffer – For STM32F303x6/8: 3 x 12-bit DAC channels Output buffer only on DAC1_CH1	– x2 on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L47xxx/48xxx and STM32L43xxx/44xxx – x1 on STM32L45xxx/46xxx
Resolution	12 bits	

Table 29. DAC differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

DAC	STM32F303 line	STM32L4 Series STM32L4+ Series
Features	– Left or right data alignment in 12-bit mode – Noise-wave and triangular-wave generation (DAC1 only) – DAC with 2 channels for independent or simultaneous conversions	
	NA	– Buffer offset calibration – DAC1_OUTx can be disconnected from output pin – Sample and hold mode for low-power operation in Stop mode
DMA	Yes	Yes
External Trigger	Yes	Yes
	DAC1_CH1 TIM6 TRGO TIM3 TRGO or TIM8 TRGO TIM7 TRGO TIM15 TRGO TIM2 TRGO TIM4 TRGO EXTI line9 SWTRIG DAC1_CH2 TIM6 TRGO TIM3 TRGO TIM7 TRGO TIM15 TRGO TIM2 TRGO EXTI line9 SWTRIG	TIM6 TRGO TIM8 TRGO(1) TIM7 TRGO TIM5 TRGO(1) TIM2 TRGO TIM4 TRGO(1) EXTI line9 SW TRIG
Supply requirement	2.4 V to 3.6 V	– 1.8 V to 3.6 V – Independent power supply (V_{DDA})
Reference Voltage	External 2.4 V ≤ V_{REF+} ≤ V_{DDA}	External (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)
Configuration	-	SW compatible except for output buffer management

Color key:
= New feature or new architecture
= Same feature, but specification change or enhancement
= Feature not available (NA)
= Differences

1. Except on STM32L43xxx/44xxx.

4.17 Comparator (COMP)

Table 30 presents the differences between the COMP interface of STM32F303 line and STM32L4 Series / STM32L4+ Series:

Table 30. Comp differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

COMP	STM32F303 line	STM32L4 Series STM32L4+ Series
Type	– COMP1/2/3/4/5/6/7 on F3xB/C/D/E – COMP2, COMP4, COMP6 on F3x6/8 rail-to-rail	COMP1, COMP2 rail-to-rail
Input	– COMP1/2/3/4/5/6/7: Inverting: 7 (DAC1_CH1, DAC1_CH2, DAC2_CH1, Vrefint, ¾ Vrefint,½ Vrefint, ¼ Vrefint) – COMP1: Non Inverting: 2 (PA1, PA0) – COMP2: Non Inverting: 3 (PA3, PA7, PA2) – COMP3: Non Inverting: 4 (PB12, PD15, PB14, PD14) – COMP4: Non Inverting: 4 (PB0, PE7, PB2, PE8) – COMP5: Non Inverting: 4 (PB10, PD13, PB13, PD12) – COMP6: Non Inverting: 4 (PB11, PD11, PB15, PD10) – COMP7: Non Inverting: 3 (PC1, PA0, PC0)	– COMP1: Non Inverting: 2 (PC5, PB2) Inverting: 8 (PB1,PC3, DAC1_OUT1/2, VREFINT, 1, 3/4, 1/2, 1/4) – COMP2: Non Inverting: 2 (PB4, PB6) Inverting: 8 (PB3, PB7, DAC1_OUT1/2, VREFINT, 1, 3/4, 1/2, 1/4)
Output	– Generation of break input signals for timers through GPIO alternate function. TIM1/TIM8/TIM20 – Generation of wakeup interrupt or events (EXTI line)	– Generation of break input signals for timers through GPIO alternate function – TIM1/TIM8 (STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – TIM1 (STM32L45xxx/46xxx and STM32L43xxx/44xxx) – Generation of wakeup interrupt or events (EXTI line)

Table 30. Comp differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

COMP	STM32F303 line	STM32L4 Series STM32L4+ Series
Features	Window comparator (only on STM32F303xB/C): COMP1/2, COMP3/4 and COMP5/6	Window comparator
	– Output with blanking source – Programmable hysteresis only on STM32F3xB/C	– Output with blanking source – Programmable hysteresis
	Programmable speed/consumption (only on STM32F3xB/C)	Programmable speed/consumption (COMP1/COMP2)
Supply requirement	2.0 V to 3.6 V	1.62 V to 3.6 V
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	
Color key: = New feature or new architecture = Same feature, but specification change or enhancement		

4.18 Operational amplifier (OPAMP)

STM32L4 Series and STM32L4+ Series devices implement some enhanced OPAMPs compared to STM32F303 line devices. *Table 31* shows the differences.

Table 31. OPAMP differences between STM32F303 line and STM32L4 Series / STM32L4+ Series

OPAMP	STM32F303 line	STM32L4 Series STM32L4+ Series
Instances	– x4 (B/D/C/E) – x1 (6/8)	– x2 (STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – x1 (STM32L45xxx/46xxx and STM32L43xxx/44xxx)
Features	– Rail-to-rail input and output voltage range – Low input bias current – Low input offset voltage – Low power mode – Fast wakeup time – Gain bandwidth of 1 MHz – Programmable gain amplifier (PGA)	

Table 31. OPAMP differences between STM32F303 line and STM32L4 Series / STM32L4+ Series (continued)

OPAMP	STM32F303 line	STM32L4 Series STM32L4+ Series
Configuration	-	– Register mapping is not the same. – Refer to STM32L4 reference manuals for details

Color key:

= Same feature, but specification change or enhancement

= Differences

5 Revision history

Table 32. Document revision history

Date	Revision	Changes
11-Jul-2016	1	Initial release.
13-Feb-2017	2	Updated the whole document with reference to: – STM32L49xxx/4Axxx devices – STM32L47xxx/48xxx devices – STM32L45xxx/46xxx devices – STM32L43xxx/44xxx devices Updated STM32L4 Series reference manual list in cover. Updated *Table 1: STM32L4 Series and STM32L4+ Series memory availability*. Updated *Figure 3: STM32L4 Series / STM32L4+ Series generation of clock for SAI master mode (when MCLK is required)*. Updated Section 2.1: Package availability: – Added *Table 2: Packages available on STM32L4 Series*. – Updated *Table 3: Package availability on STM32F303 line*. – Added *Table 4: STM32F303 line and STM32L4 Series and STM32L4+ Series pinout differences (QFP)*. – Added *Table 5: STM32F303 line and STM32L4 Series / STM32L4+ Series pinout differences (BGA)*. – Added *Section : SMPS packages*. Updated *Table 7: Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx devices* note 1. Updated *Table 8: Bootloader interfaces* adding I2C4 and CAN2. Updated *Table 10: Peripheral address mapping differences* adding I2C4 and CAN2. Updated *Table 12: DMA request differences between STM32F303 line and STM32L4 Series / STM32L4+ Series* adding I2C4 and adding notes for DCMI and HASH. Updated *Table 21: FLASH differences between STM32F303 line and STM32L4 Series / STM32L4+ Series* Flash empty check mechanism feature.
04-Sep-2017	3	Updated whole document to add STM32L4+ Series devices information.
13-Apr-2018	4	Updated: – *Table 8: Bootloader interfaces* – DAC naming: 1 DAC with 2 channels instead of 2 DACs