AN5119
Application note

How to design an application from draft with STNRG011

Introduction

This application note provides information for developing applications with the STNRG011 digital combo multi-mode PFC and time shift LLC resonant controller.

The STNRG011 is a STMicroelectronics® digital device tailored for SMPS applications. It embodies a multi-mode PFC controller, a high voltage double-ended controller for the LLC resonant half-bridge, an 800 V-rated startup generator and a sophisticated digital engine, that manage optimal operation of the three blocks.

All the key application parameters of the device are stored into an internal NVM (non-volatile memory), allowing wide configurability and calibration.

The application note details the steps for developing an application with the STNRG011, from the application layout to the NVM final tuning, including the initial programming of the NVM. For any other information about the STNRG011 product, please refer to the STNRG011 datasheet.

Contents

1 Design power stages

Start designing the power stages as if it is a full analog design. The STNRG011 allows the use of existing analog design with a digital controller with few modifications.

The design of the PFC stage is a standard TM PFC. During the design, fixed thresholds must be taken into account, in particular the PFC OC1 and PFC OC2 comparators' thresholds. The PFC ZCD sensing design is easily achieved by following the layout suggestions. Finally, the bulk resistor voltage divider has to be chosen accordingly to the application. Usually, the standard ratio $k = 5.16 \cdot 10^{-3}$ (i.e. 484.5 V on the bulk voltage correspond to 2.5 V on the PFC_FB pin) is suggested.

During the design of the LLC stage, the split capacitor and the series shunt resistor must be chosen as a trade off taking into account the LLC OC2 threshold but also the available LLC_CS signal at the maximum working frequency (i.e. at the minimum time shift) of the application. The secondary side compensation network could be a single pole compensation, as a patented symmetric time shift control has been implemented. The footprints of a speed-up network could be foreseen in order to improve the response in case of fast load transients. The LLC auxiliary winding turns ratio must be chosen in order to supply the application after power-on. In addition, a resistor voltage divider has to be connected from the LLC auxiliary winding to the LLC_AUX pin for overvoltage protection.

2 Layout the application

During the layout design, attention must be given to the position of the PFC and LLC stages: all the suggestions for analog designs are still valid (separated ground returns, avoid high impedance signals below coils and transformers, the signal and power connections as short as possible, put filters for signals near IC pins and refer their ground to the signal ground, and so on), but the complexity of the 2-stage design within a single IC is still unlikely to be successful even if all these suggestions are followed.

As an example, if the PFC and LLC stages are away from each other, some connections are longer than others. In this case, the suggestion is to design with the IC near the PFC MOSFET and its current sense, because the LLC stage is less susceptible to signal degradation, provided signal R-C filters are put near IC pins. Also ensure that the LLC signal connections are not placed near high voltage switching connections. (i.e. the half-bridge node and the high-voltage floating structure for HVG).

The IC has two ground returns, to increase the noise immunity: power ground on the PGND pin and the signal ground on the SGND pin. Both grounds have to be connected together as close as possible to the IC. Then, route the PGND to the center star ground below the bulk capacitor, while using the SGND to connect the filters ground. It is recommended to put the LLC current sense resistor (connected in series with the split capacitor and towards ground) near the signal ground pin of the IC, to reduce the path to the LLC_CS pin.

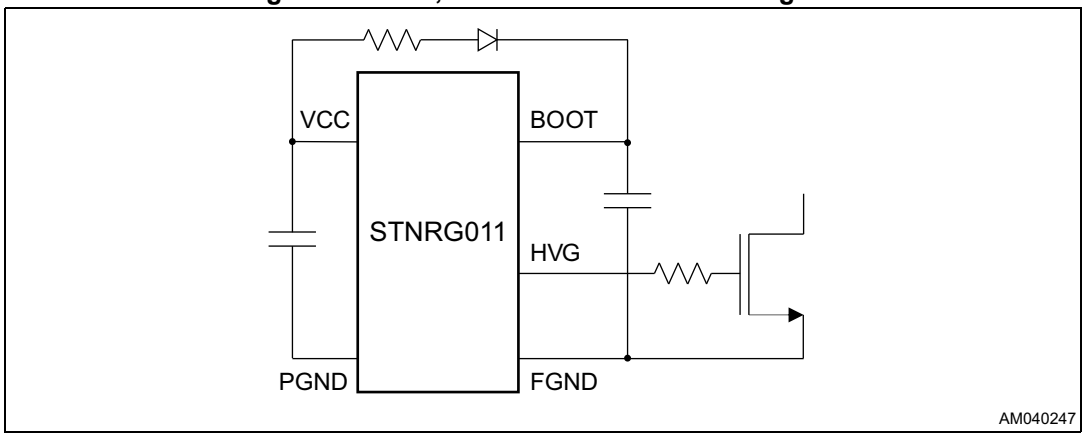
Attention must be given to maximum rating of the pins and use resistor dividers to match signals to the pin range of the IC.

Layout suggestions are described hereafter for each pin or structure.

2.1 BOOT pin1, HVG pin 2, FGND pin 3

The BOOT, HVG and FGND pins are connected to the internal HV floating high-side driver for the upper MOSFET of the LLC resonant section. An external bootstrap diode is necessary to charge the bootstrap capacitor during the LVG on phase, in order to supply the floating structure during the HVG on phase. Connect the FGND pin directly to the source of the high-side MOSFET with a dedicated connection and reduce the loop area from the HVG pin to the FGND pin to reduce the switching emission.

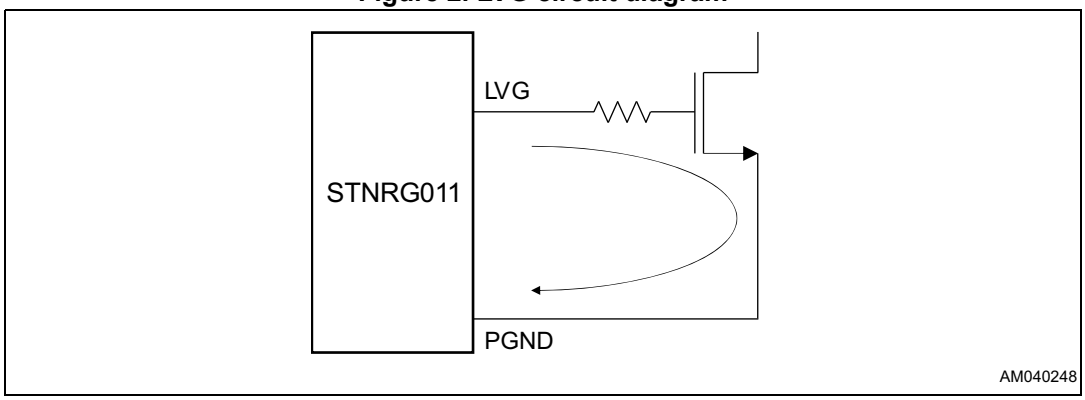
Figure 1. BOOT, HVG and FGND circuit diagram



2.2 LVG pin 5

The LVG pin is the low-side gate drive output and it is connected to the gate of the low-side MOSFET of the resonant half-bridge converter. Reduce the loop area from the LVG pin to the PGND pin and keep the power loop as short as possible to reduce the switching emission.

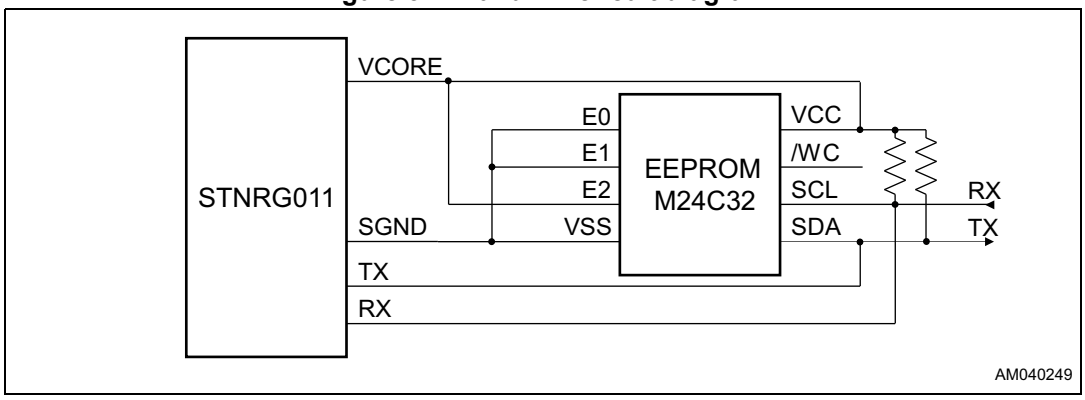
Figure 2. LVG circuit diagram



2.3 TX pin 6, RX pin 7

The TX and RX pins are used for the UART communication for the monitoring function and are shared with the I^2C interface for the EEPROM communications. The TX and RX names are referred to the device for the UART interface. Regarding the I^2C interface, the clock signal SCL is implemented on the RX pin while the data signal SDA is implemented on the TX pin. The EEPROM address must be hardwired at 100.

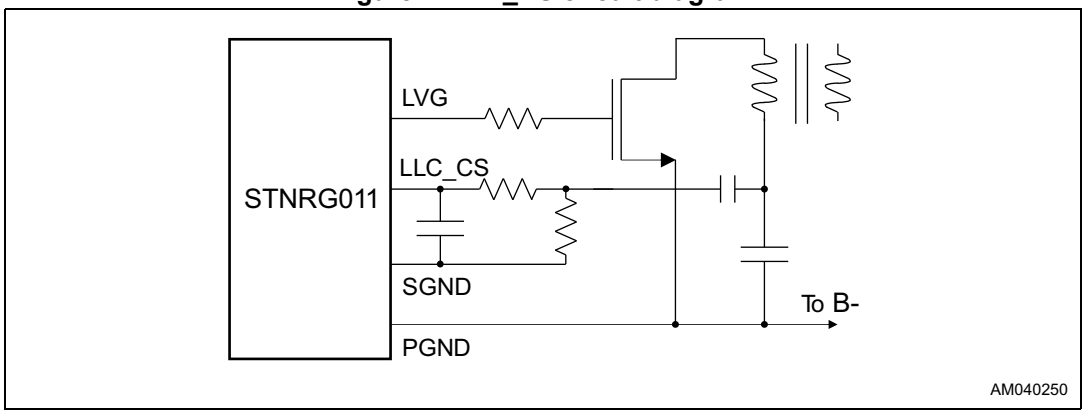
Figure 3. TX and RX circuit diagram



2.4 LLC_CS pin 8

The LLC_CS pin is connected to the resonant current sense resistor through a low pass filter to reduce noise. It is recommended to put the current sense resistor (connected in series with the split capacitor and towards ground) near the SGND pin, to reduce the path to the LLC_CS pin. The low pass filter must have a time constant that filters the switching noise but has a negligible time delay for the resonant current sensing. In addition, the low pass filter must be placed near the pin with ground referred to the SGND pin.

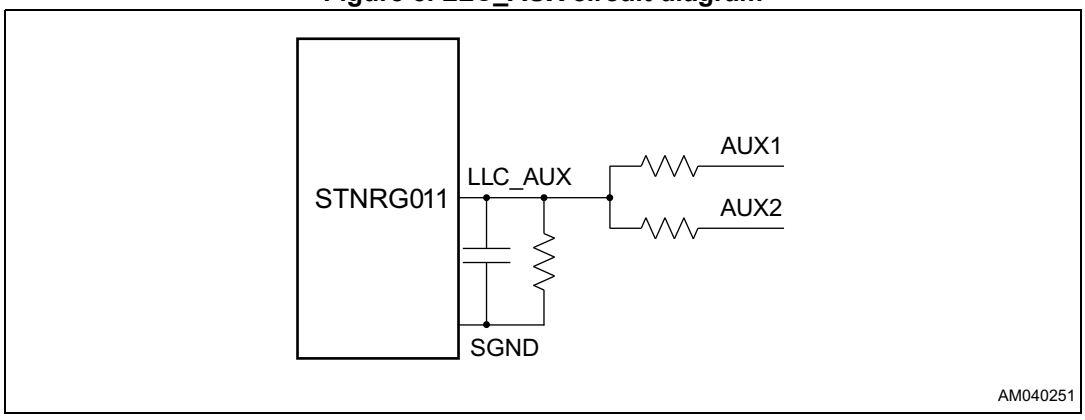
Figure 4. LLC_CS circuit diagram



2.5 LLC_AUX pin 9

The LLC_AUX pin is used to sense the LLC auxiliary voltage for output overvoltage protection and to the drive the external burst mode. It is connected with a resistor divider to the auxiliary coil of the LLC transformer, to sense the output voltage. OVP and external burst mode thresholds must be kept in mind when designing the LLC_AUX network.

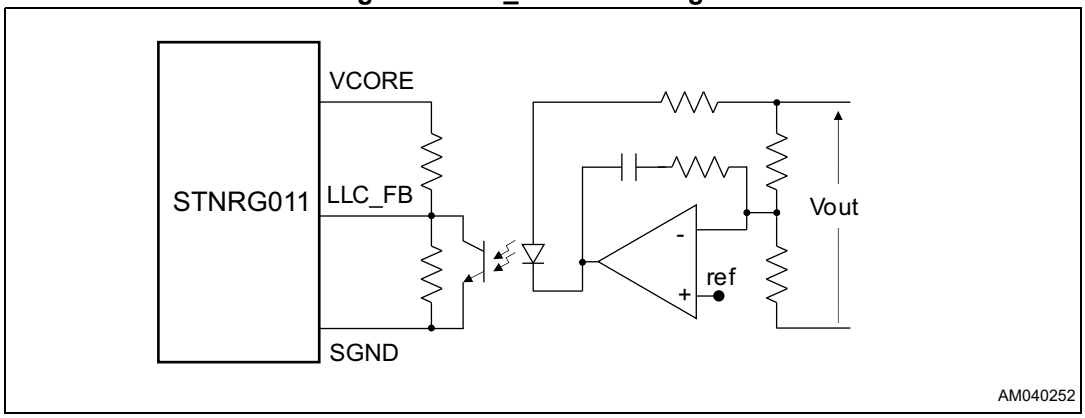
Figure 5. LLC_AUX circuit diagram



2.6 LLC_FB pin 10

The LLC_FB pin is used to sense the feedback signal coming from the secondary side through a low pass filter to reduce noise. It is recommended to refer both the feedback circuitry and the low pass filter to the SGND pin, to increase the noise immunity. It is suggested to design the resistor divider from the VCORE pin to the LLC_FB pin in order to set the voltage just above the FSR of the internal ADC on the LLC_FB pin that is 2.5 V.

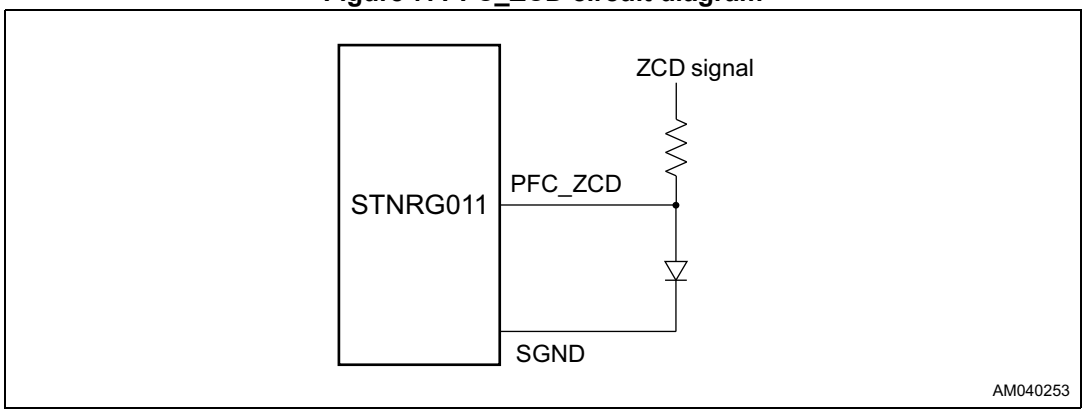
Figure 6. LLC_FB circuit diagram



2.7 PFC_ZCD pin 11

The PFC_ZCD pin is connected to the ZCD signal coming from auxiliary coil of the PFC inductor, with a resistor divider. Even though thresholds are NVM selectable, when the mains peak becomes similar to the bulk voltage, the signal is very small. A signal diode with an anode connected to the PFC_ZCD pin can be used to improve the ZCD signal instead of the lower resistor of the divider. The minimum ZCD resistor value depends on the minimum ZCD auxiliary winding voltage and on the maximum clamped pin current of 2 mA.

Figure 7. PFC_ZCD circuit diagram

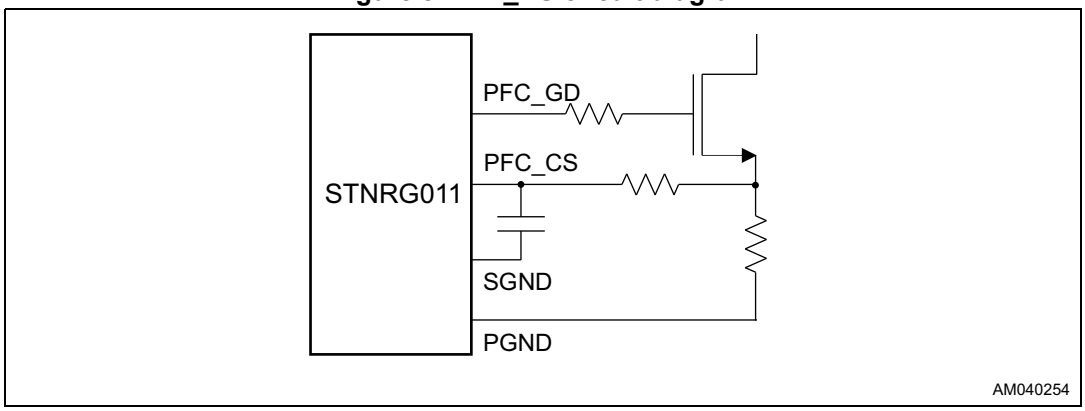


2.8 PFC_CS pin 12

The PFC_CS pin is connected to the PFC sense resistor through a low pass filter to reduce noise. The low pass filter must have a time constant that filters the gate turn-on noise but has a negligible time delay for the PFC current sensing. Also, the low pass filter must be placed near the pin with ground referred to the SGND pin.

The PFC_CS pin is used both for the overcurrent protections and for the THD improver: calculated on-time is applied when PFC_CS voltage exceed the internal threshold.

Figure 8. PFC_CS circuit diagram

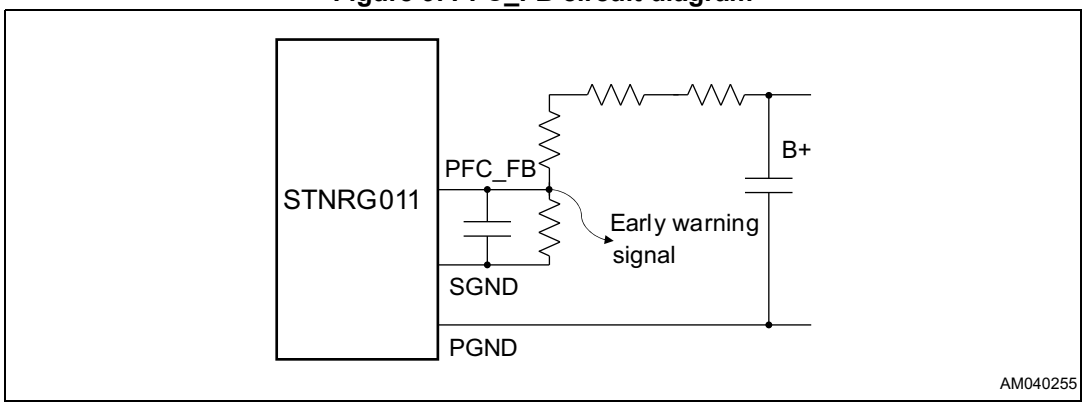


2.9 PFC_FB pin 13

The PFC_FB pin is connected to the bulk voltage resistor divider with a low pass filter to reduce noise. Both the low-side of the resistor divider and the low pass filter must be placed near the pin, with ground referred to the SGND pin.

The pin is also used to generate the early warning signal for the “Power OK” functionality if a fault is detected (for the list of faults that generate an early warning signal, please refer to the STNRG011 datasheet). A latch can be used to store the POK information.

Figure 9. PFC_FB circuit diagram



2.10 VCORE pin 14

The VCORE pin is connected to the internal Vcore, derived from Vcc. Bypass this pin with a 1 μF ceramic capacitor to the SGND.

This pin can be used to supply the EEPROM, as well as the feedback and any other circuitry.

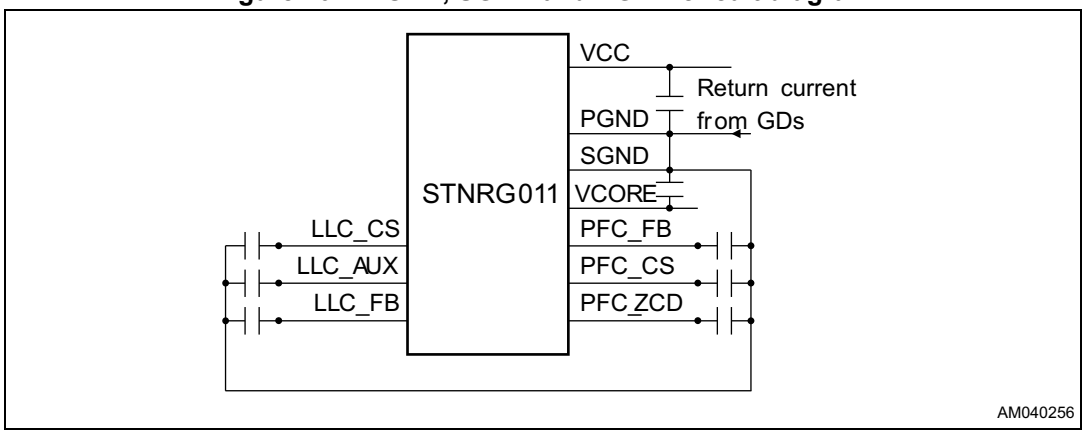
2.11 SGND pin 15, PGND pin 16

The SGND pin is the ground current return for the signal parts of the IC, while the PGND pin is the ground current return for both the PFC gate driver and the low-side gate driver of the half-bridge.

The SGND and PGND pins must be connected together as close as possible to the IC.

Keep the PCB trace that goes from the PGND pin to the sources of the PFC and the low-side LLC MOSFETs separated from the trace that collects the grounding of the bias components and connected to the SGND pin.

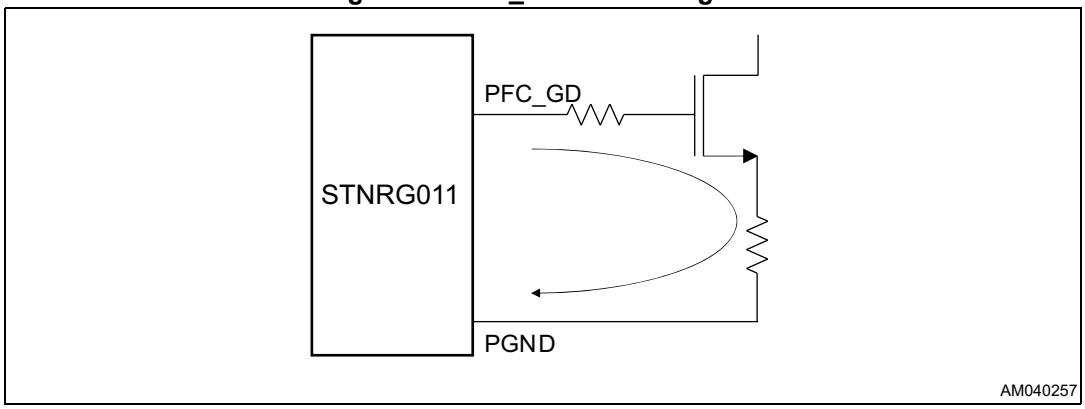
Figure 10. VCORE, SGND and PGND circuit diagram



2.12 PFC_GD pin 17

The PFC_GD pin is the PFC gate drive pin and it is connected to the gate of the PFC MOSFET. During the turn-on and turn-off, the gate current flows also through the sense resistor and could interfere with the PFC current sense. Reduce the loop area from the PFC_GD pin to the PGND pin to increase noise immunity and the reduce the switching emission. The power loop must be kept as short as possible.

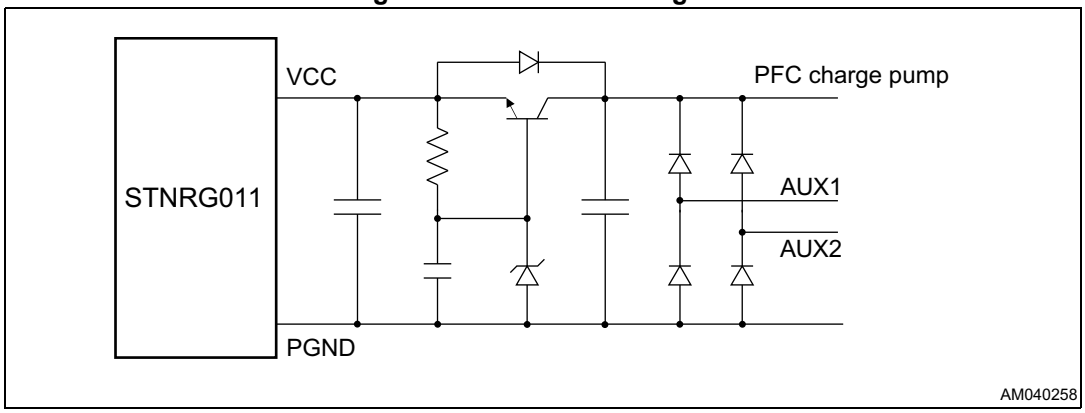
Figure 11. PFC_GD circuit diagram



2.13 VCC pin 18

The VCC pin is used to supply voltage both signal parts of the IC and the gate-drivers. Bypass this pin with a 1 µF ceramic capacitor to the PGND. During start up, capacitors connected to the pin are charged by HVSU from the VAC pin. As soon as the PFC is switched on, the auxiliary winding from the PFC inductor must sustain the Vcc high. During the run mode, the auxiliary winding connected to the LLC transformer must sustain the entire application. When designing the application, ensure that the voltage on this pin does not exceed the minimum value of the internal Zener clamp that is 19 V. For this reason, a series regulator is strongly recommended.

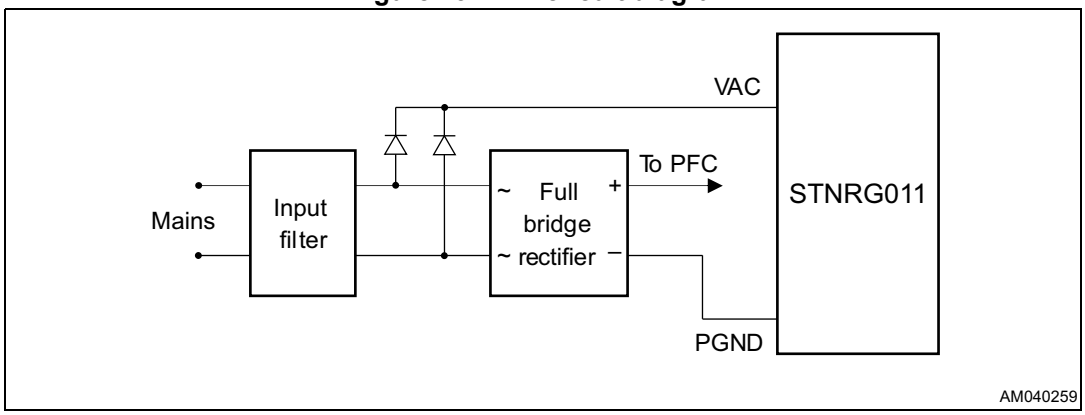
Figure 12. VCC circuit diagram



2.14 VAC pin 20

The VAC pin is used to sense the mains and to charge Vcc capacitors during the start-up. The rectification must be done with a couple of diodes connected directly to the mains, before the input full bridge rectifier but after the input filter. Please note that the device is sensing a low frequency signal (100 Hz ÷ 120 Hz) therefore an economical standard diode should be used (like 1N4007 or similar). Using an ultrafast rectifier will not add any benefit; depending on the board, it could even have the drawback to inject noise on the VAC pin.

Figure 13. VAC circuit diagram



3 NVM parameter programming

In order to modify NVM parameters and check EEPROM content, connect the STEVAL-PCC020V1 board both to the PC and to the STNRG011. A graphical user interface (GUI) allows to modify NVM parameters and to check EEPROM content in an easy way. For more information about the STEVAL-PCC020V1 board and the GUI, please refer to the STEVAL-PCC020V1 user manual UM2342. Enter the ATE mode using the GUI and read the default NVM of the IC. Use the default NVM as the starting point: this NVM has all the protections enabled with latched behavior and this should avoid any damage to the board in case of failure. In case no external EEPROM is used, be sure that “Patch upload from EEPROM” is disabled, otherwise the system will not start. In the other case, the patch upload can be left enabled but the EEPROM must be completely initialized to zero. For information about all the NVM parameters, please refer to UM2340- STNRG011 NVM parameters description.

3.1 PFC parameters

Start setting up the PFC parameters

- Use the low Ki and Kp parameters to have a slow response of the PFC and keep disabled the “PFC boost exiting burst” feature. These parameters will be tuned after the application is running, to improve the behavior of the PFC response of a load transient.
- Set “PFC MOSFET LEB” to the middle value 267 ns. This parameter will be adjusted after the application is running, checking if the PFC MOSFET is prematurely turned off due to the capacitive spike, especially at high mains.
- Set to zero both the THD improver parameters.
- Set the “PFC maximum power” to 2 times the value obtained using the formula in “PFC power calculation” paragraph in the UM2340. Hereafter is reported the final formula:

Equation 1

$$PFC\ \ maximum\ \ power = 2 \cdot \frac{P_{MAX} \cdot L_{PFC}}{7.62V \cdot \mu s}$$

- Set the “PFC pss” to 1/5 of the “PFC maximum power” parameter.
- Set the “PFC pcc” to the maximum. This parameter could be reduced after the burst mode is fully working.
- Set “PFC Min Pin Vskip”, “PFC Max Pin Vskip (delta)”, “PFC Delta Pin Vskip” and “PFC maximum DCM power” parameters to the minimum value. The correct values will be set with the PFC tuning tool after the application is running.
- Set the “PFC Min Tsw Vskip” and the “PFC Max Tsw Vskip” parameters considering the design specifications.
- Set the “Skipping area threshold” to zero. The final value will be set after the application is running with the PFC tuning tool.
- Set the “PFC Vout target” according to the resistor divider from the bulk voltage and the desired PFC output voltage.
- Set the “PFC Vout SS end (delta)” at the voltage LLC has to start. The lowest value 19.5 mV is the best one in case there is no preference (the lower the delta value, the higher the voltage at which LLC starts).

- Set the “PFC UVP threshold (delta)” to the desired value, considering the design specifications. As the starting point, the lowest value 0.156 V is the best to avoid the system working below resonant frequency.
- Set the “PFC SW OVP threshold (delta)” to the middle selection 78.1 mV.

3.2 LLC parameters

Continue setting the LLC parameter

- Select the range the LLC will work, considering the resonance frequency. As a rule of thumb, considering a system designed to work near resonance in nominal condition, if the resonance frequency is greater than 70 kHz the standard range can be used, while if the resonance frequency is less than 60 kHz the low frequency range is suggested.
- Set the “LLC HVG first Ton” considering that the peak value of the resonance current must not trigger the LLC OC2 threshold. This would be to set the parameter to

Equation 2

$$LLC\ \ HVG\ \ first\ \ Ton < \frac{1V}{2 \cdot Rdiv} \cdot \frac{Lres}{PFC\ \ Vout} \cdot \frac{Cres}{Csplit}$$

Where

  - *Lres* is the value of the resonant inductor (i.e. the leakage inductance in case of the integrated transformer) (e.g. 110 μH)
  - *Cres* is the value of the resonance capacitor (e.g. 22 nF)
  - *Rdiv* is the resistor divider from the split capacitor to the LLC_CS pin (e.g. 12 Ω)
  - *PFC Vout* is the output voltage of the PFC (e.g. 400 V)
  - *Csplit* is the splitter capacitance of the resonant tank current (e.g. 330 pF)
- Set the “LLC LVG first TS” as the HVG one. This could be changed after the application is running, to improve the resonant current shape during the initial LLC pulses.
- Set the “LLC dead time” as half-bridge design requirements.
- Set the “LLC soft-start speed” to the minimum value. This could be increased in case the LLC soft-start needs to be faster.
- Set the “Minimum time shift” and “Maximum time shift” parameters as design requirement. It is suggested to set the “Minimum time shift” equal to 358.3 ns (716.7 ns in case “LLC low frequency range” is enabled) in order to avoid the burst mode entering at the first startup.
- Set the “LLC OLP threshold” to the maximum value to exclude the OLP feature. This value will be fine-tuned after the application is running.
- Set the “LLC OLP timeout” parameter as the design requirement.
- Set the “ACP sensitivity” high and “Hard ACP detection” and “Soft ACP feature” enabled to avoid damaging when the LLC starts for the first time.
- Set the “Soft ACP entering threshold”: as a rule of thumb, a good starting value is between 1/30 and 1/40 of the resonance period.
- Set the “Soft ACP TS decrement”: as a rule of thumb, a good starting value is between 1/20 and 1/30 of the resonance period.
- Set the “Maximum soft ACP occurrences” to the minimum. This value could be set to the maximum if the soft ACP intervention is aggressive.

3.3 Burst mode parameters

Set the burst mode parameters.

- Set the “External burst mode” feature depending on the application. If the feature is enabled, please be sure that the LLC_AUX pin is kept higher than 0.9 V to to avoid entering burst mode. The pure or hybrid external burst mode will be selected after the application is running and burst mode parameters have been set.
- Set the “BM enter for min TS” to disable. The feature could be enabled, if required, after having set burst mode parameters.
- Set the “Burst entering digital filtering” to the maximum value 990 us. This value could be reduced when the application is fully running, in case lower filtering is needed.
- Set the “LLC_FB burst entering thr” to the minimum, to avoid entering burst mode at initial turn-on.
- Set the “LLC_FB burst wake-up thr” and the “Min TS in burst mode” considering the time shift necessary to work at the resonance and set the parameters with a time shift slightly higher. As the starting point, 1/3 of the resonance period can be used for the “Min TS in burst mode”. Set the “LLC_FB burst wake-up thr” considering the equivalent time shift, and set it below the “Min TS in burst mode” parameter.
- Set the “LLC_FB burst wake-up hyst” to the minimum.
- Set the “Min number of burst pulses” equal to 4 and the “Max number of burst pulses (delta)” equal to 2. These parameters, together with the “Min TS in burst mode” are strictly related to the output ripple in the burst mode and they will be adjusted when the application is running. Reducing the “Min number of burst pulses” up to 2, the PFC turn-on time could not be enough to keep the bulk voltage high, as the PFC is synchronized with the LLC during burst mode. For this reason, 4 is the suggested starting value.
- Set the “Min time between burst seq” to 10.2 ms and the “Max time between burst seq (delta)” to 4.97 ms.These two values will be adjusted looking at the LLC_FB voltage in the burst mode, selecting the values that avoid the saturation of the optocoupler.
- Set the “Minimum period to exit burst” at the minimum value 66.7 μs, in order to exit the burst at very high loads. This parameter will be adjusted measuring the period between burst sequences at the burst mode exit current.
- Set the “No-burst window width” to 7.5 ms.

3.4 Comparators setting

Set the comparators filtering and thresholds

- Set the “Surge comparator digital filtering” to the maximum value 500 ns. This could be reduced if a faster reaction time to surge is needed.
- Set the “PFC CS comp digital filtering” to the maximum value 50 ns while the “PFC CS comp hysteresis” is set to the minimum value 5 mV.
- Set the “PFC OC2 digital filtering” to a middle value to filter noise but to have a fast response in case of the protection is triggered.
- Set the “PFC OC1 digital filtering (delta)” and the “PFC ZCD digital filtering” to the minimum value 33.3 ns.
- Set the “PFC ZCD comp falling thr” and the “PFC ZCD comp rising thr” according to the design. However it is suggested to set them to 0 mV and 110 mV for falling and rising thresholds respectively.
- Set the “PFC HW OVP digital filtering”, “LLC OLP comp digital filtering” and “LLC OC2 comp digital filtering” to a middle value to filter noise but to have a fast response in case the protection is triggered.
- Set the “LLC ZCD comp digital filtering” to a middle value (e.g. 250 ns). This value has to be adjusted when the application is running, looking at the noise on the LLC_CS pin.
- Set the “LLC ZCD comp hysteresis” to the max. value 10 mV.
- Set the “LLC OVP digital filtering” to a middle value to filter noise but to have a fast response in case the protection is triggered.

At this point, write the NVM on the device and exit the ATE mode.

4 Getting ready and turn-on the board

Before applying AC voltage at the input, connect the probes of the oscilloscope to the most relevant signals of the board. Those suggested are: the bulk voltage, Vcc, LLC_FB pin and output voltage. The bulk voltage can be used to trigger the AC turn-on. If other channels are available connect the PFC_CS pin, PFC_ZCD pin, LLC_CS pin and the half-bridge node.

Load the output of the converter with half the maximum load and turn on the AC voltage: if the board is designed correctly and no faults have been triggered, the output voltage should be regulated. Otherwise, turn-off AC voltage, have a look at the oscilloscope's waveforms and at the EEPROM content.

The fault that triggered the system to turn off will be written to the EEPROM. This will restrict the research field and usually identify the fault condition. Sometimes, the fault triggered could be indirect. As an example, a PFC_CS disconnection fault could be the PFC_CS pin disconnected from the sense resistors but also the PFC_GD pin disconnected from the PFC MOSFET.

When the system starts without any fault, the NVM fine-tuning can proceed.

5 NVM fine-tuning

5.1 PFC parameters

The first step is to set the PFC parameters: check with oscilloscope that the PFC MOSFET is never prematurely turned-off, especially at high mains. If this happens, increase the “PFC MOSFET LEB” parameter. Check also if the PFC voltage regulation is stable. In case the PFC soft-start is too slow, the “PFC pss” parameter can be increased. Write new values on the NVM and check the behavior.

Try to turn on the application at full load and check that the PFC regulation is stable. In case the PFC reaches the SW OVP threshold and oscillates, try to increase the “PFC Kp” and/or the “PFC Ki” parameters and try again.

When the PFC does not reach the SW OVP threshold during the full load startup, open the PFC tuning tool and follow the instructions. The software will help to set all the parameters related to the PFC mode, from the ReCOT functionality to valleys-skipping and DCM parameters. During measurements, the GUI remotely changes the PFC mode in order to measure the reported power. If the mode change fails (especially at the full load), check the PFC behavior: if the PFC SW OVP is triggered, try to increase the “PFC Ki” and “PFC Kp” parameters, while if the PFC OC1 comparator is triggered, try to increase the “PFC OC1 digital filtering (delta)” parameter.

When the procedure is completed, turn-off the AC mains and set the new PFC parameters in the NVM. Then turn on the AC mains again and check if the PFC starts correctly, checking also that the EEPROM content does not show any new fault.

Check that the system always works out of the skipping area when the load is higher than 75 W and at different mains voltages (suggested at 100 Vac and 230 Vac as JEIDA-MITI class D limits and EN61000-3-2 class D limits respectively). It is suggested to to check by decreasing the load in order to enter the skipping area region and increasing the load, verifying the input power for which the system exits the skipping area. The accuracy of the skipping area power threshold is inversely proportional to the compensation of the ReCOT functionality.

Set the “PFC maximum power” parameter by setting the load to the overload condition (that will be set later) and reading the input raw value from the main window of the GUI. Increase the observed value by 30% in order to have enough margin during transient. The value can be further adjusted looking at the PFC stage transient response.

Last but not the least, increase (if necessary) the “PFC Ki” and/or “PFC Kp” parameters to improve the dynamic performance of the PFC.

Write down on the NVM all the parameters before continuing with the board set up.

5.2 LLC and burst mode parameters

After the PFC is fully working, the LLC and burst mode parameters have to be fine-tuned.

Turn on AC mains with half load and verify the LLC soft-start with the oscilloscope: check the initial LVG and HVG pulses and verify that the LLC_CS pin has enough margin from the LLC OC2 threshold at 700 mV. In case the initial pulses bring the resonant tank current near the OC2 threshold, reduce the “LLC HVG first Ton” parameter. If needed, the “LLC LVG first TS” parameter can be modified to have a centered-to-zero resonant current from the initial pulses.

In case the LLC soft-start is too slow, the “LLC soft-start speed” parameter can be increased.

In order to set the “LLC OLP threshold” parameter, increase the load up to the overload threshold and read the peak voltage value of the LLC_CS signal. Use this value to set the “LLC OLP threshold” parameter.

With AC mains turned-on, try to reduce the load to zero (or if the tank is not designed to regulate the zero load, decrease the load until the output voltage regulation is lost) and verify that the signal on the LLC_CS pin is still high enough, especially when the half-bridge changes state. In case the system triggers the Hard ACP fault, probably the half-bridge commutations corrupts the LLC_CS signal. In this case, try to increase the “LLC ZCD comp digital filtering” or improve the LLC_CS pin filtering. In addition, the “Minimum time shift” could be increased.

It is mandatory to set the “LLC ZCD comp digital filtering” before setting all the other LLC and burst mode parameters. If the “LLC ZCD comp digital filtering” parameter needs to be changed after all the other parameters have been set up then the burst mode entering and exiting threshold will probably change and it will be necessary to slightly tune those parameters again.

In case the pure external burst mode is requested, it is not necessary to change the “LLC_FB burst entering thr” parameter, because the minimum value is already set. Otherwise, in case the hybrid external burst mode or the standard burst mode is requested, set the load at the desired burst mode entering threshold and read the LLC_FB voltage value. Use this value to update the “LLC_FB burst entering thr” parameter, writing the nearest parameter on the NVM.

Turn-on again the AC mains at half load and slightly decrease the load up to the burst mode entering threshold: the system has to enter the burst mode. Please note that in case the hybrid external burst mode has been selected, the external BM comparator on the LLC_AUX pin must be low in order to enter burst mode. The system could be able to sustain the burst mode with the previously selected parameters or could shut down. In the second case, try to increase the “Min TS in burst mode” and the “Max number of burst pulses (delta)” parameters.

In case the system is able to sustain the burst, go to zero load and verify bulk voltage and Vcc regulation, as well as the output voltage ripple and LLC_FB behavior. In case the system shuts down for UVLO, try to increase the “Min number of burst pulses” parameter. If it is still not able to sustain the Vcc, the current consumption from the VCC and VCORE pins must be reduced or a bleeder has to be connected to the output of the converter, to increase the burst frequency. A re-design of the LLC transformer could be necessary if none of the proposed solutions is effective. Depending on the LLC feedback compensations, it could happen that the LLC_FB voltage is sampled higher than “LLC_FB burst wake-up thr” at the end of the burst mode and the burst is not stable. In this case, the system exits the burst

mode because it senses that a transient load occurred. In order to avoid this issue, higher “Min TS in burst mode” or higher “Min number of burst pulses” are requested.

Check the LLC_FB voltage behavior by increasing the load, in order to select the “Min time between burst seq” and “Max time between burst seq (delta)” parameters that avoid saturation of the optocoupler collector voltage.

Increase the load up to the burst mode exit point and measure the time between burst sequences: use this time to select the appropriate “Minimum period to exit burst”. In case the system is not able to sustain the output voltage in burst mode at the desired burst mode exit point, it is necessary to increase the “Max number of burst pulses (delta)” parameter. Repeat the procedure to measure and set the “Minimum period to exit burst” parameter and verify it decreasing and increasing the load.

Check the soft ACP intervention during the heavy load transient, and correct soft ACP parameters consequently. The “Soft ACP entering threshold” and/or the “Soft ACP TS decrement” parameters could be increased to reduce the peak of the resonant current during the load transient and avoid triggering the LLC OC2 comparator. The “Maximum soft ACP occurrences” parameter could be increased in case the soft ACP intervention shuts down the system during the load transient.

5.3 System parameters

After the fine-tuning has been done and the board is fully working, the system parameters can be adjusted as design requirements. As an example, the user can enable the “Shutdown feature” as well as the “Early Warning feature” or disable the “System monitoring”. The fault behavior and the maximum number of the OC2 for the PFC and the LLC can be changed if needed, as well as consecutive comparators' setting.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
19-Feb-2018	1	Initial release.