Introduction

This document gives information about H-bridge driver embedded in the L99DZ80EP and L99DZ81EP: those devices include an SPI-programmable slew-rate circuit that drives 4 external MOSFETs in a H-bridge configuration supporting electric-window applications.
L99DZ80EP and L99DZ81EP devices provide, through pins GH1/2, GL1/2 and SL1/2, dedicated driving signals to the external 4 MOSFETs.
Typical curves are described in the following figure.
Some transitions are now analyzed:

**Transition A**
Threshold voltage ext FET sampled and stored in $C_{VSW}$ during Miller Plateau $\leftrightarrow V_{TH}$.
During this phase, threshold stored in $C_{VSW}$ during Miller Plateau is increased by $I_{\text{Charge}} \times R_{\text{Gate}}$ in reference to $V_{TH}$ of the external MOSFET.

**Transition B**
Switch-off started with $R_{SW}$, "hard switching".

**Transition C**
- Reaching $V_{TH}$, $R_{SW}$ is turned-off by opening $SW_{RDSW}$
- Opening of $SW_{RDSW}$ is done with a certain delay
- Afterwards gate discharge is done by the programmed current source ($I_{\text{discharge}}$)
During this phase, $V_{Gate}$ is decreased by resistive divider $R_{SW} \leftrightarrow R_{\text{gate}}$ and "Virtually" the threshold to switch from switch mode to current mode is lower than real gate source voltage on external FET.

*Figure 4: "Transition C measurement on a real device" shows measurements performed on a real device.*
2.1 How to choose a proper Rgate resistance

Charge in the beginning of turn-off phase is discharged by the hard switch in series with the external gate resistance. Average current during this phase is approximately \((5V + V_{TH}/2) / (R_{SW} + R_{Gate})\).

Due to virtual decreased sample voltage (by resistive divider \(R_{SW} \& R_{Gate}\)) the transition from switch mode to current control mode is started almost immediately after start of turn-off of ext FET (depending on size of \(R_{Gate}\)).

Delay of opening \(SW_{RDSW}\) is approximately 100 ns (typical value).

During this time \(Q_{gate}\) must NOT be discharged to ensure to enter \(Q_{GD}\) plateau. As rule of thumb the according \(R_{Gate}\) can be calculated by the following formula:

\[ R_{Gate} \geq (5V + V_{TH}/2) \times 100ns / Q_{gate} - R_{SW} \]

That value of \(R_{Gate}\) is needed to enter current source mode.
## Table 1: Rgate values as per different MOSFET choice

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>Q_{Total} (nC)</th>
<th>Q_{GD} (nC)</th>
<th>Q_{GS} (nC)</th>
<th>Q_{Total} – Q_{GD} – Q_{GS} (nC)</th>
<th>V_{TH @ 40A} (V)</th>
<th>Calculated R_{Gate} (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST STD64N4F6AG</td>
<td>44</td>
<td>15</td>
<td>12</td>
<td>18</td>
<td>5.5</td>
<td>38</td>
</tr>
<tr>
<td>ST STD80N4F6AG</td>
<td>36</td>
<td>9</td>
<td>11</td>
<td>16</td>
<td>4.8</td>
<td>41</td>
</tr>
<tr>
<td>ST VNH7013</td>
<td>36</td>
<td>5</td>
<td>8.5</td>
<td>22.5</td>
<td>Not specified</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(2 ... 4)</td>
<td>(@V_{TH} = 5V)</td>
</tr>
<tr>
<td>Supplier A</td>
<td>45</td>
<td>12.6</td>
<td>10</td>
<td>22.4</td>
<td>4V</td>
<td>26</td>
</tr>
<tr>
<td>Supplier B</td>
<td>17.2</td>
<td>2.4</td>
<td>8</td>
<td>6.8</td>
<td>5.5V</td>
<td>109</td>
</tr>
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Revision history

Table 2: Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tbody>
<tr>
<td>17-Feb-2016</td>
<td>1</td>
<td>Initial release.</td>
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<tr>
<td>29-Feb-2016</td>
<td>2</td>
<td>Updated Figure 2: &quot;Simplified schematic of driver for external high-side&quot; Section 2.1: &quot;How to choose a proper Rgate resistance&quot;:</td>
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<tr>
<td></td>
<td></td>
<td>• Updated equation</td>
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